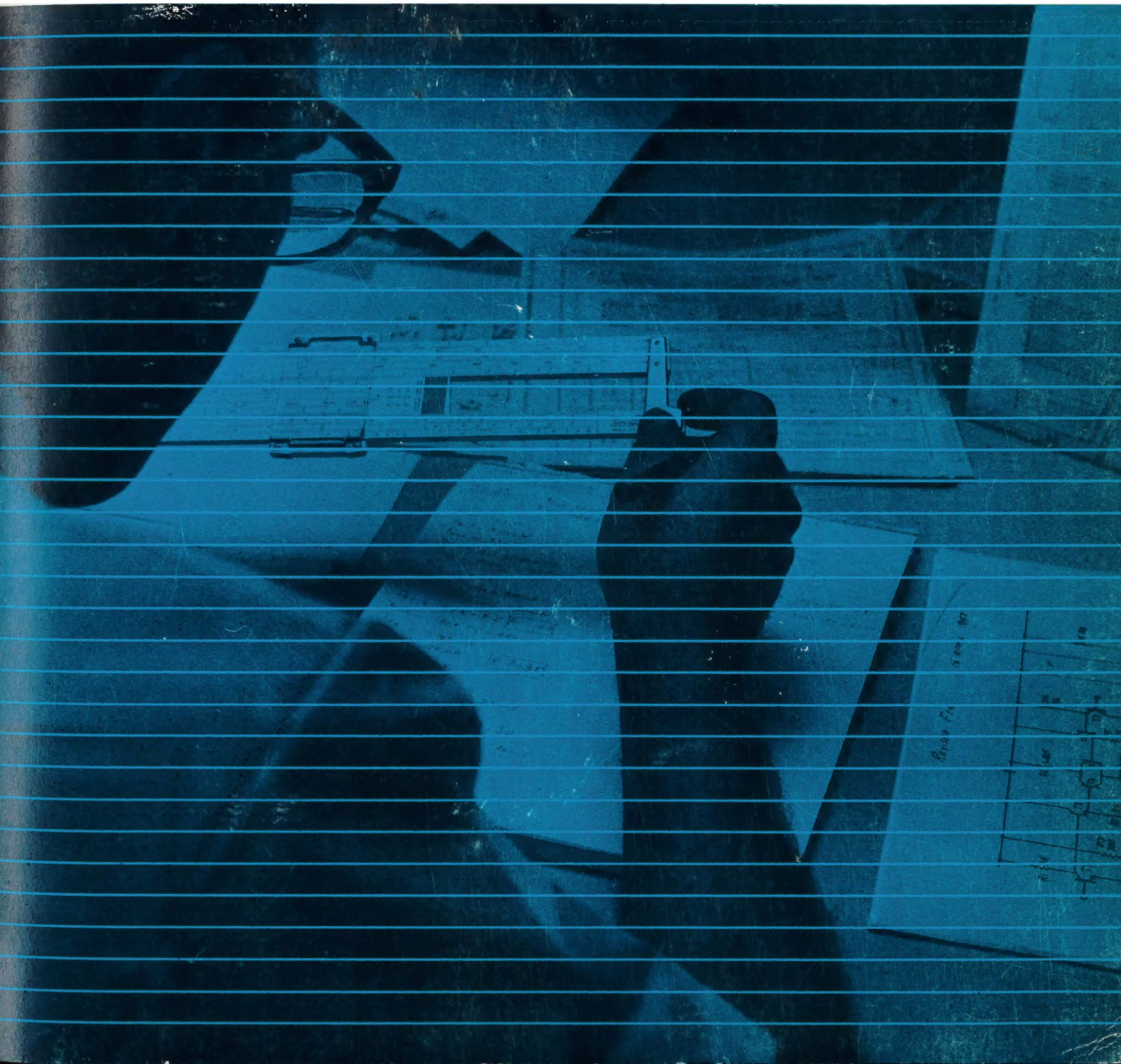# Fairchild Semiconductor
Linear Integrated Circuits
Applications Handbook

Fairchild Semiconductor Linear Integrated Circuits Applications Handbook

Written and Edited by
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Linear Microcircuit Engineering
Fairchild Semiconductor

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During the past several years, the numerous advantages of design with linear integrated circuits have become readily apparent. Total monolithic subsystem integration leads to improved system performance at lower over-all cost. Unfortunately, however, pertinent information and guidelines to the effective utilization of linear circuits are generally lacking.

Sensing the need for one comprehensive source of information, Fairchild Semiconductor has prepared the Linear Integrated Circuits Applications Handbook. This handbook contains detailed explanations and circuit diagrams on all of Fairchild's linear circuits, the design philosophy behind the circuits themselves, and many practical applications illustrative of their versatility.

The LIC Applications Handbook should provide significant insight into the advantages and limitations inherent in monolithic construction and how these relate to specific systems design problems, and serve as a convenient reference for all users of linear integrated circuits.

INTEGRATED CIRCUIT FABRICATION

The manufacturing process used to construct linear microcircuits is an extension of the Planar* process developed by Fairchild to produce silicon transistors. An integrated circuit begins with the growth of high-purity silicon crystals: a small, perfect seed crystal, carefully selected for low dislocation and imperfection counts, is lowered into molten silicon and slowly withdrawn under precise control, forming a large, single crystal about 6 inches long and 1 inch in diameter. A boron impurity is added during growth to make the crystal P-type, rather than the N-type starting material of regular NPN transistors.

The finished crystal is sliced with a diamond saw into many thin wafers, each about 12 mils thick. The cut wafer is then lapped flat using a very fine grit abrasive, and chemically etched to form an extremely smooth surface. The polished wafers are placed in a furnace containing an oxidizing atmosphere at 1200°C. Oxygen penetrates the crystal lattice at the surface of the wafer, combining chemically with surface silicon atoms to form silicon dioxide — an inert, stable glass which encapsulates and passivates the wafer surface. This step is the key to the reliability and production economy attained through the Planar process.

The passivated wafer begins to take the form of an integrated circuit with the collector cutout step. The wafer is coated with a photosensitive material in a darkroom, and then exposed to light through a high resolution mask. Those portions not exposed are soluble and easily removed with a solvent rinse. At this point, an etch is used to remove the silicon dioxide from those areas not protected by the film of photosensitive material. In this way, cutouts for collector diffusion are photo-engraved

through the protective passivating silicon dioxide layer. The wafers are placed into a special high-temperature furnace whose atmosphere contains an N-type dopant. The temperature is raised, and the impurity diffused into the exposed silicon, forming a highly doped N^+ region. This N^+ diffusion is necessary to create a very low transistor collector resistance. Figure 1(a) shows the cross section of a transistor at this point in the process; the surface pattern for a typical integrated circuit is given in Figure 1(b).

With N^+ material diffused within the P substrate, the next step is the growth of the epitaxial layer. This is accomplished by first removing the passivating surface of silicon dioxide by etching with hydrofluoric acid. The wafers are then placed within a thermal reaction chamber where volatile gases are introduced, and through chemical reactions, N-doped silicon is grown on the wafer surfaces. Under these conditions, the growing layer assumes the same crystal orientation as the substrate wafer and becomes an addition or extension of this material. The thickness and resistivity of this epitaxial layer affect the voltage breakdown and saturation parameters of the finished device. After the epitaxial growth, an oxide is grown on the wafer as before, forming a new passivation for the rest of the manufacturing process (Figure 2).

Isolation masking and diffusion must now be performed to electrically isolate transistors and resistors from one another. Bands are etched through the silicon dioxide surface to prepare for the isolation of individual circuit parts. The wafers are then placed into a furnace operating at a controlled high temperature in an atmosphere of boron (P-type dopant) for isolation diffusion. The

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*Planar is a patented Fairchild process.

SiO$_2$

p SUBSTRATE   START

N+

FINISH

(a) CROSS SECTION

(b) SURFACE PATTERN
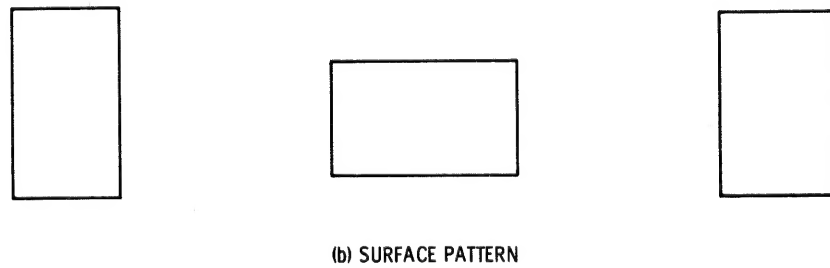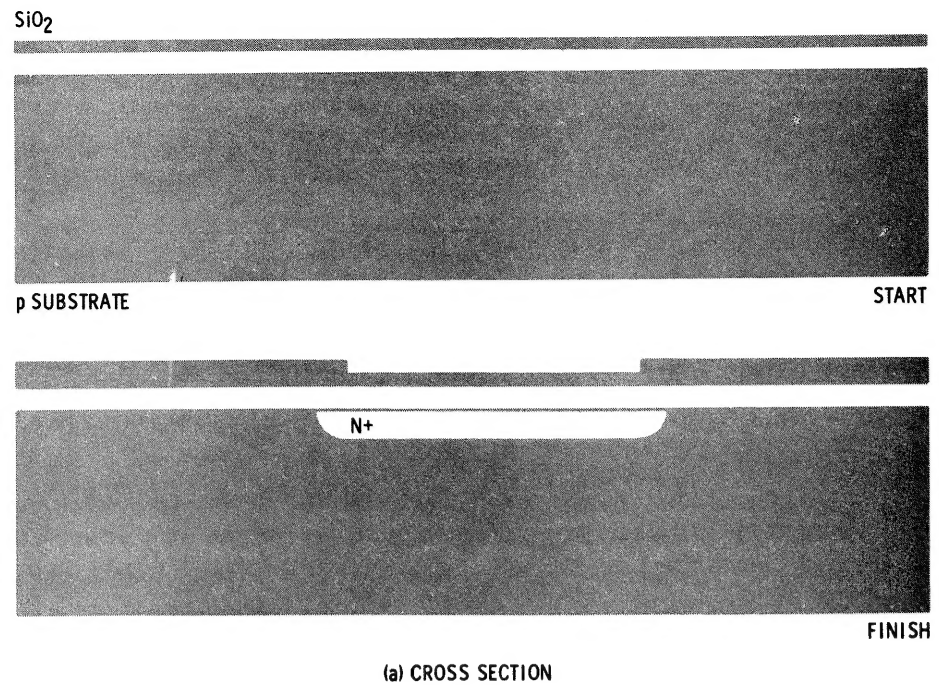
Fig. 1 Collector Cut-Out
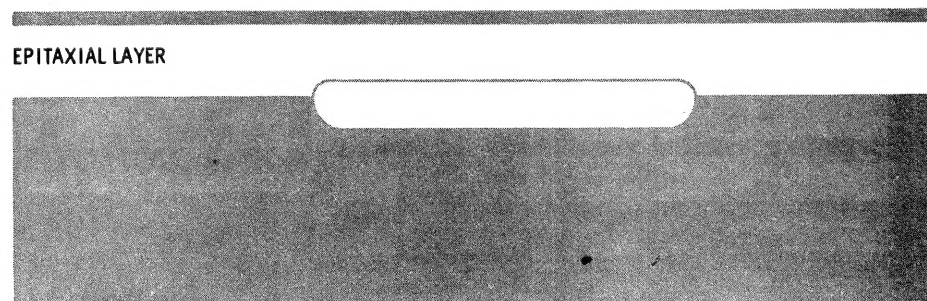
EPITAXIAL LAYER

Fig. 2 Epitaxial Growth
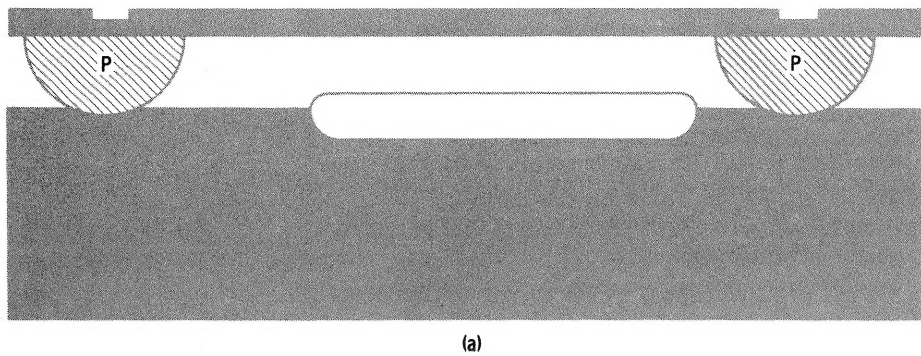
(a)
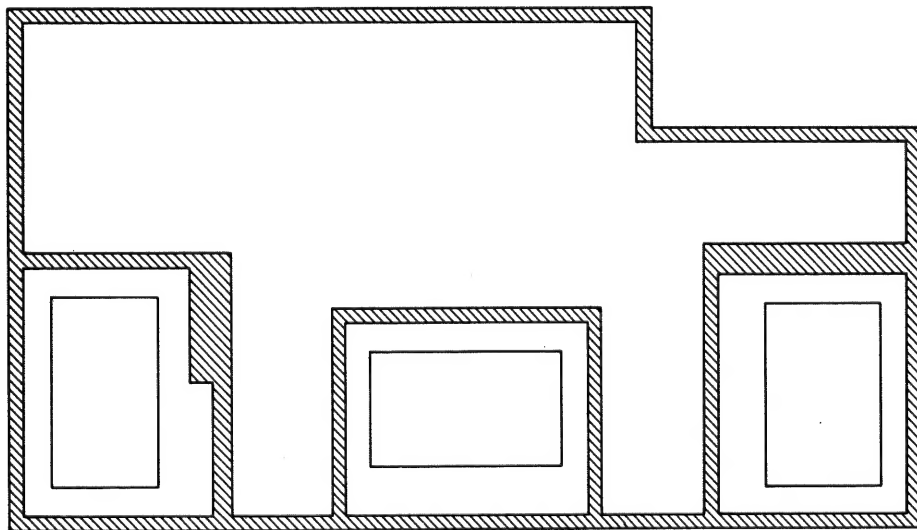
(b)

Fig. 3 Isolation

dopant diffuses through the exposed epitaxial N-type layer, forming a highly concentrated P-type region extending through to the P-type substrate. During the diffusion, the silicon dioxide layer regrows over the masked area. In this manner, isolated pockets of N-type material, which will become the collector regions or resistor regions, are formed (Figure 3). The regions are isolated from each other by the back-to-back diodes created by the isolation diffusion. If the substrate is connected to the most negative circuit potential, then each transistor has its collector connected to the cathode of a diode which can never become forward biased.

The wafer is again masked and etched for the simultaneous diffusion of the base region and resistors. Once again, boron is used as the diffusing impurity in this high-temperature diffusion. The base region is diffused into the N-type epitaxial layer to form the collector-base diode of each transistor as well as all the resistors in the circuit. The oxygen atmosphere in the furnace re-oxidizes the cutout portions of the wafer surface and seals them against contamination or injury. As the diffusion progresses downward into the wafer, it also proceeds laterally, diffusing into the silicon covered by the original protective oxide. This is shown in Figure 4.

3

(a)

(b)
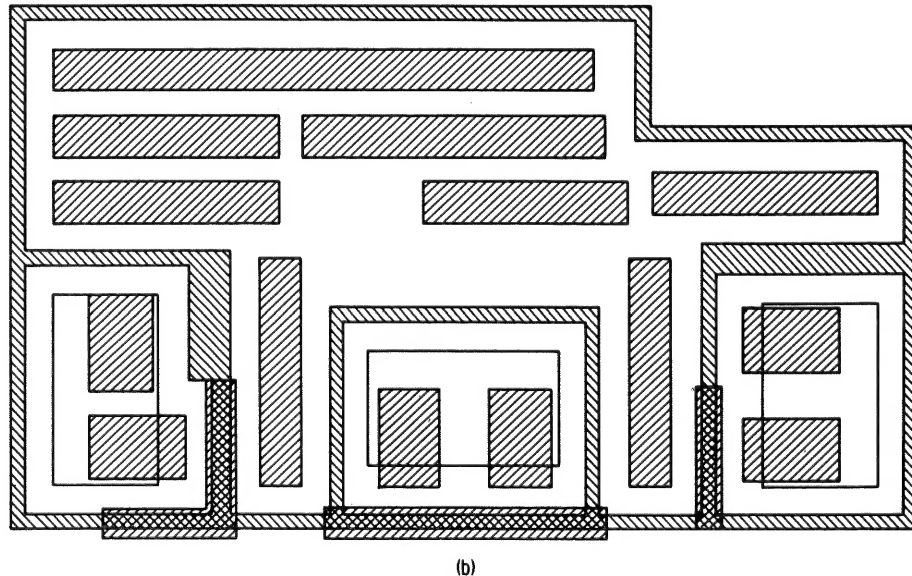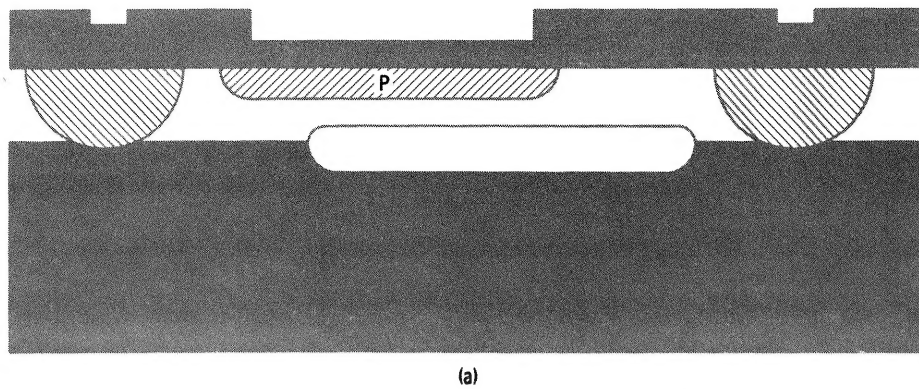
Fig. 4 Base Diffusion

Another precisely indexed masking step is performed to remove oxide for the emitter diffusion and for the top-side collector contacts. In a high-temperature step, phosphorus (an N-type impurity) is diffused into the surface at 1200°C. This impurity forms the emitter region. Again, silicon dioxide forms as the diffusion progresses, covering the photoengraved area and sealing the surface. Side diffusion carries the junction underneath the protective layer. Notice in Figure 5 that in each case, the diffused region ends underneath an oxide that existed previously. This oxide permanently protects the actual junctions of the device against exposure to the outside environment.
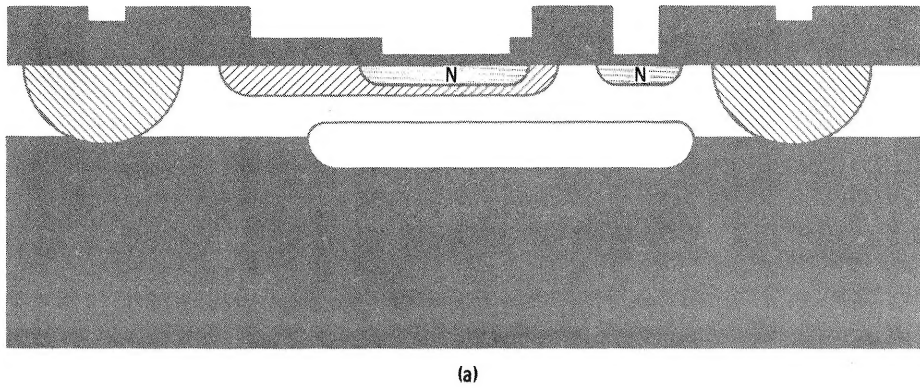
(a)
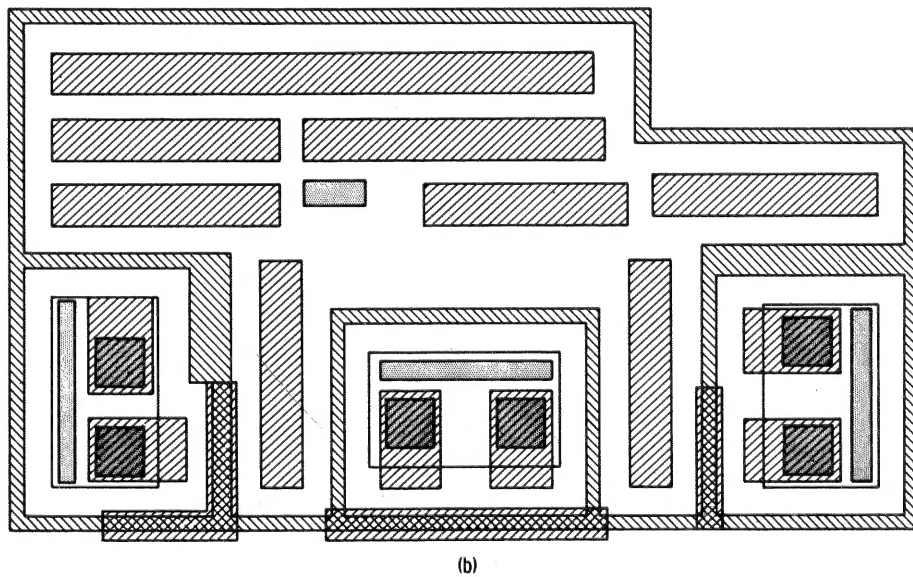
(b)

Fig. 5 Emitter Diffusion

At this point, the transistors and resistors of the integrated circuit are complete. They must now be intraconnected to form the desired circuit function. This is done by evaporating metal onto the surface of the silicon wafer using the Metal-Over-Oxide process.* Before this can be done, however, a hole must be photoengraved over the appropriate regions so that the metal can make contact.

This is done in a masking step similar to the others (Figure 6). The wafers are now placed into a high-vacuum chamber containing a metal evaporator. Aluminum is boiled from a hot tungsten filament. The evaporated metal deposits in a thin, even coat over the entire wafer surface. In this manner, many wafers, comprising several thousand linear microcircuits, are processed at one time.

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*Metal-Over-Oxide is a patented Fairchild process.

(a)

(b)
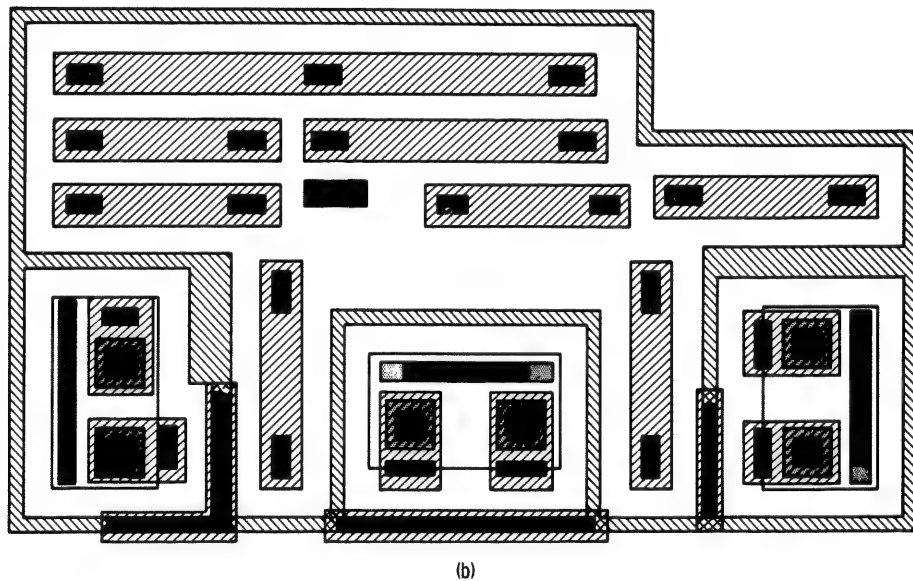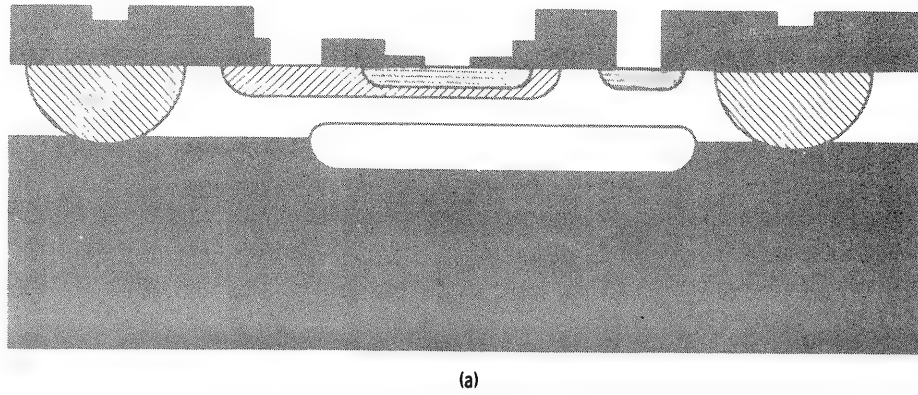
Fig. 6 Exposure of Contact Areas

In another precise photoengraving step, the aluminum layer is masked and selectively etched to leave a pattern of intraconnections between transistor and resistor elements in the circuit. All connections to the outside—inputs, outputs, power supply, and ground—are brought out to the periphery of the element as large aluminum pads for easy, reliable connections. The wafers then are placed in an alloying oven so that the aluminum intraconnections will make good electrical contact with the circuit elements. The wafer is now complete (Figure 7) and needs only to be cut into individual elements and packaged.

Up to this point, all operations have been on many wafers at a time. The elimination of separate handling is a major factor in the reduction of production costs. This batch processing also increases the reliability and uniformity of devices.

Each integrated circuit on the wafer is electrically tested by a special tester that makes contact to the aluminum pads with a set of very finely-pointed probes. Units that fail are marked with a dot of colored dye to distinguish them from functional units after the wafer is cut apart. The wafer
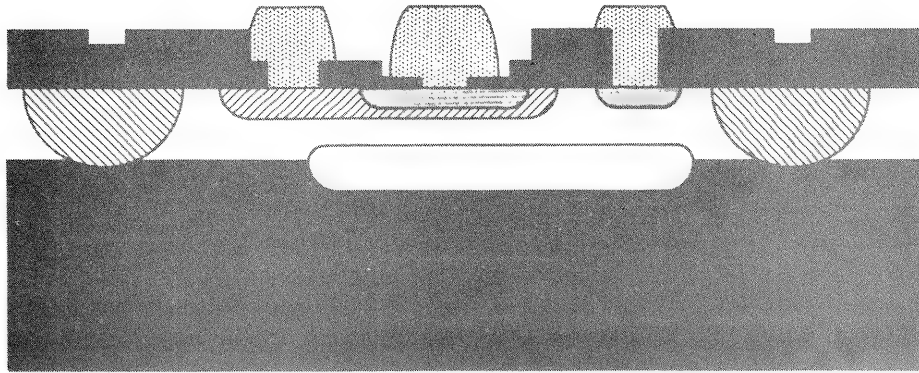
(a)
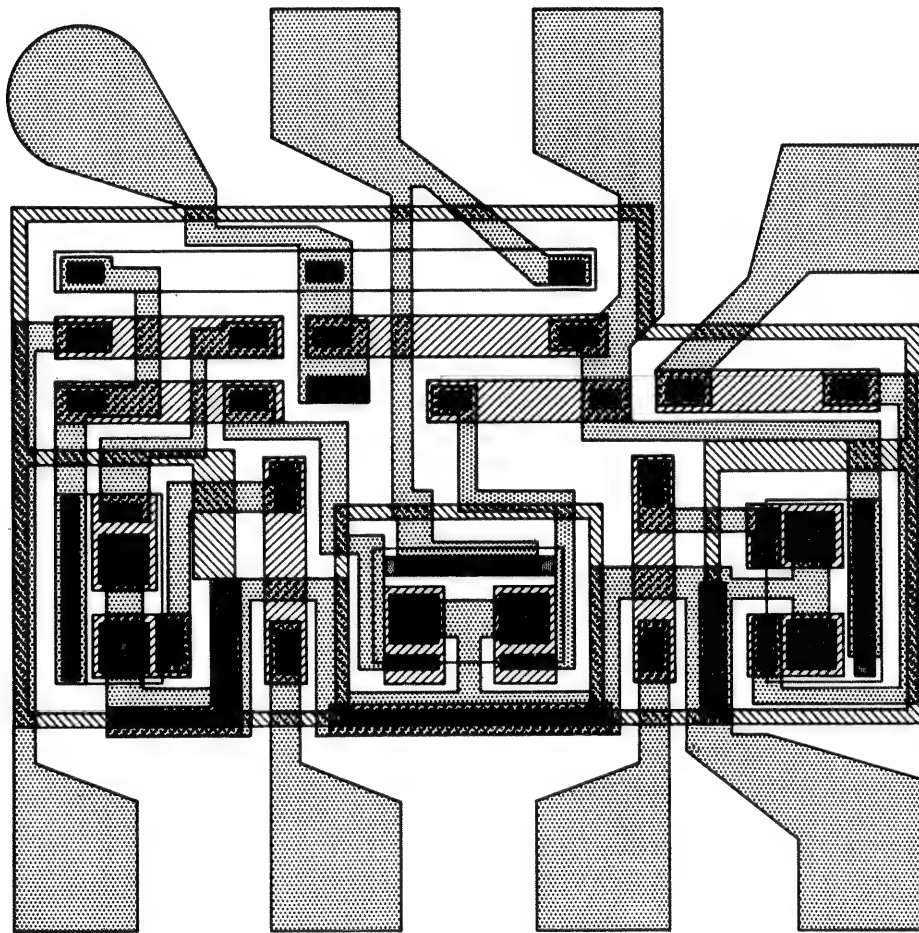
(b)

Fig. 7 Metal Intraconnections

is then cut up into individual integrated circuits using a technique very similar to the cutting of glass. A diamond scribe is used to make fine scratches on the surface of the wafer between circuits. The wafer is mechanically separated along these lines into uniform, square dice. The reject dice are then sorted out, and the good dice thoroughly cleaned and inspected for defects under high-power microscopes before expensive hand labor is incurred.
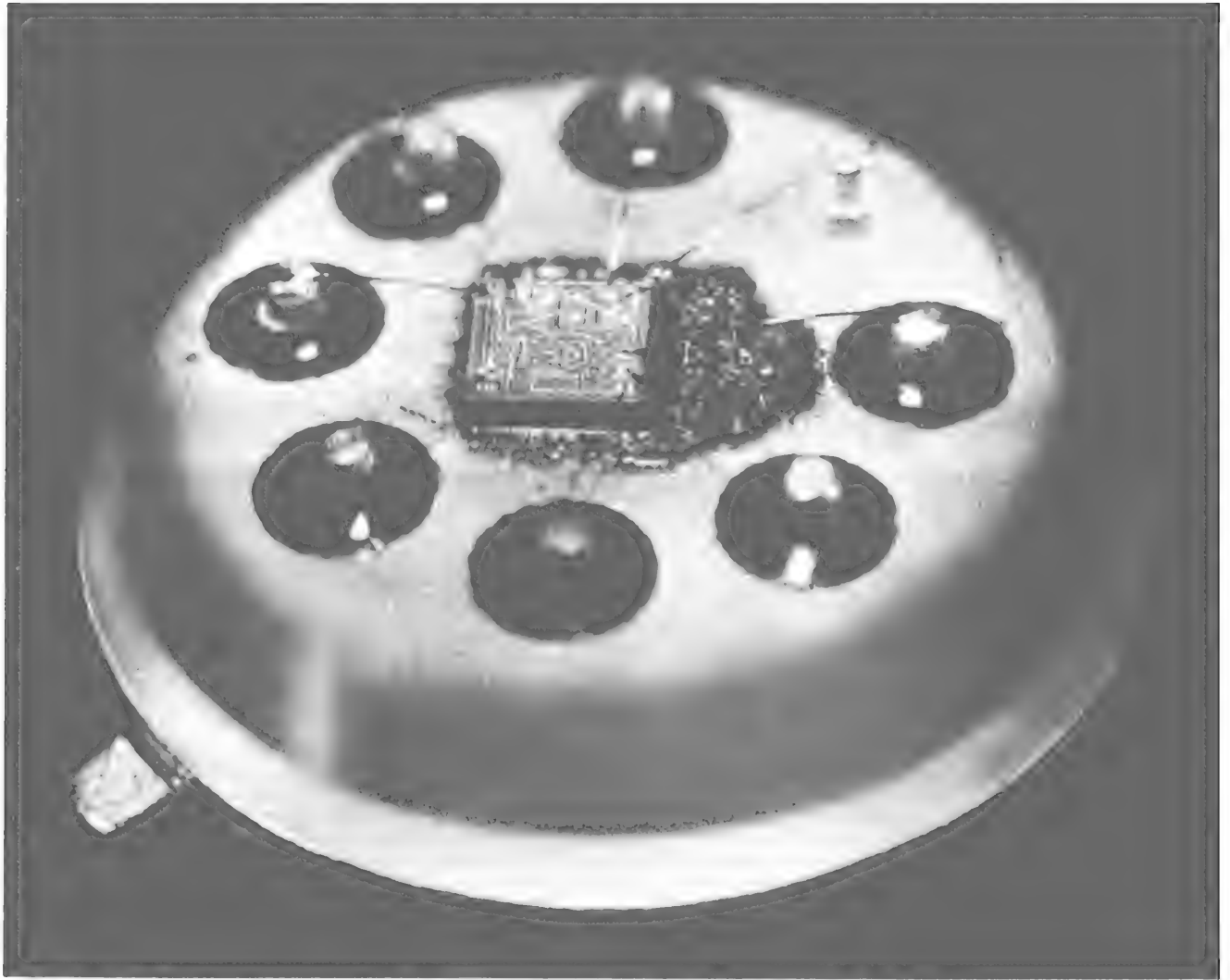
Fig. 8 Lead Attachments

Following visual inspection, the die is soldered to the center of a header using a high-temperature alloy preform. Fine wires are attached to each bonding pad and spot-welded to the external leads (Figure 8). A final optical inspection is then conducted to ensure that the die has not been damaged in any manner up to this time. After passing this inspection, the mounted device is thoroughly cleaned and a cap is welded to the header. After final seal, each microcircuit is subjected to mechanical shock tests, temperature cycling, centrifuge acceleration tests, and 100% electrical testing over the temperature range of the particular device. Even after the final electrical factory tests, devices are continually sampled by Quality Control to confirm that they meet rigid specifications. Finished units are then marked and packaged for shipment to customers.

The integrated circuit components in production today are limited both in type and in range of value. These limitations have been more troublesome with linear than with digital integrated circuits since conventional linear designs utilize a greater variety of parts. Because of the close control of components, large resistances, circuit adjustments, and complementary transistors generally required, serious problems have arisen in adapting discrete component designs to monolithic construction.

With monolithic construction, it is impractical to control the absolute value of resistors to closer than 20-30% of nominal, and, in addition, the temperature coefficient of diffused silicon resistors is quite high (0.2%/°C). Large resistors require excessive surface area and make the integrated circuit difficult to manufacture. The same is true for capacitors. Circuit adjustments, although possible with thin-film resistors, are time-consuming, subject to irreversible error, and therefore costly. Finally, the manufacture of complementary transistors on a single silicon substrate increases the number of processing steps as well as the degree of control that must be exercised. Even then, it is practically impossible to optimize the characteristics of both the NPN and the PNP transistors.

In many cases, attempts have been made to develop new technology in order to integrate existing designs. This approach has met with varying degrees of success, but has generally resulted in circuits that are difficult to produce in large volume. To realize a practical microcircuit with any certainty and within a reasonable period of time, it is necessary to use existing production technology. Fortunately, with some specialized circuit design techniques, performance can be achieved with present technology which, in many cases, is equal to or better than that obtainable with discrete-component circuits. These techniques make it possible to avoid the restrictions imposed by the limited types of components, poor tolerances and the restricted range of component values. Furthermore, they make use of the inherent advantages of integrated circuit components: close matching of active and passive devices over a wide temperature range, excellent thermal coupling throughout the circuit, the economy of using a large number of active devices, the freedom of selection of active device geometries, and the availability of devices which have no exact discrete-element counterpart.

The techniques discussed in this chapter utilize elements that can be easily constructed in monolithic form to avoid processing difficulties or substantial yield losses in manufacturing. The methods shown eliminate the need for the wide variety of components and tight component tolerances usually required with discrete designs by substituting parts that can be made simply and that make use of the special characteristics obtainable with monolithic construction. This is of particular practical significance in that circuit design is a non-recurring cost for a particular microcircuit, while restrictive component tolerances or extra processing steps represent a continuing expense in manufacturing. In this section, a broad indication of what can be done with integrated circuit design techniques will be described, rather than specific details. Examples of practical circuits will be given to illustrate important points.

BIASING CIRCUITS

One of the basic problems encountered in integrated circuits is bias stabilization of a common-

emitter amplifier. Conventional discrete design methods usually require substantial DC degeneration and a bypass capacitor to reduce degeneration at the frequencies to be amplified. With integrated circuits, however, the required bypass capacitors are much too large to be practical. This problem has been overcome in the past by using some sort of differential or emitter-coupled amplifier connection. Such a solution has been adequate in many instances, but suffers from a lack of versatility.

The close matching of components and tight thermal coupling obtained in integrated circuits permit much more radical solutions. An example is given in Figure 1(a). A current source can be implemented by imposing the emitter-base voltage of a diode-connected transistor operating at one collector current across the emitter-base junction of a second transistor. If the two transistors are identical, their collector currents will be equal; hence, the operating current of the current source can be determined from resistor R_1 and the supply voltage. Experiment has shown that this biasing scheme is stable over a wide temperature range, giving collector current matches between the biasing and operating devices typically better than five percent, even for power dissipations in Q_2 above 100 mW.

A third and more subtle variation is given in Figure 1(c). If R_3 and R_4 as well as Q_1 and Q_2 are identical, the collector currents of the two transistors will be equal since their bases are driven from a common voltage point through equal resistances. The collector current of Q_1 will be given by:

$$I_{C1} = \frac{V^+ - V_{BE}}{R_1} - \left(2 + \frac{R_3}{R_1}\right) I_B , \qquad (1)$$

where a single V_{BE} and I_B term is used since both transistors are identical. For $V_{BE} << V^+$ and $I_B << I_C$, Eq. (1) becomes

$$I_{C1} = I_{C2} \approx \frac{V^+}{R_1} . \qquad (2)$$

If $R_2 = 1/2\ R_1$, the output voltage is

$$E_0 \approx \frac{V^+}{2} , \qquad (3)$$

which means that the amplifier is biased at its optimum operating point (one-half the supply voltage), independent of supply voltage or temperature, and dependent only on how well the parts within the integrated circuit match.

(a) CURRENT SOURCE
(b) TRANSFORMER COUPLED AMPLIFIER
(c) RC-COUPLED AMPLIFIER
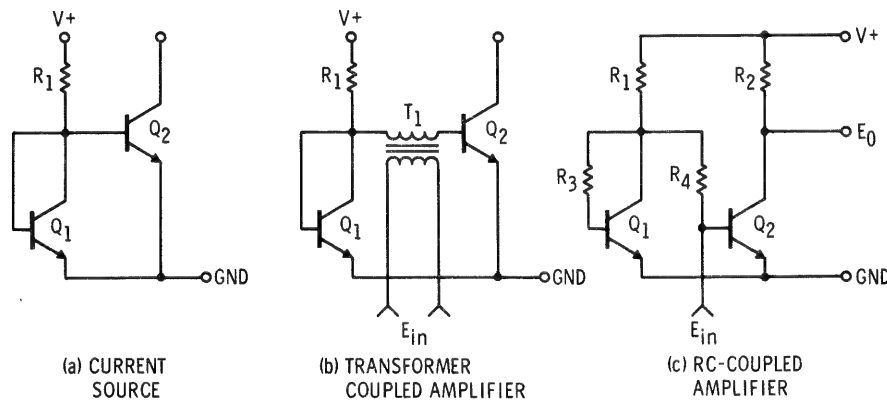
Fig. 1 Biasing Techniques Applicable to Integrated Circuitry which Take Advantage of Precise Matching and Close Thermal Coupling.

An extension of this idea is shown in Figure 1(b). A transformer with a low resistance secondary can be inserted between the biasing transistor and the second transistor. Then Q_2 is stably biased as an amplifier without requiring bypass elements, and the transformer secondary is coupled to the amplifier without disturbing the bias conditions.

A simple amplifier using the biasing of Figure 1(c) is illustrated in Figure 2. Emitter degeneration resistors R_5 and R_6 are employed to control gain and raise input impedence without disturbing the balanced biasing. A cascade connection of Q_2 with Q_3 reduces input capacitance, while the emitter-follower gives a low output impedance.
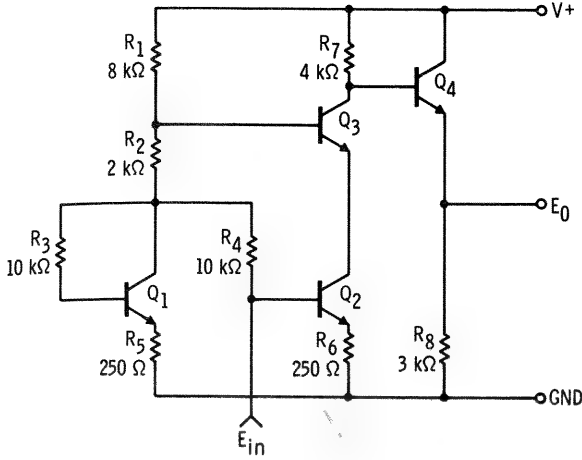
Fig. 2 General Purpose Wideband Amplifier Using Balanced Biasing Techniques.

Another biasing circuit that makes use of the well-matched characteristics of integrated components is shown in Figure 3. This is an emitter-coupled RF/IF amplifier intended for use with external L-C tuned circuits and requires neither dual supply voltages nor large-value bypass capacitors.
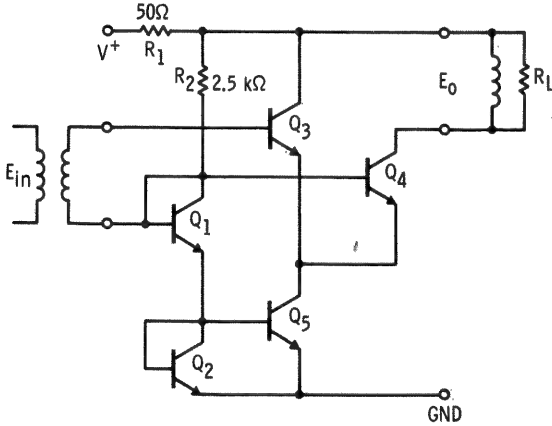
Fig. 3 RF/IF Amplifier Using Balanced Biasing.

The biasing is easily understood if it is again assumed that all parts within the circuit are well matched and the transistor current gains are high enough that the base currents can be neglected. It is also assumed that the transformer windings, particularly in the input circuit, have a low enough DC resistance to be neglected.

The collector current of the biasing diode-connected transistor, Q_2, is

$$I_{C2} = \frac{V^+ - 2V_{BE}}{R_2 + 2R_1} \approx \frac{V^+}{R_2},\qquad (4)$$

since $R_2 >> R_1$ and $V^+ >> 2V_{BE}$.

All of the transistors are assumed to be identical; hence, the collector current of Q_5 is equal to that of Q_2 because their bases are fed from a common voltage point. The collector current of Q_5 splits evenly between Q_3 and Q_4 with zero input signal. When the amplifier is driven into limiting, this current is alternately switched between Q_3 and Q_4. To prevent saturation of Q_4 when the amplifier is driven with a large signal, the load resistance must be low enough that current limiting occurs before the output voltage drops to $2V_{BE}$. Thus, for a transformer-coupled output,

$$R_L \le \frac{2(V^+ - 2V_{BE})}{I_{C2}}$$

$$\le 2R_2 \qquad (5)$$

In addition to overcoming problems encountered in integrated circuits, this circuit provides improved performance by giving first, essentially unilateral operation, which increases the available power gain and simplifies tuning, and second, a symmetrical limiting characteristic, which reduces the detuning, phase error, and blocking that occur when conventional amplifiers saturate.

It can be seen from the above that the matching characteristics of a monolithic circuit have made possible biasing methods that are superior to those attainable with discrete designs. Excellent biasing stability is achieved over a wide temperature range without wasting any of the supply voltage across bias stabilization networks. In addition, no bypass capacitors are required.

THE EFFECT OF MISMATCHES ON BALANCED BIASING

The assumption that the two transistors in Figure 1(c) were identical is, of course, not entirely true in a practical microcircuit. This deviation from reality will now be considered.

In Eq. (1) of the text, the mismatches in emitter-base voltage and base currents are third-order effects since the absolute values of V_{BE} and I_B are second-order terms. Therefore, Eq. (1) is assumed to hold in this analysis. Equation (2), however, is strongly affected by the match between Q_1 and Q_2. This influence will be reflected by the equation

$$I_{C2} = I_{C1} + \Delta I_{C2} \qquad (6)$$

where ΔI_{C2} is the change in collector current of Q_2 due to non-equal emitter-base voltages and base currents in Q_1 and Q_2.

Both mismatch terms above can be combined to give

$$\Delta V_{IN} = \Delta V_{BE} + R_4 \Delta I_B \,, \qquad (7)$$

where ΔV_{BE} and ΔI_B are, respectively, the emitter-base voltage difference and base current difference of the two devices operating at equal collector currents. (These terms are chosen because they are important in the performance of DC amplifiers, and data on the parameters—both for transistor pairs and for complete integrated amplifiers—is common). This ΔV_{IN} will have the same effect on bias stability as an equal DC input voltage applied in series with R_4 to an ideally balanced amplifier.

In order to determine the relationship between ΔV_{IN} and ΔI_{C2}, it becomes necessary to introduce the familiar expressions:[1]

$$I_C = I_S \, exp \left(\frac{qV_{BE}}{kT} \right) \qquad (8)$$

and

$$I_B = I_S \, exp \left(\frac{qV_{BE}}{mkT} \right) \qquad (9)$$

where I_S is the saturation current, q is the charge of an electron, k is Boltzmann's constant, T is the absolute temperature and m is a constant with a value between one and two. These expressions hold up to high currents, where emitter contact and base spreading resistances become important, and down to low currents, where collector leakage currents cause inaccuracy. They are valid, within a percent or so, for operation over at least six decades of current with well-made silicon transistors.

Differentiation of Eq. (8) gives

$$\frac{\Delta I_C}{\Delta V_{BE}} = \frac{qI_C}{kT} \qquad (10)$$

Similarly, for Eq. (9),

$$\frac{\Delta I_B}{\Delta V_{BE}} = \frac{qI_B}{mkT} \qquad (11)$$

and hence

$$R_{IN} = \frac{mkT}{qI_B} \qquad (12)$$

From this, with reference to Figure 1(c), it can be shown that

$$\Delta I_{C2} = \left(\frac{R_{IN} \Delta V_{IN}}{R_{IN} + R_4} \right) \left(\frac{qI_{C2}}{kT} \right)$$

$$= \frac{m(\Delta V_{BE} + R_4 \Delta I_B)}{\frac{mkT}{q} + R_4 I_{B2}} I_{C2} \qquad (13)$$

where m is physically significant as the ratio of the AC current gain to the DC current gain at the operating current level (typically 1.6 for low-current operation and 1.2 for operation approaching the current gain peak).

Hence, Eq. (13) can be written

$$\Delta I_{C2} \cong \frac{m(\Delta V_{BE} + R_4 \Delta I_B)}{\frac{mkT}{q} + R_4 I_B} I_{C1} \qquad (14)$$

For $R_{in} << R_4$, this becomes

$$\frac{\Delta I_{C2}}{I_{C1}} = \frac{m\Delta I_B}{I_B} = \Delta h_{fe} \qquad (15)$$

where

$$\Delta h_{fe} = \frac{h_{fe2} - 1}{h_{fe1}} \qquad (16)$$

For $R_{IN} >> R_4$, the result is

$$\frac{\Delta I_{C2}}{\Delta I_{C1}} = \frac{q\Delta V_{BE}}{kT} \qquad (17)$$

Since R_{IN} varies drastically over the $-55°C$ to $+125°C$ temperature range commonly expected

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[1]C.T. Sah, "Effect of Surface Recombination and Channel on P-N Junction and Transistor Characteristics," *IRE Trans. on Electron Devices*, Vol. ED-9, pp. 94-108, January 1962.

of integrated circuits, Eq. (15) can be taken to represent the low temperature extreme and Eq. (17) the high temperature extreme. Therefore, a more-than-worst-case solution for full temperature range operation is

$$\left|\frac{\Delta I_{C2}}{I_{C1}}\right| \le \left|\frac{q\Delta V_{BE}}{kT}\right| + \left|\Delta h_{fe}\right| \qquad (18)$$

To give some idea of the results obtainable, the first term in Eq. (18) is typically less than 0.02, while the second term is typically less than 0.07 for operation over the full temperature range.

CONSTANT CURRENT SOURCE

With integrated circuits, the formation of current sources in the microampere current range can be difficult because of the relatively large resistance values usually required. The circuit shown in Figure 4 makes possible a current source with an output in the tens of microamperes using resistances of only a few kilohms. It makes use of the predictable difference in emitter-base voltage of two transistors operating at different collector currents. Solving Eq. (8) for V_{BE} gives

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \qquad (19)$$

This expression can be used to find the emitter-base voltage difference between two transistors:

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} \ln\left(\frac{I_{C2}}{I_{S2}}\right)$$

$$= \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) + \frac{kT}{q} \ln\left(\frac{I_{S2}}{I_{S1}}\right) \qquad (20)$$

For equal collector currents, Eq. (20) becomes

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_{S2}}{I_{S1}}\right) \qquad (21)$$

Considerable testing has shown that for adjacent, identical integrated circuit transistors, this term is typically less than 0.5 mV. It is also relatively independent of the current level, as might be expected since I_S should be a constant. Hence, the emitter-base voltage differential between adjacent integrated circuit transistors operating at different collector currents is given by

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) \qquad (22)$$

within a fraction of a millivolt.

With the circuit in Figure 4, a relatively large collector current is passed through the diode-connected biasing transistor, Q_1. The emitter-base voltage of this transistor is used to bias the current-source transistor, Q_2. If, for simplicity, the base currents of the transistors are neglected, the resistance required to determine the current-source current is given by

$$R_2 = \frac{\Delta V_{BE}}{I_{C2}} = \frac{kT}{qI_{C2}} \ln\left(\frac{I_{C1}}{I_{C2}}\right) \qquad (23)$$

For the circuit in Figure 4, the resistance is

$$R_2 = \frac{kT}{qI_{C2}} \ln\left(\frac{V^+ - V_{BE}}{R_1 I_{C2}}\right) \qquad (24)$$

The effect of non-zero base currents can be easily determined in that they both subtract directly from I_{C1} and I_{B2} subtracts from I_{C2}.

One interesting feature of this circuit is that, for $V^+ >> V_{BE}$ and $I_{C1} >> I_{C2}$, the output current will vary roughly as the logarithm of the supply voltage. Therefore, if the current source is used to bias the input stage of an operational amplifier, the operating collector current and voltage gain of the input stage will vary little over an extremely wide range of supply voltages.

From Eq. (22), it can be seen that the emitter-base voltage differential is a linear function of absolute temperature. It might be expected, therefore, that the output current of the current source would vary in a similar manner. Such is the case, as illustrated in Figure 4. The plot is for $I_{C1} \approx 50 I_{C2}$ with both zero-temperature coefficient resistors and high-resistivity diffused resistors (bulk impurity concentration less than 10^{17} atoms/c.c.). It is notable that diffused resistors provide overcompensation for this characteristic.

The same principle used with the current source can be employed to make a Darlington-connected amplifier stage insensitive to high temperature leakages, and to stabilize it over a wide temperature range. This is shown in Figure 5. The more conventional method would be to connect a resistor
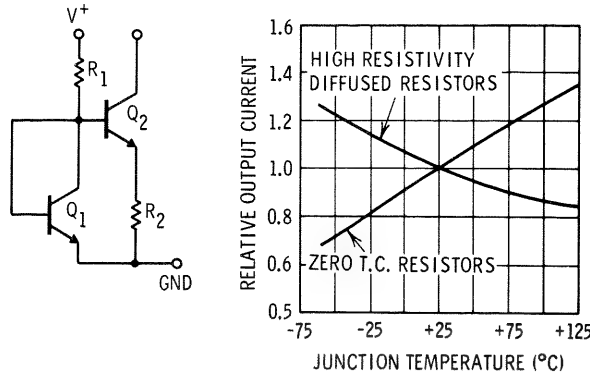
Fig. 4 A Current Source for Generating Very
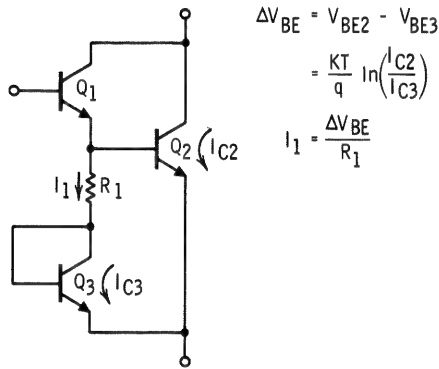Small Currents Using Moderage
Value Resistors.

$$\Delta V_{BE} = V_{BE2} - V_{BE3}$$

$$= \frac{KT}{q} \ln\left(\frac{I_{C2}}{I_{C3}}\right)$$

$$I_1 = \frac{\Delta V_{BE}}{R_1}$$

Fig. 5 Schematic Illustrating Principle of the
Modified Dalington Connection.

across the emitter-base junction of Q_2. The re-
quired value of resistance, however, would be
large. Further, since the emitter-base voltage has a
negative temperature coefficient, and the resistors
a positive temperature coefficient, the bleed cur-
rent would become small at high temperatures
(where it is needed most) and large at low tempera-
tures (where it is undesirable). With the scheme in
Figure 5, however, resistance values more than an
order of magnitude lower can be used and the
bleed current has a strong positive temperature
coefficient, as desired.

LEVEL SHIFTING

In linear integrated circuits, some form of DC
level shifting is often required in the signal path.
With discrete designs, this can be accomplished
by using complementary transistors or, perhaps,
zener diodes. Both these approaches, however,
have their limitations with respect to integrated
circuits.

A circuit which avoids many of the previous
problems is shown in Figure 6. It uses only NPN
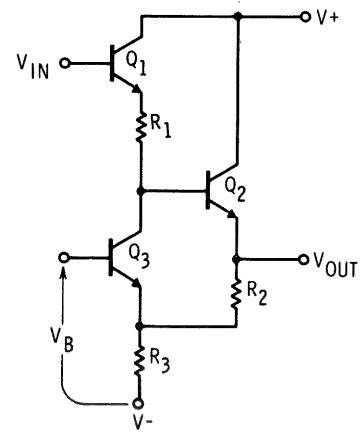
Fig. 6 Circuit for Providing DC Level Shifting
as well as Signal Gain.

transistors, and its operation can be made essen-
tially dependent only on resistor ratios. Tran-
sistor Q_1 serves as an input buffer, and level shifting
is accomplished by the voltage drop across R_1 due
to the collector current of Q_3. Feedback from the
output, through R_2, is used to increase this voltage
drop for negative-going output swings and de-
crease it for positive-going signals. Properly de-
signed, the stage will provide substantial voltage
gain, high input impedance, low output imped-
ance, and an output swing nearly equal to the
supply voltages, in addition to the desired DC level
shift.

Assuming that $V^+ + V^- >> V_{BE}$ and that the gain
is less than about 5, the voltage gain of the circuit
can be obtained from

$$\Delta V_{OUT} = \Delta V_{IN} - R_1 \Delta I_{C3}, \tag{25}$$

where

$$\Delta I_{C3} = \frac{\Delta V_{OUT}}{R_2} \tag{26}$$

Hence,

$$\Delta V_{OUT} = \Delta V_{IN} + \frac{R_1}{R_2} \Delta V_{OUT} \tag{27}$$

and

$$A_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{1 - \frac{R_1}{R_2}} \tag{28}$$

The output impedance can be approximated by

14

$$R_{OUT} = \frac{R_1 A_V}{h_{FE2}} \qquad (29)$$

As the input impedance is usually negative, it is necessary that the level-shifting stage be driven from a low impedance source for stability. Sufficient conditions for stability are

$$R_S << \frac{h_{FE1} R_2}{A_V} \qquad (30)$$

A rather ingenious complementary transistor structure for level-shifting can be produced with no complication of the normal NPN processing techniques. The lateral PNP shown in Figure 7

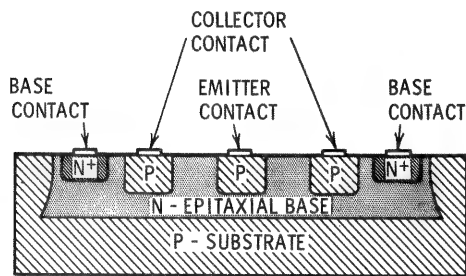Fig. 7 Cross-Sectional View of Lateral PNP Transistor.

is made using what is usually an NPN base diffusion for an emitter; this is surrounded by a second base diffusion which serves as a collector. The normal NPN collector region is then the PNP base. However, the device has a low current gain (approximately 2), a parasitic current gain to the integrated circuit substrate, and limited frequency response. These limitations can be largely overcome with additional process controls and processing steps, but then the device loses much of its attractiveness. Nonetheless, there are undoubtedly a large number of applications which can use the surface PNP, although not on a one-to-one basis with discrete transistors.

PINCH RESISTORS

A potentially useful element that has received much mention but little actual application in integrated circuits is the pinch resistor. This is an ordinary diffused (base) resistor, the cross-sectional area of which has been effectively reduced by making an emitter diffusion on top of it (see Figure 8(a)). The emitter diffusion raises the sheet resistivity from the usual 100 or $200\Omega/sq$ to $10k\Omega/sq$ or higher, thereby permitting rather large resistors to be made in a relatively small area. The pinch
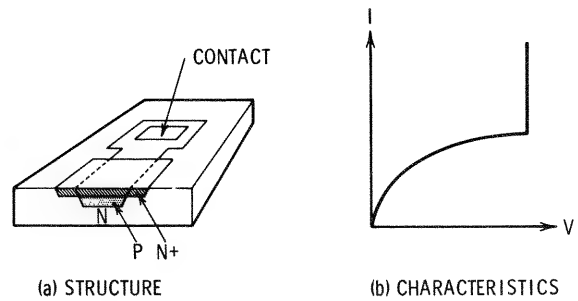
Fig. 8 Pinch Resistors.

resistor, however, has several limiting characteristics. As can be seen from Figure 8(b), it is linear only for small voltage drops, and it has a low breakdown voltage (5 to $10V$). Neither the linear nor the nonlinear portions of the characteristics can be controlled well, and the resistance at the origin can easily vary over a 4:1 range in a normal production situation. In addition, the resistor has a very strong positive temperature coefficient, changing by about 3:1 over the $-55°C$ to $+125°C$ temperature range.

On the other hand, there is a strong correlation between the pinch resistor values and transistor current gains obtained in manufacture. Within a given process, the sheet resistivity is roughly proportional to the current gains near the current-gain peak (where surface effects have little influence on the current gain). Further, the resistors tend to track with the current gains over temperature. The matching of identical pinch resistors is also nearly as good as base resistors and substantially better than transistor current gains, since the current gains are affected by unpredictable surface phenomenon whereas the pinch resistors are not.

In Figure 2, both R_3 and R_4 have small voltage drops across them; to obtain the highest possible input impedance consistent with satisfactory bias stability, it would be advantageous to have these resistor values proportional to the transistor current gain. The characteristics of pinch resistors can be employed effectively here.

Another application for pinch resistors is the preamplifier shown in Figure 9—originally designed as part of a hearing aid amplifier. With hearing aids, the maximum supply voltage is $1.55V$, and accordingly, the voltage sensitivity and low breakdown of pinch resistors are of little concern. Power drain, however, is a problem, and large resistances are needed. In this circuit, only matching of the pinch resistors (R_1, R_2, and R_3) is required for proper operation. The fact that the
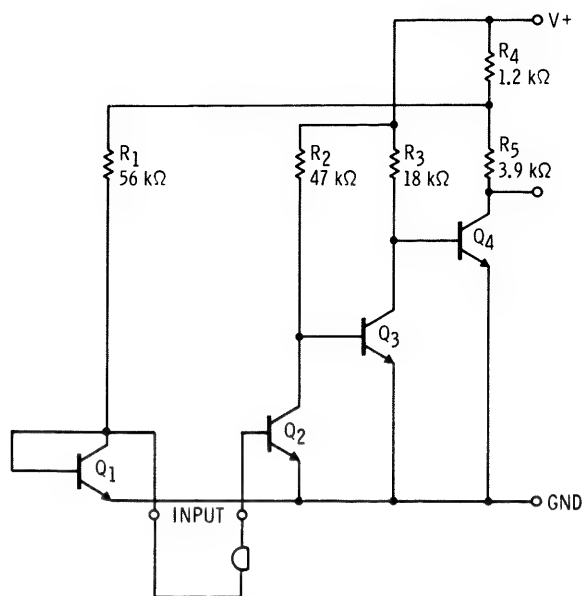
Fig. 9 A Low-Voltage, High-Gain Microphone Preamplifier Illustrating the Use of Pinch Resistors.

pinch resistors correlate with current gain makes the circuit far less sensitive to current gain variations: the pinch resistors and current gains can be varied simultaneously over a greater than 7:1 range without any noticeable degradation of performance.

The above examples show that even though pinch resistors have extremely poor characteristics by discrete component standards, certain characteristics — namely good matching, a correlation between resistor values and current gain, and high sheet resistivities — make them extremely useful elements in circuit design. The pinch resistors can actually function better than precision resistors in certain applications in that they can be used to help compensate for production variations in current gain and the change in gain with temperature.

OPERATIONAL AMPLIFIERS

The operational amplifier is one of the most versatile devices available to the electronics industry today. In addition to performing the traditional computing functions of addition, subtraction, integration, and differentiation, it is widely used in such diverse applications as signal conditioning, analog instrumentation, active filters, servo systems, process control, nonlinear function generators, regulators, and many other routine functions.

The versatility of the operational amplifier results from the use of a large amount of negative feedback around the device. The characteristics of the amplifier in a given application with feedback are determined by the external feedback elements alone, over which the designer can exercise the degree of control required by his application. He can, therefore, use a single amplifier in many different functional circuits.

Now that high performance operational amplifiers (such as the Fairchild μA709C) have become available at costs below a few dollars, more and more engineers will find it economical to use these devices to solve their circuit problems. It is the purpose of this chapter to provide a brief review of operational amplifier fundamentals for the benefit of those engineers who are making their first venture into the field. Detailed discussions and derivations can be found in many textbooks and journals, and in the application notes published by several of the leading operational amplifier manufacturers, some of which are listed in the references at the end of the chapter.

THE IDEAL OPERATIONAL AMPLIFIER

The most versatile operational amplifier has a differential input and a single-ended output (Figure 1). The circuit amplifies the difference between the voltages applied to its two input terminals; a
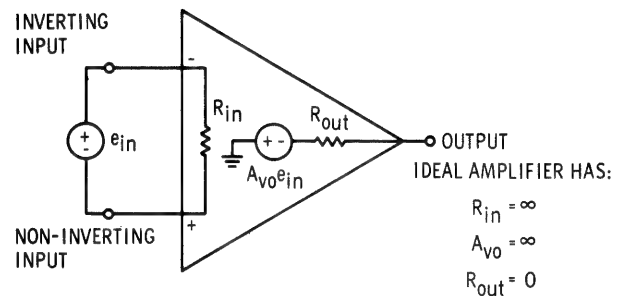
Fig. 1 Equivalent Circuit for Basic Operational Amplifier.

positive voltage at the inverting input (or "summing point") produces a negative output, while one at the non-inverting input produces a positive output.

The ideal operational amplifier is characterized by:

1) infinite voltage gain
2) infinite input resistance
3) zero output resistance
4) infinite bandwidth
5) zero offset

Two very powerful tools for circuit analysis and design are implied by the ideal properties listed above. As a result of infinite input resistance

NO CURRENT FLOWS INTO EITHER INPUT TERMINAL

Because of the infinite gain, when negative feedback is applied around the amplifier

THE DIFFERENTIAL INPUT VOLTAGE IS ZERO.

Proper use of these two simple, basic properties makes possible rapid, first-order analysis of any operational amplifier circuit, regardless of complexity.

INVERTING AMPLIFIER

Figure 2 shows the connection for a basic feedback circuit, the inverting amplifier. Calculation of
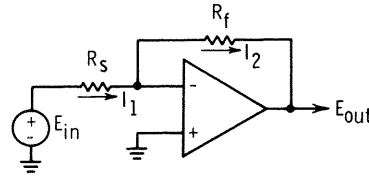

Fig. 2 Inverting Amplifier.

the voltage gain proceeds very simply: since the differential input voltage is zero, the potential at the inverting input equals that of the non-inverting input (ground), and therefore the two currents are

$$I_1 = \frac{E_{in}}{R_S} \qquad (1)$$

$$I_2 = -\frac{E_{out}}{R_f} \qquad (2)$$

Since no current flows into the amplifier, $I_1 = I_2$, and thus the voltage gain is

$$\frac{E_{out}}{E_{in}} = -\frac{R_f}{R_S} \qquad (3)$$

The input impedance is R_S, the output impedance is zero, and any value of gain can be obtained by proper choice of the feedback elements.

Because of the virtual ground at the summing point, any number of input voltages may be applied to the amplifier and summed at the output without interaction between the sources. Each input sees its respective resistor as the input resistance, and the current in the feedback resistor is the algebraic sum of the current from each input source.

The operational amplifier may also be used as a current source. This is accomplished by putting the load in the feedback loop (i.e., $R_L = R_f$ in Figure 2). The current through the load is given by Eq. (1) and is completely independent of the load impedance.

NON-INVERTING AMPLIFIER

Another basic feedback circuit is given in Figure 3; this is the non-inverting amplifier, or potentiometric connection. Since no current flows into the amplifier inputs, R_f and R_S form a simple voltage
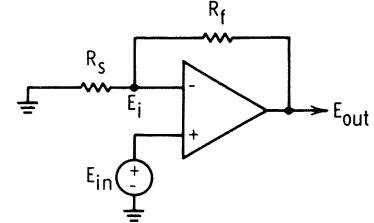

Fig. 3 Noninverting Amplifier.

divider, and the voltage at the inverting input is equal to

$$E_i = \frac{R_S}{R_f + R_S} E_{out} \qquad (4)$$

This voltage must be equal to the input voltage because of the infinite voltage gain, and therefore

$$\frac{E_{out}}{E_{in}} = 1 + \frac{R_f}{R_S} \qquad (5)$$

In this case, the input impedance is infinite, the output impedance is zero, and only voltage gains above unity are possible.

A unity-gain buffer, or voltage-follower, results when the source resistor (R_S) is removed; any value of R_f can be used in the ideal case since no current flows in the feedback path.

DIFFERENTIAL AMPLIFIER

Figure 4 shows a circuit that uses both inputs to the operational amplifier. Operation is best seen
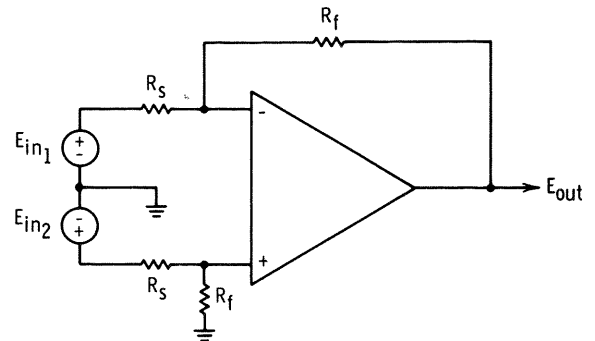

Fig. 4 Differential Amplifier.

by considering each input separately. The output voltage due to the signal on the inverting input is

$$E_{out_1} = -\frac{R_f}{R_S} E_{in_1} \qquad (6)$$

and the output from the non-inverting input is

$$E_{out_2} = \left(1 + \frac{R_f}{R_S}\right) \left(\frac{R_f}{R_f + R_S}\right) E_{in_2} \qquad (7)$$

The voltage divider at the non-inverting input has

been included to make the over-all gains from both signals equal, so the total output voltage will be

$$E_{out} = \frac{R_f}{R_S} \left(E_{in_2} - E_{in_1} \right) \qquad (8)$$

FEEDBACK ELEMENTS

Resistance feedback elements have been shown so far, but in general, any form of complex or non-linear feedback may be used. The over-all transfer function may be derived similarly, with appropriate changes being made to include the reactive or non-linear relationships.

A capacitor used as the feedback element, for example, will integrate the input voltage, since the current through the feedback loop charges the capacitor and is stored there as a voltage at the output. A differentiator can be obtained by reversing the feedback elements, with the capacitor as the source and the resistor as the feedback element. A diode or transistor in the feedback path yields a logarithmic output. The various possibilities and combinations are too vast to be mentioned here, but several practical examples are given in the chapter on applications.

SOURCES OF ERROR

Unfortunately, no manufacturer has yet produced an ideal operational amplifier. In this section, the imperfections that cause practical amplifiers to depart from the ideal will be considered, along with their effect upon circuit performance.

Offset The most significant limitation affecting accuracy in DC amplifiers is offset and its variations with temperature, time, supply voltage, and common mode voltage. Although the ideal operational amplifier has exactly zero output for zero input, this is never quite achieved in practice because of the small, unavoidable mismatch that exists between components in a practical circuit. The output, therefore, will have a DC offset when there is no input signal. Offset is generally referred to the input and, being independent of the amplifier gain, can be directly compared with the input signal.

Figure 5 gives an equivalent circuit for the operational amplifier showing the principal sources of offset. The input offset voltage (V_{OS}) is defined as the voltage that must be applied between the
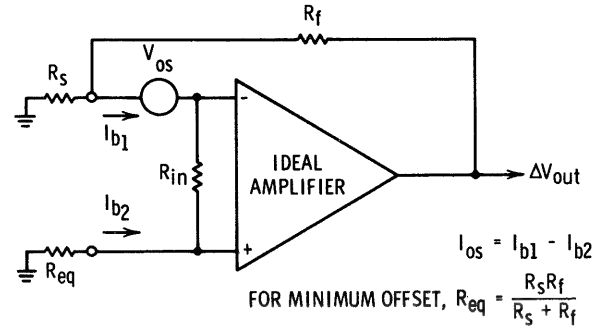

Fig. 5 Equivalent Circuit Showing Sources of Offset.

input terminals to obtain zero output. Input bias current is the average of the two currents

$$\left(\frac{I_{b1} + I_{b2}}{2} \right)$$

that flow into the inputs when the output is nulled, and input offset current (I_{os}) is the difference of the two input currents under the same conditions. Both voltage and current offset (which have random and independent polarities), together with the impedance levels of the external components, must be considered when predicting the performance of an operational amplifier circuit.

The total output offset voltage developed by the general circuit of Figure 5 is

$$\Delta V_{OUT} = \left(1 + \frac{R_f}{R_S} \right) V_{OS} + I_{b_1} R_f - I_{b_2} R_{eq} \left(1 + \frac{R_f}{R_S} \right) \qquad (9)$$

Since the two bias currents in a well-matched differential amplifier are approximately equal, their effect upon offset can be cancelled by making the impedance to ground equal at both inputs. Thus, by making

$$R_{eq} = \frac{R_s R_f}{R_s + R_f}, \text{ the output offset becomes}$$

$$\Delta V_{OUT} = \left(1 + \frac{R_f}{R_S} \right) V_{OS} + R_f I_{os} \qquad (10)$$

It will be assumed in the following discussions that the resistances have been equalized; however, in those applications where it is not possible to do this, the contribution of the input bias currents must be considered, as shown in Eq. (9).

It should be noted (from Eq. 10) that the offset produced at the output is independent of whether the amplifier is being operated in the inverting or non-inverting connection. Referred to the input signal, this means that the offset error will be different for the two configurations, even though the voltage gains are equal. For the inverting amplifier, the input-referred offset is

$$\Delta V_{IN} = \left(1 + \frac{R_S}{R_f}\right) V_{OS} + R_S I_{OS} \tag{11}$$

while for the non-inverting amplifier it becomes

$$\Delta V_{in} = V_{OS} + I_{OS} \left(\frac{R_S R_f}{R_f + R_S}\right) \tag{12}$$

A fixed input offset is not usually a great problem because biasing circuits can be added to cancel it out in critical applications. However, drift of offset with temperature, time, etc., introduces a basic input error because this change cannot be distinguished from the input signal. Drift with temperature is generally specified as an average over a specified temperature range. This is done because a fairly large change in temperature is necessary to make accurate drift readings, and because it is uneconomical to record data and compute drifts at a large number of temperature points. Drift specifications, therefore, should be interpreted as a maximum change in offset over the temperature range, and do not imply that the temperature coefficient is linear over this range.

By virtue of their differential design, operational amplifiers are relatively unaffected by power supply regulation and ripple. The ability of the amplifier to discriminate against supply variations is termed the supply voltage rejection ratio, and is defined as the ratio of the change in input offset voltage to the change in supply voltage. It is usually specified as $\mu V/V$ or $\mu V/\%$. This factor must be considered in critical applications where the supplies may not be well-regulated.

A basic property of the differential amplifier is its ability to amplify signals applied between its input terminals, while rejecting those common to both inputs. When the gains from the inputs are not exactly equal, an output will be produced for a common mode input voltage. The ratio of the common mode voltage to this error (which is referred to the input as a change in offset) is the common mode rejection ratio, and is generally specified in dB. The input voltage range specification defines the maximum amplitude of common mode voltage that may be applied to the amplifier without exceeding the common mode rejection ratio

figure. Rejection ratios on the order of 70-100 dB are commonly obtained with practical amplifiers. In the circuit of Figure 4, it is necessary that the R_S and R_f resistors at each input be very closely matched if the inherent rejection capability of the amplifier is to be utilized. If the resistors are balanced to a fraction (δ) of nominal value, and it is assumed that the worst case combination of mismatch exists between the resistors, the output error caused by a common mode input (V_{CM}) is given by

$$\Delta V_{OUT} = V_{CM} \frac{4\delta}{\left(1 + \frac{R_S}{R_f}\right)} \tag{13}$$

where R_S and R_f are nominal values, and

$$\delta << 1.$$

Therefore, for a given change of input offset (ΔV_{OS}), the resistors must be matched to an accuracy of

$$\delta = \frac{\Delta V_{OS}}{V_{CM}} \left(\frac{1 + \frac{R_f}{R_S}}{4}\right) \tag{14}$$

If the ratio $V_{CM}/\Delta V_{OS}$ is equal to or larger than the minimum common mode rejection ratio specification of the amplifier, the maximum possible untrimmed rejection ratio will be obtained. Note that slightly unbalancing either of the R_S or R_f resistors can cancel the DC common mode error due to the amplifier and give an effective rejection ratio of infinity. The resultant common mode error then consists only of distortion components developed in the amplifier as the inputs are swung over the common mode range.

It should be remembered that common mode errors are present only when a voltage is applied to the non-inverting input, and effectively disappear whenever either input voltage becomes zero.

Another source of input offset, which is sometimes overlooked, is the rectification of high frequency signals. These signals may be coupled into the input of the amplifier by capacitive or inductive coupling, or may even be present in the input signal itself. The specification for the maximum frequency where full output can be obtained from the amplifier is usually regarded as a limitation upon the output slewing rate capabilities of the amplifier. However, another reason for this specification is that offsets may be generated when the

input signal contains high value frequency components that exceed the full output response specification.

Noise Any spurious signal at the output of an amplifier that is not present in the input signal can be considered as noise. For AC amplifiers, random noise generated with the amplifier limits the smallest signal that can be distinguished at the input, while in DC applications, offset voltage and offset drift are the dominant factors. Like offset and drift, random noise can be characterized by a series noise-voltage generator and a parallel noise-current generator at the amplifier inputs, as shown in Figure 6.
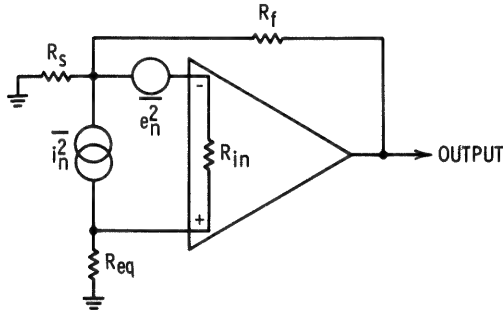

Fig. 6 General Feedback Circuit with Noise Sources.

The generators $\overline{e_n^2}$ and $\overline{i_n^2}$ represent the mean square value of voltage and current assumed to be responsible for the noise generated within the amplifier, and are usually defined in terms of power per unit bandwidth. In general, the amplifier noise generators are not statistically independent; for high-gain transistors operated at low collector currents, however, the correlation coefficient is quite small and may be neglected.

The noise current is found from the noise voltage produced when the amplifier is operated with very high source resistances, and the noise voltage is found from the noise developed with the inputs shorted. With these generators placed in front of the amplifier as inputs, it is possible to calculate the noise performance of the amplifier for any source resistance and bandwidth.

Narrowband Noise The input-referred noise of an amplifier connected in the general feedback circuit of Figure 6 is given by

$$\overline{e_t^2} = 4kTR_T + \overline{i_n^2}R_T^2 + \overline{e_n^2} \qquad (15)$$

where $R_T = R_{eq} + \dfrac{R_s R_f}{R_s + R_f}$ is the total resistance seen by the input terminals.

The first term of Eq. (15) is the thermal noise generated in the source and feedback resistors, and is the noise that would be obtained if the amplifier were noiseless. The second term is the noise voltage produced by the input noise current flowing through the input resistors, and the third term is the contribution from the input noise-voltage generator. It should be noted that the total input noise is independent of the amplifier input resistance, and of any feedback except insofar as these parameters influence the closed-loop gain.

Noise figure is perhaps the most widely used parameter for indicating amplifier noise performance. It is a measure of the degradation in signal-to-noise ratio suffered by a signal passing through the amplifier. Noise figure (F) may be defined as the ratio of the total input noise power to the noise power from the signal source alone, and is commonly expressed in decibels. Thus,

$$F = \frac{\overline{e_t^2}}{\overline{e_g^2}} \qquad (16)$$

where $\overline{e_g^2} = 4\,kTR_g$ is the thermal noise generated by the output resistance of the signal source. In Figure 6, R_g can be represented by either R_s or R_{eq}, depending on whether the inverting or non-inverting connection is used. The other resistors in R_T must be chosen such that their effect is small compared to R_g to keep from degrading the noise figure.

The noise figure will have a minimum value F_m when the source resistance has the optimum value R_{gm}, where

$$R_{gm} = \sqrt{\frac{\overline{e_n^2}}{\overline{i_n^2}}} \ , \text{ and} \qquad (17)$$

$$F_m = 1 + \frac{\overline{e_n^2}}{2kTR_{gm}}. \qquad (18)$$

It is not always possible to connect a matching network between signal source and amplifier to obtain the optimum noise figure. It can be seen from Eq. (15) that the noise figure for low source resistances is determined primarily by the value of the noise-voltage generator, and for high source resistances by the noise-current generator. Both of these generators are usually functions of frequency, with a noise power spectrum which is constant at high frequencies and inversely proportional to frequency at low frequencies. Hence, the

spot noise figure will vary with frequency as well as with source resistance.

The source resistance used in calculating noise figure must be that resistance seen looking directly into the output terminals of the signal source, and should not include external resistors added between source and amplifier. External resistors can only increase the noise figure and thus should be made small compared to R_g. The noise figure will also be degraded by a frequency compensation network connected across the input terminals, as is sometimes used to achieve a high slew rate. This is because the compensation network increases the high-frequency gain seen by the amplifier noise-voltage generator and hence causes a severe increase in high-frequency noise output.

Wideband Noise In general, the noise figure measured over a wide bandwidth will differ from the spot noise figure because of $1/f$ noise. The total wideband input noise can be found by integrating Eq. (15), including the frequency dependence of the noise generators and the frequency response of the amplifier. Thus, the mean square wideband noise is

$$\overline{E_t^2} = \int_0^\infty \overline{e_t(f)^2}\, A(f) df, \qquad (19)$$

where $A(f)$ is the relative frequency response of the circuit.

Eq. (19) is difficult to solve explicitly using exact expressions for noise voltage and gain response. A close approximation can be made, however, by using asymptotes to represent the frequency-dependent characteristics and then integrating by parts. The noise spectrum can be represented as shown in Figure 7(a), where $\overline{e_{to}^2}$ is the total high-frequency spot noise and f_N is the $1/f$ break frequency. Thus.

$$\overline{e_t(f)^2} = \overline{e_{to}^2} \text{ for } f_N \leqslant f \leqslant \infty, \text{ and} \qquad (20)$$

$$\overline{e_t(f)^2} = \overline{e_{to}^2} \left(\frac{f_N}{f}\right) \text{ for } 0 \leqslant f \leqslant f_N. \qquad (21)$$
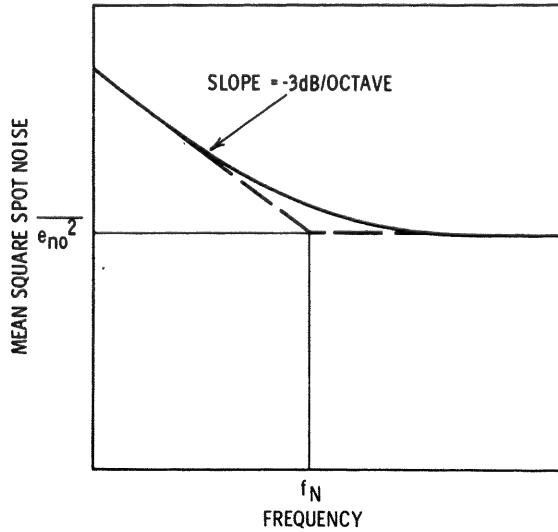
A typical amplifier frequency response is given in Figure 7(b); it rolls off at low frequencies at a rate of $r_1\, dB$/octave beginning at f_L, and at high frequencies at $r_2\ dB$/octave beginning at f_H. Other amplifier frequency characteristics can be approximated in the same manner. Hence, for this example, $A(f)$ is given by

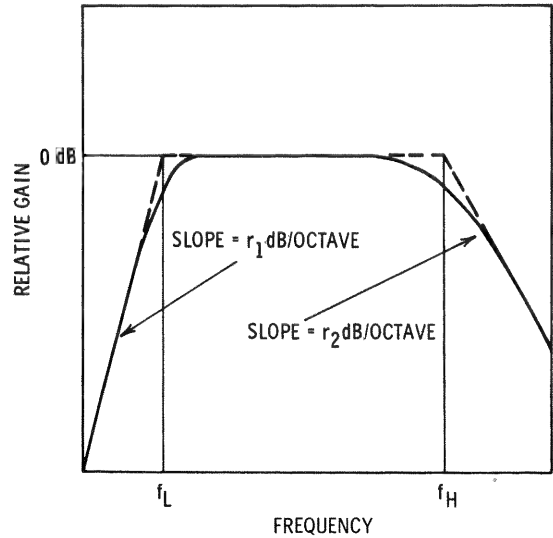$$A(f) = \left(\frac{f}{f_L}\right)^{\frac{r_1}{3}} \quad \text{for } 0 \leqslant f \leqslant f_L, \qquad (22)$$

$$A(f) = 1 \quad \text{for } f_L \leqslant f \leqslant f_H, \text{ and} \qquad (23)$$

$$A(f) = \left(\frac{f_H}{f}\right)^{\frac{r_2}{3}} \quad \text{for } f_H \leqslant f \leqslant \infty. \qquad (24)$$

Assuming that the $1/f$ break frequency of the noise voltage falls within the amplifier passband $(f_L < f_N < f_H)$, the integral of Eq. (19) can be broken into four parts, as follows:

(a.) NOISE SPECTRUM APPROXIMATION

(b.) AMPLIFIER FREQUENCY RESPONSE APPROXIMATION

Fig. 7 Approximate Frequency Characteristics for Finding Wideband Noise.

part 1: $0 \leq f \leq f_L$,

$$\overline{e_1^2} = \int_0^{f_L} \overline{e_{to}^2} \left(\frac{f_N}{f}\right) \left(\frac{f}{f_L}\right)^{\frac{r_1}{3}} df = \overline{e_{to}^2} \left(\frac{3f_N}{r_1}\right) \tag{25}$$

part 2: $f_L \leq f \leq f_N$,

$$\overline{e_2^2} = \int_{f_L}^{f_N} \overline{e_{to}^2} \left(\frac{f_N}{f}\right) df = \overline{e_{to}^2} \, ln \left(\frac{f_N}{f_L}\right) \tag{26}$$

part 3: $f_N \leq f \leq f_H$,

$$\overline{e_3^2} = \int_{f_N}^{f_H} \overline{e_{to}^2} \, df = \overline{e_{to}^2} \, (f_H - f_N) \tag{27}$$

part 4: $f_H \leq f \leq \infty$,

$$\overline{e_4^2} = \int_{f_H}^{\infty} \overline{e_{to}^2} \left(\frac{f_H}{f}\right)^{\frac{r_2}{3}} df = \overline{e_{to}^2} \left(\frac{f_H}{\frac{r_2}{3}-1}\right). \tag{28}$$

The total mean square noise voltage is then given by the sum of Eqs. (25) - (28)

$$\overline{E_t^2} = \overline{e_{to}^2} \left[\frac{f_H}{(1-\frac{3}{r_2})} + f_N \left(\frac{3}{r_1} - 1 + ln\frac{f_N}{f_L}\right)\right]. \tag{29}$$

This wideband noise voltage defines the minimum signal that can be distinguished at the input to the amplifier.

The wideband noise from the signal source alone is found by integrating over the bandwidth:

$$\overline{E_g^2} = \int_0^{\infty} \overline{e_g^2} \, A(f) \, df = \overline{e_g^2} \left[\frac{f_H}{(1-\frac{3}{r_2})} - \frac{f_L}{(1+\frac{3}{r_1})}\right]. \tag{30}$$

Assuming that the bandwidth is reasonably wide ($f_H >> f_L$), the over-all noise figure is

$$F = \frac{\overline{E_t^2}}{\overline{E_g^2}} = \frac{\overline{e_{to}^2}}{4kTR_g} \left[1 + \frac{f_N}{f_H} \left(1 - \frac{3}{r_2}\right) \left(\frac{3}{r_1} - 1 + ln\frac{f_N}{f_L}\right)\right]. \tag{31}$$

In some instances, it is necessary to know the peak-to-peak value of the wideband noise voltage rather than the rms value given by Eq. (29). If the bandwidth is wide enough such that the effect of $1/f$ noise can be neglected, the distribution of the peak amplitude of the noise can be represented by a Normal distribution having a standard deviation equal to the rms value. By defining the peak-to-peak amplitude as that voltage which is exceeded less than 1% of the time, the peak-to-peak noise voltage will be equal to 2.6 times the rms voltage.

Open-Loop Gain

A factor that contributes error in every application employing operational amplifiers is that the amplifier gain is not infinite. Because it isn't, ideal transfer characteristics cannot be obtained exactly and can only be approached, but with an accuracy that is usually limited by the accuracy of the passive components in the circuit.

The general gain relationship for closed-loop circuits where the amplifier has a finite open-loop gain, A_{VO}, is

$$A = (\text{ideal gain}) \left[\frac{1}{1 + \frac{1}{\beta A_{VO}}}\right] \tag{32}$$

$$\text{where } \frac{1}{\beta} = \left(1 + \frac{R_f}{R_s}\right) \left(1 + \frac{R_{eq} + \frac{R_s R_f}{R_s + R_f}}{R_{in}}\right) \tag{33}$$

and R_s, R_f, R_{eq}, R_{in} are as shown in Figure 5.

The term βA_{VO} is defined as the "loop gain" and is the factor that determines how close to the ideal a given amplifier circuit will be. Note that the expression for loop gain is independent of the particular configuration used. This means that an inverting amplifier will have less loop gain for a given closed loop gain than a non-inverting amplifier. Note also from Eq. (33) that the feedback elements must be small compared to the finite amplifier input resistance if the loop gain is not to be degraded.

From Eq. (32) the percentage error due to finite gain is approximately

$$\epsilon(\%) = \frac{100}{\beta A_{vo}} \qquad (34)$$

The gain error given above is not, in itself, particularly important because the feedback resistor ratio can always be trimmed to compensate for this error. However, the stability of the closed-loop gain is an important consideration in most circumstances. Gain stability can be found by differentiation of Eq. (32):

$$\frac{\Delta A}{A} = \frac{\dfrac{\Delta A_{vo}}{A_{vo}}}{1 + \beta A_{vo}} \qquad (35)$$

which shows that any variation in open loop gain is reduced by the loop gain. In general, output impedance, input impedance, linearity, distortion, and gain stability are all improved by the loop gain factor.

Frequency Response Like all amplifying devices, operational amplifiers have the ability and inclination for oscillation under appropriate feedback conditions. Inspection of Eq. (32) reveals that if the loop gain equals unity and its sign is negative (positive feedback), the circuit will oscillate. Therefore, it is necessary to ensure that the loop gain be reduced to less than unity before the loop phase shift reaches 180°. This is accomplished by designing the loop gain to have a uniform roll-off with frequency, at a rate of about 6dB/octave, beginning at a relatively low frequency and continuing until it passes through unity. Since the phase shift associated with such a roll-off (Figure 8) is 90°, the circuit cannot become unstable.

Discrete component operational amplifiers usually have this frequency compensation built in, but integrated circuit versions do not because of the impracticality of integrating the large value capacitors normally required. The user, therefore, must supply his own frequency compensation, external to the microcircuit itself. This has both advantages and disadvantages: it means the user must understand the principles of frequency compensation and be able to apply them to the circuit at hand; but it also means the usefulness and versatility of the amplifier are considerably increased because optimum high frequency bandwidth and loop gain can be obtained for any value closed-loop gain. A 40 dB amplifier with fixed compensation, for example, would have a closed loop bandwidth of only *10kHz* (Figure 9), while variable compensation gives a full *1MHz* bandwidth.

It should be remembered that all parameters which depend upon loop gain — gain stability, input and output impedance, phase shift, linearity, etc. — are degraded at high frequencies because of the necessary roll-off in loop gain.

The close-loop response of an operational amplifier to a pulse or step function input depends upon the amplitude of the signal. For small signals, the
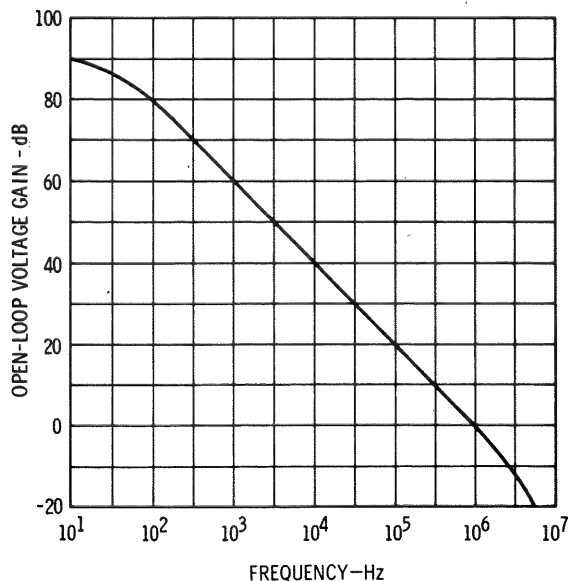
(a) GAIN
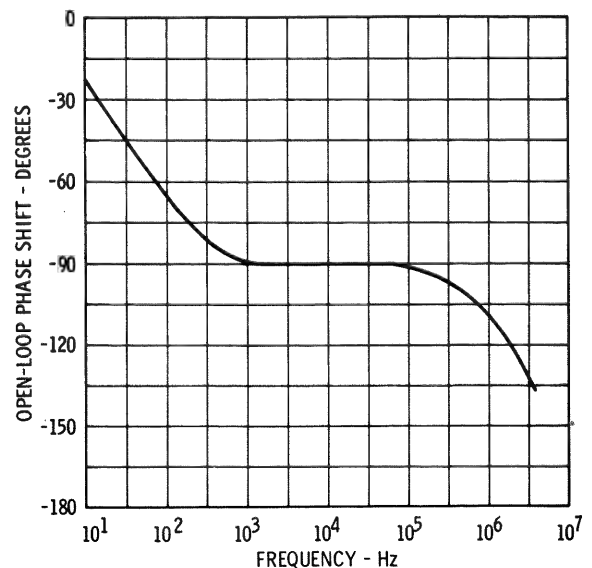
(b) PHASE

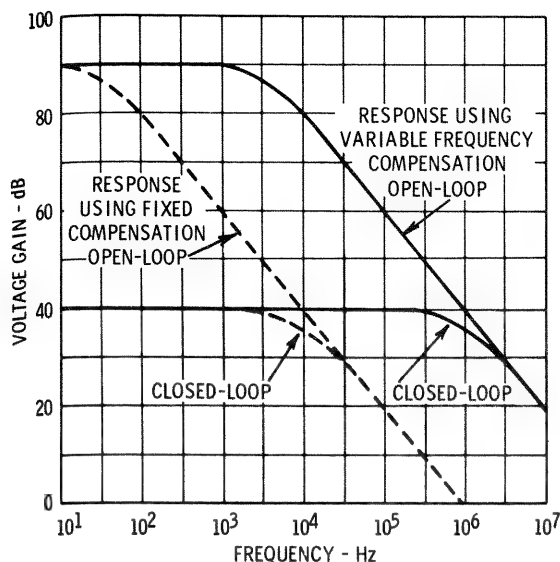Fig. 8 Typical Open-Loop Gain and Phase Frequency Response.

Fig. 9 Performance with Adjustable Frequency Compensation.

output will be an exponential with a time constant inversely proportional to the closed-loop bandwidth. The closed-loop bandwidth, as seen above, can be maximized for any particular gain and does not necessarily have to be inversely proportional to the closed-loop gain, as with discrete amplifiers.

Apart from bandwidth, operational amplifiers have limitations on the maximum rate of change that the output can follow for large input signals. This is a result of the finite current available to charge the internal capacitances at various nodes within the amplifier. The maximum rate of change, or slew rate, also defines the maximum frequency where full sine-wave output swing can be obtained from the amplifier. The slew rate (ρ) is related to the peak sine-wave signal (A_p) at a given frequency (ω) by the equation

$$\rho = A_p \omega \qquad (36)$$

Driving an amplifier beyond its slewing limit results in a triangular output that decreases with increasing frequency. It can also disturb the DC conditions within the amplifier and cause an effective change in the offset voltage, as mentioned previously.

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1. "Operational Amplifiers, Parts I-IV", Analog Devices, Cambridge, Mass.

2. "Handbook of Operational Amplifier Applications", Burr-Brown, Research Corporation, Tucson, Arizona.

3. "Handbook of Operational Amplifier Active RC Networks", Burr-Brown Research Corporation, Tucson, Arizona.

4. "Review of Operational Amplifier Principles", Fairchild Instrumentation, Mountain View, California.

5. "Applications Manual for Computing Amplifiers", Philbrick Researches, Incorporated, Dedham, Mass. (this publication also has an extensive bibliography on operational amplifiers).

6. "Nexus Notes", Nexus Research Laboratories, Incorporated, Canton, Mass.

Since microelectronic components match each other very closely over large temperature ranges and production variations, but absolute values have a relatively large spread, it is natural that balanced circuits such as differential amplifiers are widely used in integrated circuits. The basic circuit is extremely versatile and can provide linear amplification from DC through audio to high frequencies. A differential amplifier usually requires a minimum number of external capacitors in any given application; also, the use of large resistors can usually be avoided and the gain of the circuit can be made a function of resistance ratios rather than of actual resistance values.

The μA730 (Figure 1) is a basic, single-stage differential amplifier intended for use as a gain block in general-purpose DC and AC applications.
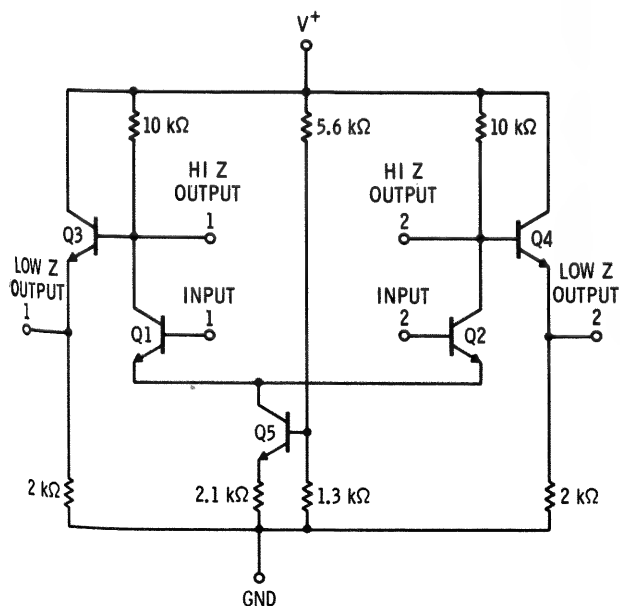
It was formerly available under part number μC111. The circuit uses the standard matched differential pair with a transistor constant current source supplying the emitters; emitter-followers at the output provide a low output impedance and prevent loading of the differential pair. Analysis of the circuit is covered in many standard texts and will not be included here. Figure 2 is a photomicrograph of the device.
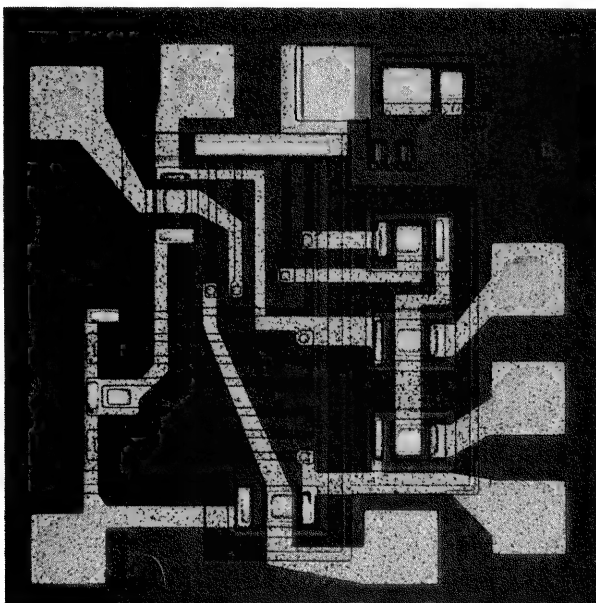
Fig. 2 Photomicrograph of the μA 730.

PERFORMANCE

Typical electrical characteristics are listed in Table I. The excellent matching obtained with monolithic construction is reflected in the offset voltage, offset current, and common-mode rejection figures. The voltage transfer function of the

Fig. 1 Schematic Diagram of the μA 730.

TABLE I

TYPICAL ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS $(T_A = 25°C, V^+ = 12.0\ V,$ and $V_{CM} = 3.5\ V$ Unless otherwise specified)	VALUE	UNITS
Input Offset Voltage	$R_S \leqslant 50\Omega$	1	mV
Input Offset Current		0.5	μA
Input Bias Current		3.5	μA
Input Resistance		20	kΩ
Differential Voltage Gain	$R_L \geqslant 100\ k\Omega$	145	
Differential Distortion	$R_L \geqslant 100\ k\Omega$	80	mVpp
Bandwidth		1.5	MHz
Single-Ended Output Resistance		70	Ω
Output Voltage Swing	$R_L \geqslant 100\ k\Omega$	8.0	Vpp
Supply Current	$R_L \geqslant 100\ k\Omega$	9.5	mA
Power Consumption	$R_L \geqslant 100\ k\Omega$	114	mW
Input Voltage Range		3.5-5.2	V
Common Mode Rejection Ratio	$R_S \leqslant 50\Omega,$ $f \leqslant 1\ kHz,$ $+3.5\ V \leqslant V_{CM} \leqslant +5.2\ V$	85	dB

amplifier is shown in Figure 3. Voltage gain varies about 2dB over the −55°C to +125°C temperature range (Figure 4), and falls 8dB as the supply voltage is decreased from 12V to 6V (Figure 5).

Input offset current and bias current increase at low temperatures due to the falloff in transistor current gain and are roughly proportional to supply voltage. This is shown in Figures 6 through 9. Input and output impedance are also dependent upon current gain, and have the temperature characteristics given in Figures 10 and 11.
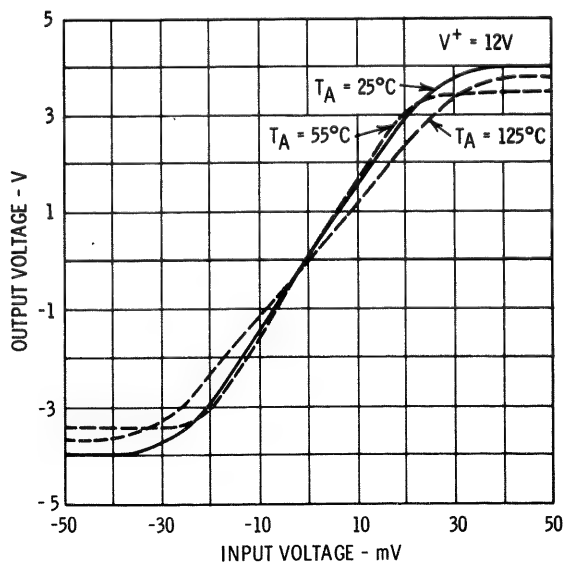
Fig. 3 Voltage Transfer Characteristic.
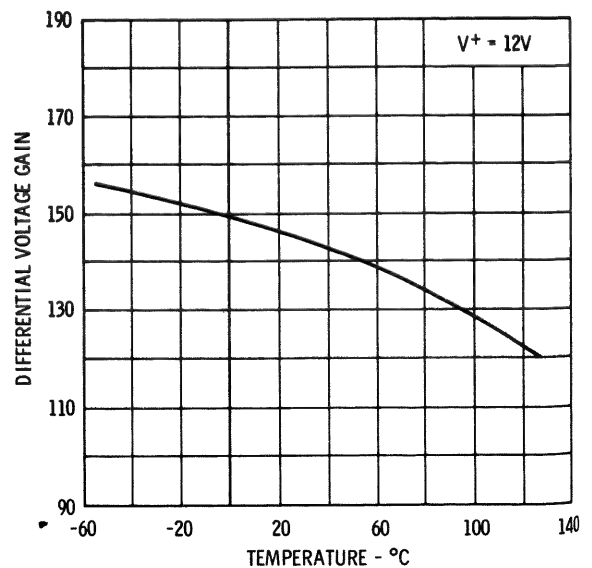
Fig. 4 Differential Voltage Gain as a Function of Ambient Temperature.
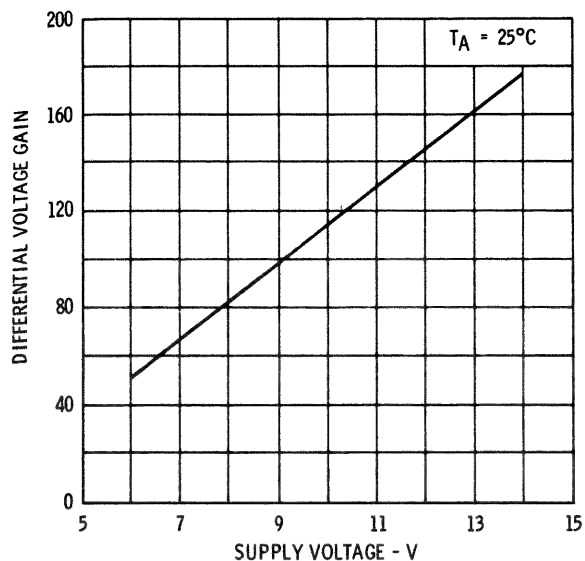
Fig. 5 Differential Voltage Gain as a Function of Supply Voltage.
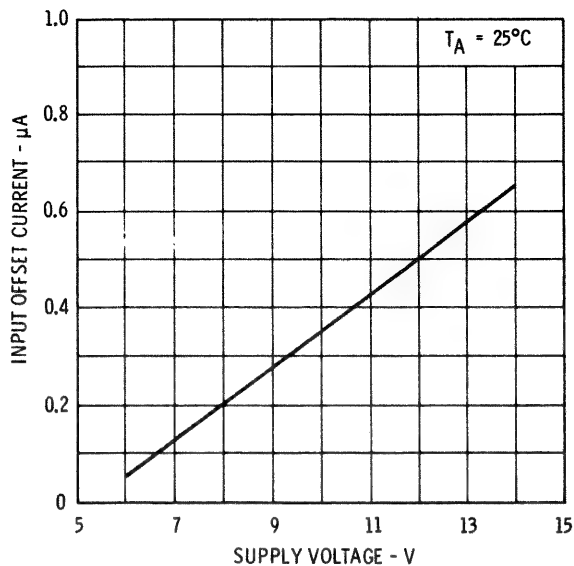
Fig. 7 Input Offset Current as a Function of Supply Voltage.
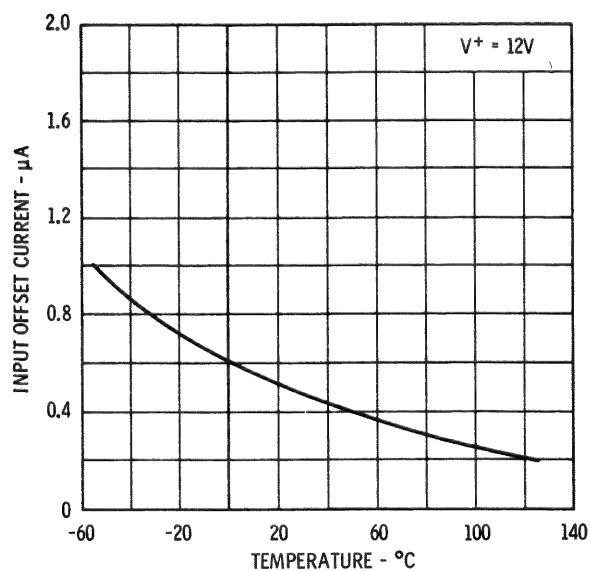
Fig. 6 Input Offset Current as a Function of Ambient Temperature.
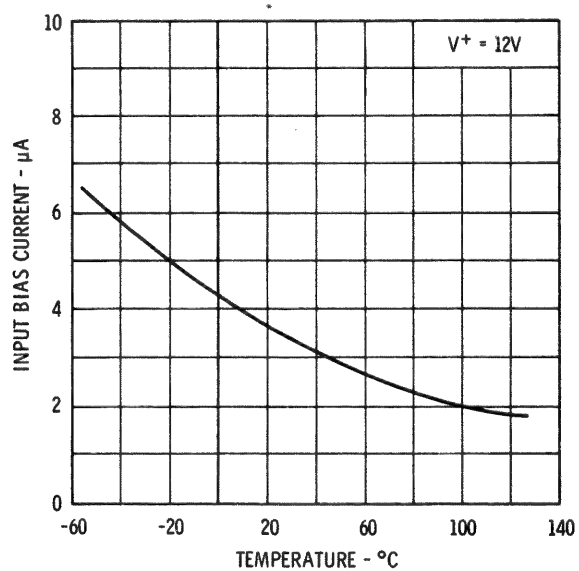
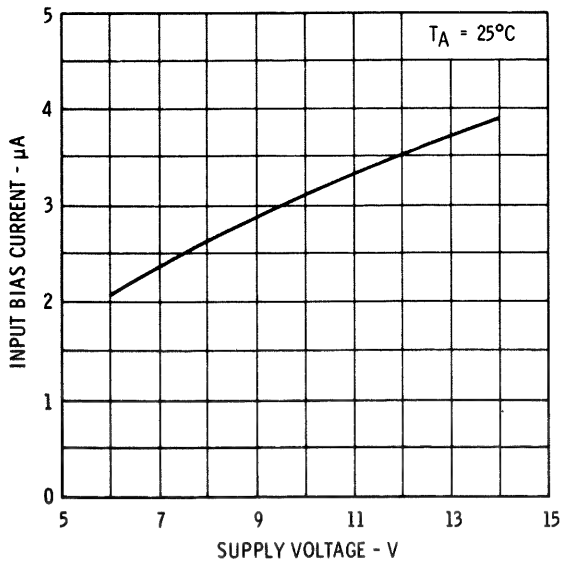Fig. 8 Input Bias Current as a Function of Ambient Temperature.

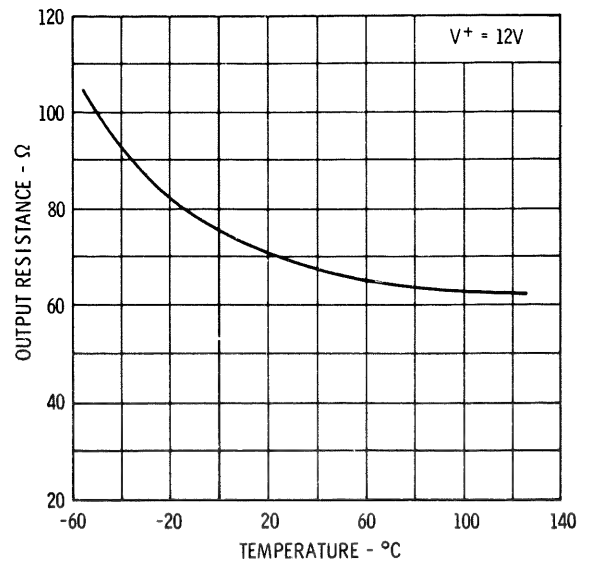Fig. 9 Input Bias Current as a Function of Supply Voltage.

Fig. 11 Output Resistance as a Function of Ambient Temperature.

Common mode rejection ratio is relatively independent of temperature, falling about 5 dB over the temperature range (Figure 12). Figure 13 shows that the common mode output voltage also varies little with temperature; change with supply voltage is given by Figure 14.
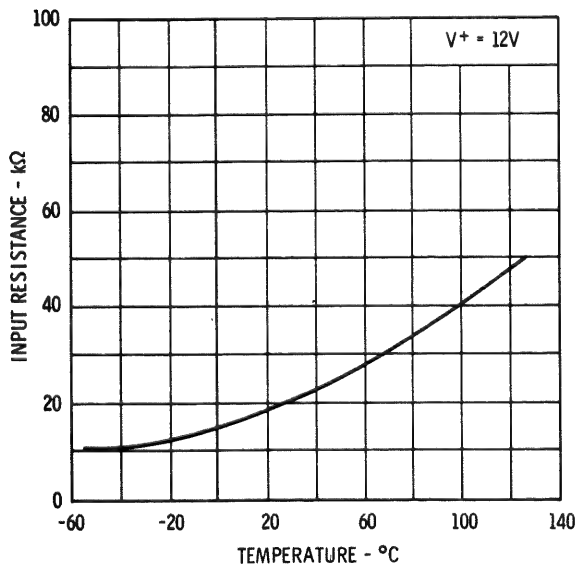
Fig. 10 Input Resistance as a Function of Ambient Temperature.
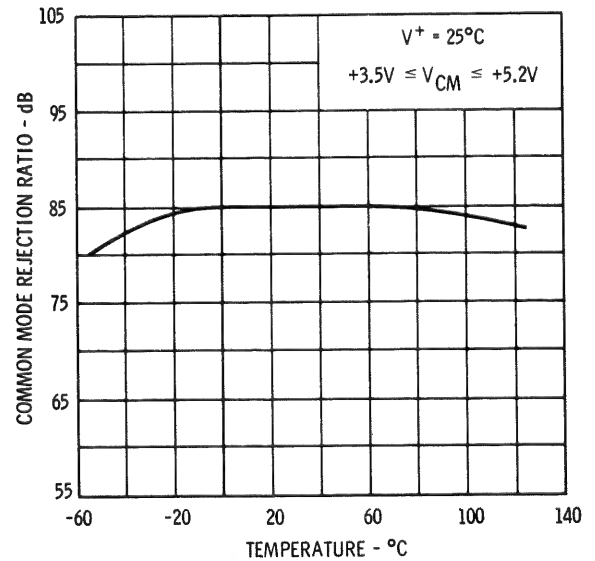
Fig. 12 Common Mode Rejection Ratio as a Function of Ambient Temperature.
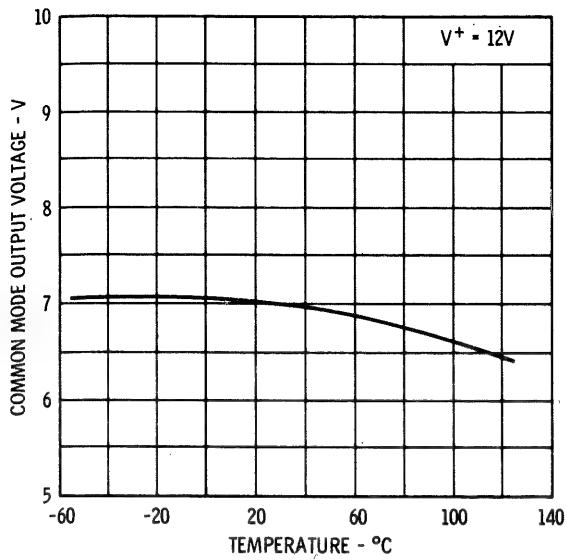
Fig. 13 Common Mode Output Voltage as a
Function of Ambient Temperature.
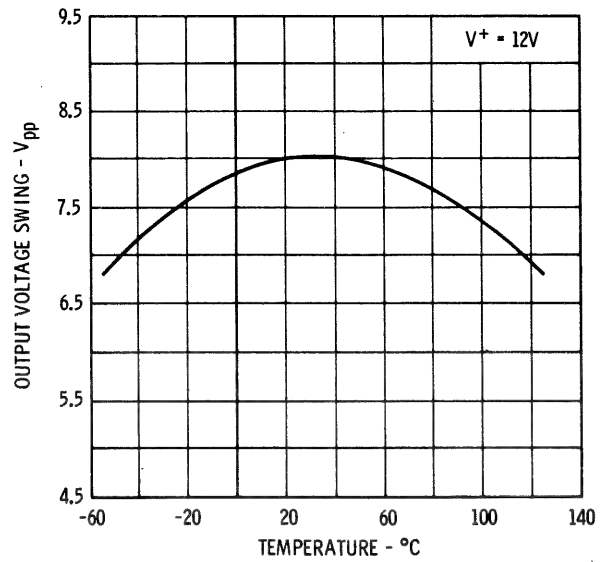
Fig. 15 Output Voltage Swing as a Function of
Ambient Temperature.

Single-ended output voltage swing as a function of temperature, supply voltage, and loading is demonstrated in Figures 15 through 17. Owing to the emitter-follower outputs, the amplifier can drive a 1kΩ load with little loss in output swing.

Power supply requirements are given in Figures 18 and 19. Bandwidth is about $1.5MHz$, as can be seen from the frequency response shown in Figure 20.
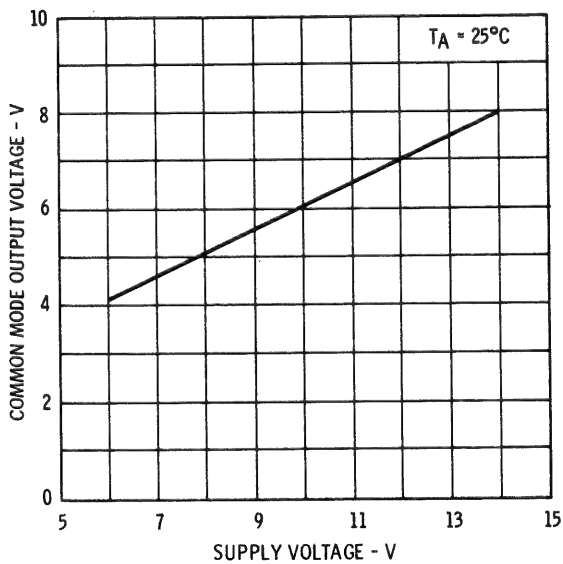
Fig. 14 Common Mode Output Voltage as a
Function of Supply Voltage.
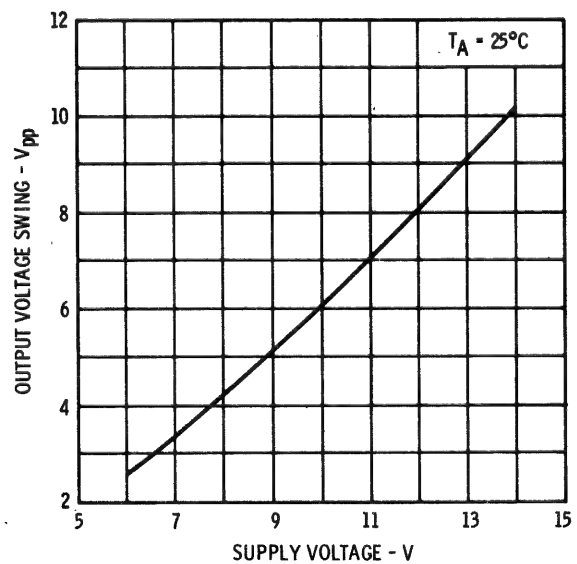
Fig. 16 Output Voltage Swing as a Function of
Supply Voltage.

31
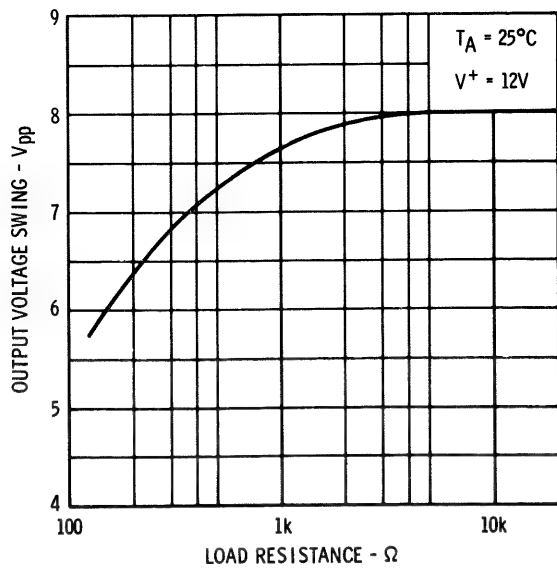
Fig. 17 Output Voltage Swing as a Function of
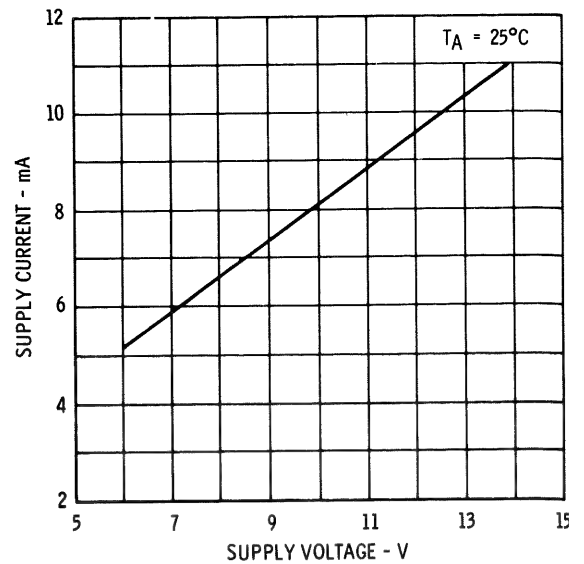Load Resistance.

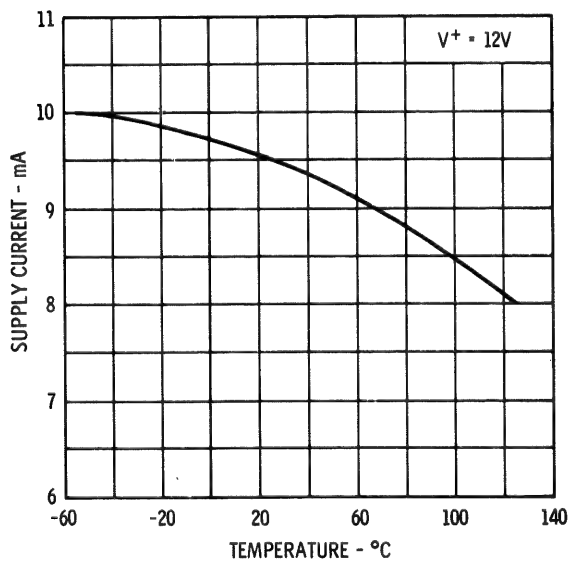Fig. 19 Supply Current as a Function of Supply
Voltage.

Fig. 18 Supply Current as a Function of Ambient
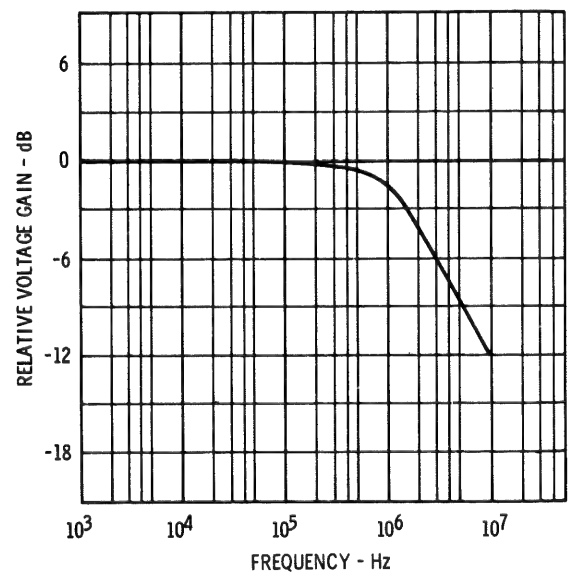Temperature.

Fig. 20 Frequency Response.

The μA702A is a medium-gain operational amplifier meant for use with external feedback elements to determine operating characteristics. It is useful as a general-purpose DC or AC amplifier to frequencies as high as 30 *MHz*.

Applications include amplifying the output of transducers such as resistive bridges, thermocouples, hall-effect devices, and photodiodes. With proper feedback elements, it can also perform the integrating, differentiating, summing, and subtracting functions required in an analog computer. In addition, the amplifier can be used with reactive feedback elements for precise frequency shaping of the gain characteristics, or with a bridged-T filter to make a bandpass amplifier. Diodes can be incorporated in the feedback loop to form a low-threshold detector and instrument rectifier, or the amplifier can be operated open loop as a voltage comparator.

The μA702A utilizes the inherent advantages of monolithic construction to achieve low DC offset and low thermal drift, as well as wide-band operation and low power consumption. A Planar* epitaxial manufacturing process, similar to that widely used by Fairchild Semiconductor for digital integrated circuits, is employed. A sectional view indicating the different diffusions is given in Figure 1.

The circuit is unusual in that large resistances and complementary transistors have been eliminated with no sacrifice in performance. In addition, the important characteristics of the amplifier are dependent only on the matching of components, rather than their absolute value. The degree of match normally available in integrated circuitry makes adjustments unnecessary.

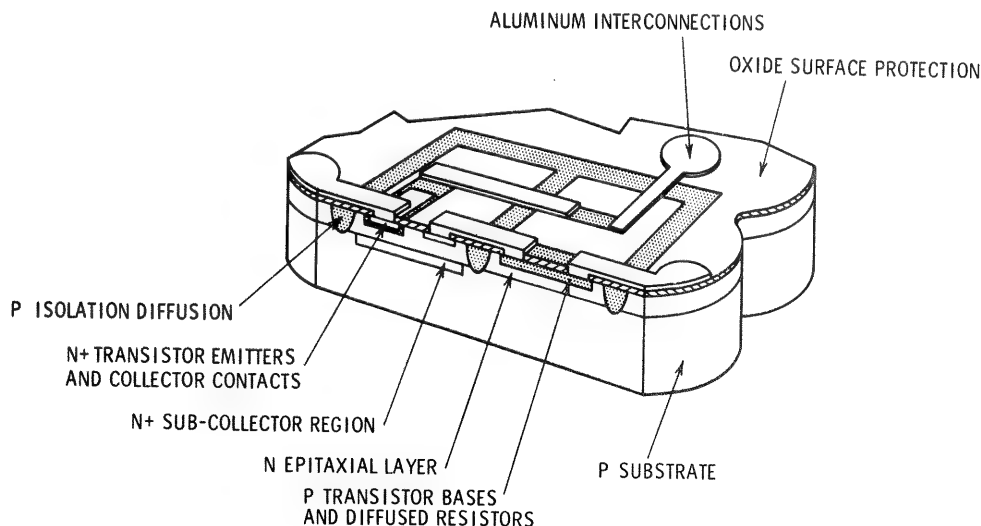The active area of the integrated amplifier has been minimized not only to improve high-fre-

ALUMINUM INTERCONNECTIONS

OXIDE SURFACE PROTECTION

P ISOLATION DIFFUSION

N+ TRANSISTOR EMITTERS AND COLLECTOR CONTACTS

N+ SUB-COLLECTOR REGION

N EPITAXIAL LAYER

P TRANSISTOR BASES AND DIFFUSED RESISTORS

P SUBSTRATE

Fig. 1 Sectional View of Fairchild Planar Epitaxial Integrated Circuit.

* Planar is a patented Fairchild process.

quency response, but also to reduce the possibility of crystalline defects and surface phenomena that may cause failures. This helps to decrease manufacturing costs as well as increase reliability. A photomicrograph of the 45-mil square chip is shown in Figure 2.
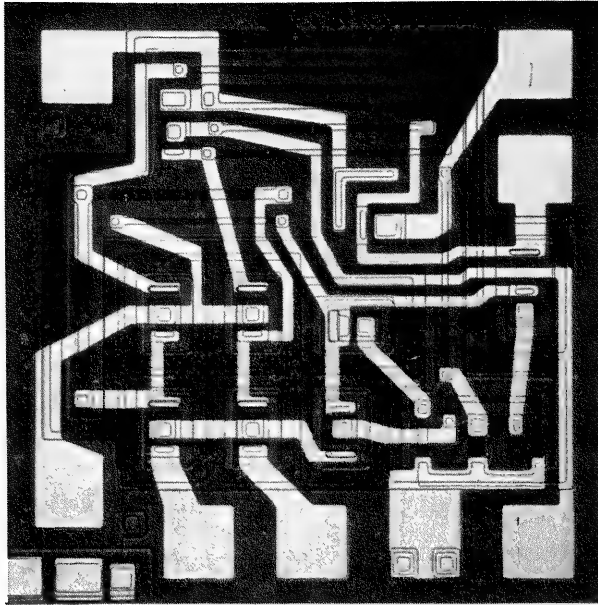

Fig. 2 Photomicrograph of the μA 702A.

INPUT STAGE

In general, the desirable characteristics for the input stage of a DC amplifier are low offset voltage, offset current, input current, and thermal drift. Matched differential pairs are almost universally used. With this configuration, the input bias of one active device cancels that of the other to give offset and drift dependent only on the degree of match.

In cases where offset voltage is of prime importance, the bipolar transistor is undoubtedly the best choice of an active device for the input stage. Offset voltages of a few millivolts are easily obtained over a wide temperature range. Low input currents and high input impedance can be realized by using very high-gain transistors and operating them at sufficiently low collector currents. A Darlington input stage can also be used at some sacrifice in offset voltage, thermal drift, and noise figure. Other active devices, notably the field-effect transistor, are difficult to match closer than several tens of millivolts. Low offset and drift with FET's cannot be obtained without elaborate compensation procedures. The use of these devices is limited, accordingly, to cases where offset voltage is of secon-

dary importance and an input current less than a few nanoamperes is mandatory.

Thus it appears that the most satisfactory compromise for the input stage of a general-purpose amplifier is a matched pair of bipolar transistors operated at a low collector current. In an integrated circuit, the input-stage transistors can be matched quite easily over several decades of collector current by making them with identical structures and locating them physically close together. There is, however, a problem in obtaining the low collector currents; conventional circuit designs require large resistance values.

Greatly reduced resistance values can be used at the expense of input-stage gain. Some analysis of the problem shows that a low gain in the input stage can be tolerated if the second stage is well-balanced. The offset of the second stage appears as an input offset divided by the gain of the input stage. In the distribution curves obtained in manufacturing an integrated amplifier, the input stage offset will increase with the equivalent second-stage offset as the square root of the sum of squares. For example, if the gain of the input stage is two and the 90-percent point in the distribution curves for the individual input and second stage offsets is 5 mV, the 90-percent point in the distribution of complete amplifiers will be only 5.6 mV. Hence, even with this low gain, the offset contribution from the second stage is quite small.

These facts were used in the design of the input stage (see Figure 3). The transistors are operated at 200-μA collector current, but only 2-kΩ collector-load resistors are used. This gives an unloaded differential gain of approximately 15. Therefore, if a balanced second-stage design is employed, its contribution to input offset can be made negligible. The differential input stage (Q_2 and Q_3) and its load resistors (R_1 and R_2) can be seen in Figure 3. The emitters of the input stage are fed from a current source (Q_1) to obtain good input common-mode rejection. The current source is biased from a voltage divider. The V_{BE} of the current-source transistor is compensated in the divider with a diode-connected transistor (Q_9).

SECOND STAGE

The second stage must be designed to operate with the small DC drops across the input stage load resistors and at the same time be as inherently well-balanced as the input stage. The full differential gain of the input stage should also be used. Additionally, it would be advantageous to have a single-ended output, since continuing with a differential connection to the third stage increases the number of components and creates physical layout problems on the silicon chip.

A connection which satisfies all these requirements is shown in Figure 3, which is a modification of the balanced circuit discussed in Chapter 2. Q_4

An additional feature of this circuit is that under balanced conditions the single-ended output of Q_5 is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both Q_4 and Q_5 will increase such that the voltage on the collector of Q_5 remains constant; if this voltage does change due to mismatch, the change is divided by a gain of roughly 1,000 before appearing in the input.

Because of the small load resistances of the input stage, the second-stage amplifier (Q_5) is essentially voltage-driven. The gain is not, therefore, greatly affected by the current gain of Q_5 and is relatively constant over a wide range of operating temperatures.
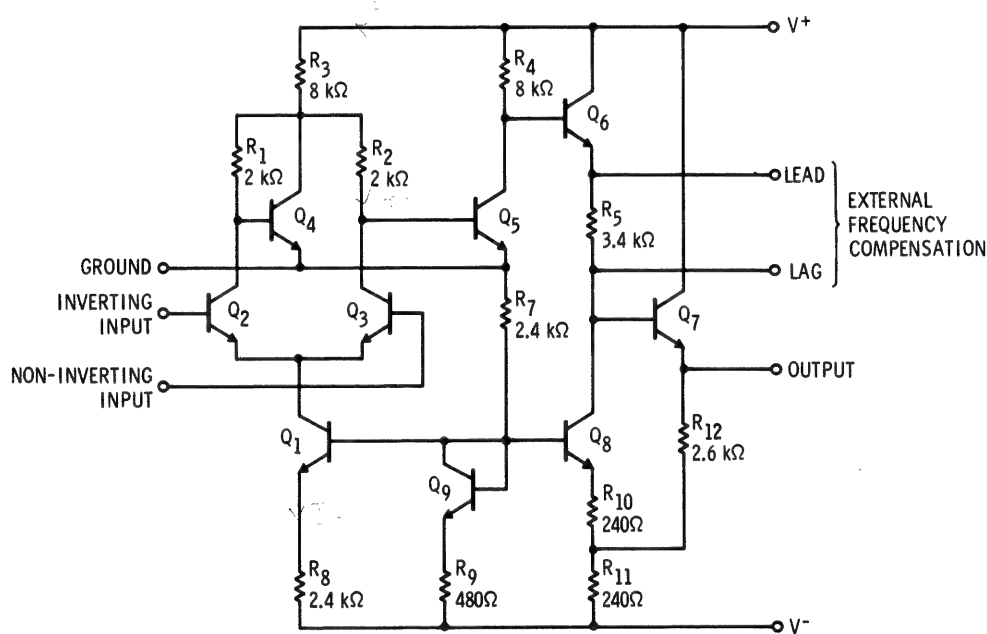
Fig. 3 Schematic Diagram of the μA 702A.

and Q_5 are identical transistors placed close to one another. Their bases are fed from a common voltage point through identical resistors (the input-stage load resistors, R_1 and R_2). Thus, when the input-stage collector currents are equal, the collector currents of Q_4 and Q_5 will likewise be equal, and the second stage will be balanced. Q_4 also functions as a unity gain amplifier that inverts the output of Q_2 and combines it with the output of Q_3 at the base of Q_5. Therefore, the full differential gain of the input stage is used and a single-ended output obtained.

OUTPUT STAGE

The first two stages have provided nearly enough voltage gain for the amplifier (> 60 dB). Since both positive and negative output swings are desired, some form of DC level shifting must be provided since the output of the second stage cannot swing negative. The usual solution to this problem is to use a PNP transistor both to give the level shifting and to provide additional gain. This is not a simple answer in monolithic integrated circuits. A second approach to level shifting is the use of a zener diode, but they are noisy and can appreciably affect the over-all noise figure of the amplifier. Furthermore, only a single-voltage zener diode (the emitter-base junction) is usually available in the circuit.

In the μA702A, the unique level-shifting circuit described in Chapter 2 is used to avoid these difficulties. It incorporates only NPN transistors, yet its performance is comparable to designs using the best complementary transistors. As can be seen from Figure 3, the output of the second stage is buffered with an emitter-follower (Q_6). A current source (Q_8) provides a voltage drop across R_5 that gives the basic level shifting. An additional emitter-follower, (Q_7) is used to achieve low output impedance. The load resistor of Q_7 is fed back to the emitter of Q_8 giving a controlled amount of positive feedback. Hence, the output stage actually has a gain in addition to DC level shifting. The feedback also enhances the available output swing so that it is nearly equal to the supply voltages.

Characteristics of this output stage include a 200-$k\Omega$ input impedance, a $5V$ DC level shift, a voltage gain of 2.5 and a 200-Ω output impedance. It can deliver a peak-to-peak symmetrical output swing of about 1.8 times the negative supply voltage.

CONDITIONS FOR DC BALANCE

An interesting feature of the over-all amplifier design is that DC balance (zero output for zero input) can be obtained independent of the supply voltages and absolute resistor values. This will be shown to hold true to a first approximation in the analysis that follows. Infinite current gains will be assumed for the transistors, as will perfect component matching in some cases. In addition, the emitter-base voltages of certain transistors will be considered equal even though they are operating at different current levels. The latter assumption is not unreasonable for an integrated circuit in that the transistor geometries can be scaled in proportion to the operating current.

Using Figure 3, the output voltage can be written as

$$V_o = V^+ - R_4 I_{C5} - R_5 I_{C8} - 2V_{BE} \qquad (1)$$

If the input-stage collector currents are equal, Q_4 and Q_5 are well matched, and R_1 is equal to R_2, then I_{C4} and I_{C5} will be equal. Thus,

$$V^+ - R_3 I_{C5} - \left(R_3 + \frac{R_1}{2}\right) I_{C1} - V_{BE} = 0 \qquad (2)$$

The collector current of Q_8 is given by

$$I_{C8} = \frac{\dfrac{R_9(V^- + V_{BE})}{R_7 + R_9} - \dfrac{R_{11}(V^- - V_0)}{R_{11} + R_{12}}}{R_{10} + \dfrac{R_{11}R_{12}}{R_{11} + R_{12}}} \qquad (3)$$

while the collector current of Q_1 is

$$I_{C1} = -\frac{R_9(V^- + V_{BE})}{R_8(R_7 + R_9)} \qquad (4)$$

Substituting Eq. (3) into Eq. (1) yields

$$\left(1 - \frac{R_5 R_{11}}{R_{10}R_{11} + R_{10}R_{12} + R_{11}R_{12}}\right) V_o =$$

$$V^+ - R_4 I_{C5} + \frac{R_5\left(\dfrac{R_9}{R_7 + R_9} - \dfrac{R_{11}}{R_{11} + R_{12}}\right)}{R_{10} + \dfrac{R_{11}R_{12}}{R_{11} + R_{12}}} V^-$$

$$+ \left(\frac{\dfrac{R_9 R_5}{R_7 + R_9}}{R_{10} + \dfrac{R_{11}R_{12}}{R_{11} + R_{12}}} - 2\right) V_{BE} \qquad (5)$$

Combining Eq. (4) and Eq. (2) gives

$$V^+ - R_3 I_{C5} + \frac{R_9\left(R_3 + \dfrac{R_1}{2}\right)}{R_8(R_7 + R_9)} V^-$$

$$+ \left(\frac{R_3 + \dfrac{R_1}{2}}{R_8 (R_7 + R_9)} - 1\right) V_{BE} = 0 \qquad (6)$$

For balanced input and second stages, as assumed, the output voltage will be given as a function of circuit parameters by the set of Eqs. (5) and (6) above. It is desired that the output voltage under this condition be zero, independent of supply voltages. This can be accomplished by setting the coefficients of V^+, I_{C5} and V^- in Eq. (5) equal to the corresponding coefficients in Eq. (6). Hence, if

$$R_3 = R_4 \qquad (7)$$

and

$$\frac{R_5\left(\dfrac{R_9}{R_7 + R_9} - \dfrac{R_{11}}{R_{11} + R_{12}}\right)}{R_{10} + \dfrac{R_{11}R_{12}}{R_{11} + R_{12}}} = \frac{R_9\left(R_3 + \dfrac{R_1}{2}\right)}{R_8(R_7 + R_9)} \qquad (8)$$

Eqs. (5) and (6) can be combined to give

$$\left(1 - \frac{R_5 R_{11}}{R_{10}R_{11} + R_{10}R_{12} + R_{11}R_{12}}\right) V_o =$$

$$\left(-1 + \frac{\dfrac{R_9 R_5}{R_7 + R_9}}{R_{10} + \dfrac{R_{11}R_{12}}{R_{11} + R_{12}}} - \frac{R_9\left(R_3 + \dfrac{R_1}{2}\right)}{R_8\,(R_7 + R_9)}\right) V_{BE} \qquad (9)$$

Substituting Eq. (8) into Eq. (9) yields

$$V_o = -V_{BE} \qquad (10)$$

Since V_{BE} is approximately 700 mV and the open-loop gain of the amplifier is approximately 3,600, the input-referred offset is roughly 0.19 mV, or about an order of magnitude smaller than offset due to random mismatching. Thus, the output voltage at null given by Eq. (10) is essentially zero and independent of both supply voltages. Further, if every resistor in the circuit is multiplied by any constant, Eqs. (7) and (8) will not be altered. The conditions that establish Eq. (10), then, are dependent only on resistor ratios — not absolute values.

Rough, order-of-magnitude calculations show that for h_{FE} greater than 30, the assumption of infinite h_{FE} is reasonable, and in fact has been substantiated by experimental work. The effect of current gain on offset was found to be substantially less than the offset due to other causes. Actually, the offsets produced by the different base currents tend to cancel nearly as well as the current-gain matching of various units will permit.

DC OFFSET AND COMPONENT MATCHING

It was assumed previously that certain components were perfectly matched and that the ratio of all resistors was held constant. This is obviously not quite true. In this section, the effect of mismatches on offset voltage will be investigated, followed by a brief description of the techniques used to minimize them.

First, the sensitivity of offset voltage to deviations in resistor ratios will be considered. The simplest method of determining the relative sensitivity of the individual resistors is to change the value of each resistor in the circuit independently and measure the effect on offset. This was done with the amplifier, and the results are given in Table I. Except for R_1 and R_2, a 10% change in any resistor value has little effect on offset. Since the actual resistance ratios in integrated circuitry are held substantially closer than 10%, deviations in the resistance ratios of R_3 through R_{12} can be neglected. Of greatest importance is the matching of R_1 with R_2, rather than the other resistors, because the offsets tend to cancel if both change together (see Table I). For this reason, these resistors have identical geometric structures, are located close together, and are made wider than other resistors.

TABLE I

CHANGE IN INPUT-REFERRED OFFSET VOLTAGE FOR 10-PERCENT CHANGE IN INDIVIDUAL RESISTOR VALUES

Resistor	Nominal Value (kΩ)	Change in Offset Voltage (mV)
R_1	2.0	+2.9
R_2	2.0	−2.9
R_3	8.0	−0.7
R_4	8.0	+0.5
R_5	3.4	+0.3
R_7	2.4	−0.1
R_8	1.4	+0.4
R_9	0.48	+0.1
R_{10}	0.24	−0.1
R_{11}	0.24	−0.3
R_{12}	2.6	+0.2

The offset sensitivity to mismatches in transistor parameters can likewise be determined. Experimentation similar to that used to determine resistor sensitivities has shown that the matching of Q_2 with Q_3 and Q_4 with Q_5 in both current gain and emitter-base voltage clearly dominates in determining offset. Every effort was made in mask design to assure that these pairs would be well-matched. First, the devices were located as close together as possible. The small size permitted center-to-center spacings of 5 mils. Second, the distance between these transistors and elements dissipating appreciable power was maximized to eliminate thermal gradients.

PERFORMANCE

Typical performance of the amplifier is summarized in Table II. Inherent design balance is demonstrated by the low offset voltage and thermal drift characteristics and the excellent supply voltage rejection and common mode rejection. Within certain limits, the amplifier may be operated with practically any combination of supply voltages without greatly affecting offset: the indicated 2:1 ratio of

TABLE II
TYPICAL PERFORMANCE FIGURES FOR THE μA702A

PARAMETER	CONDITIONS ($T_A = 25°C$ unless otherwise specified)	$V^+ = 12.0$ V, $V^- = -6.0$ V	$V^+ = 6.0$ V, $V^- = -3.0$ V	UNITS
Input Offset Voltage	$R_S \leqslant 2$ kΩ	0.5	0.7	mV
Input Offset Current		180	120	nA
Input Bias Current		2.0	1.2	μA
Input Resistance		40	67	kΩ
Input Voltage Range		-4 to $+0.5$	-1.5 to $+0.5$	V
Common Mode Rejection Ratio	$R_S \leqslant 2$ kΩ, $f \leqslant 1$ kHz	100	100	dB
Large-Signal Voltage Gain	$R_L \geqslant 100$ kΩ, $V_{out} = \pm 5.0$ V	3600		
	$R_L \geqslant 100$ kΩ, $V_{out} = \pm 2.5$ V		900	
Output Resistance		200	300	Ω
Supply Current	$V_{out} = 0$	5.0	2.1	mA
Power Consumption	$V_{out} = 0$	90	19	mW

The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$:

PARAMETER	CONDITIONS	$V^+ = 12.0$ V, $V^- = -6.0$ V	$V^+ = 6.0$ V, $V^- = -3.0$ V	UNITS
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω, $T_A = 25°C$ to $T_A = +125°C$	2.5	3.5	μV/°C
	$R_S = 50$ Ω, $T_A = 25°C$ to $T_A = -55°C$	2.0	3.0	μV/°C
Input Offset Current	$T_A = +125°C$	80	50	nA
	$T_A = -55°C$	400	280	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$	1.0	0.7	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$	3.0	2.0	nA/°C
Input Bias Current	$T_A = -55°C$	4.3	2.6	μA
Common Mode Rejection Ratio	$R_S \leqslant 2$ kΩ, $f \leqslant 1$ kHz	95	95	dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = -6$ V to $V^+ = 6$ V, $V^- = -3$ V $R_S \leqslant 2$ kΩ	75	75	μV/V
Output Voltage Swing	$R_L \geqslant 100$ kΩ	± 5.3	± 2.7	V
	$R_L \geqslant 10$ kΩ	± 4.0	± 2.0	V
Supply Current	$T_A = +125°C$, $V_{out} = 0$	4.4	1.7	mA
	$T_A = -55°C$, $V_{out} = 0$	5.0	2.1	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$	80	15	mW
	$T_A = -55°C$, $V_{out} = 0$	90	19	mW

positive and negative supply voltages need not be strictly maintained. The gain and output swing will, of course, be determined by the supply voltages. Increased output swing (up to about ±7V) can be obtained with larger negative supply voltages. Little is gained, however, by increasing the negative supply voltage beyond 70 percent of the positive supply voltage. The voltage gain and input bias current of the amplifier are roughly proportional to the negative supply voltage.

The voltage-transfer characteristics of the amplifier given in Figures 4 and 5 illustrate output-swing capabilities and linearity for supply voltages of +12V, −6V, and +6V, −3V. The maximum available symmetrical output swing is plotted as a function of load resistance in Figure 6. The primary

Fig. 6 Output Voltage Swing as a Function of Load Resistance.

limitation on output swing under load is the current available from the output load resistor (R_{12}) to drive the load with negative outputs. The swing can be improved, therefore, by connecting an external resistor between the output terminal and the negative supply voltage, as shown in Figure 6. Even larger swings can be obtained if the resistor is returned to a more negative supply. Since the output impedance is quite low, considerable excess current can be drawn in this fashion without affecting offset or gain. The peak current from the output terminal should, however, be kept below 10 mA, as higher currents would cause excessive dissipation in the output transistor, thermal gradients across the silicon die, and possible thermal feedback. Figure 7 shows how the output swing varies with supply voltage.

Fig. 4 Voltage Transfer Characteristic for +12V, −6V Supplies.
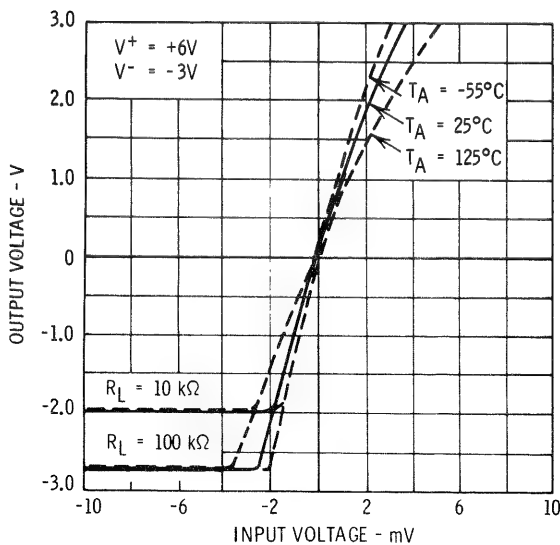
Fig. 5 Voltage Transfer Characteristic for +6V, −3V Supplies.
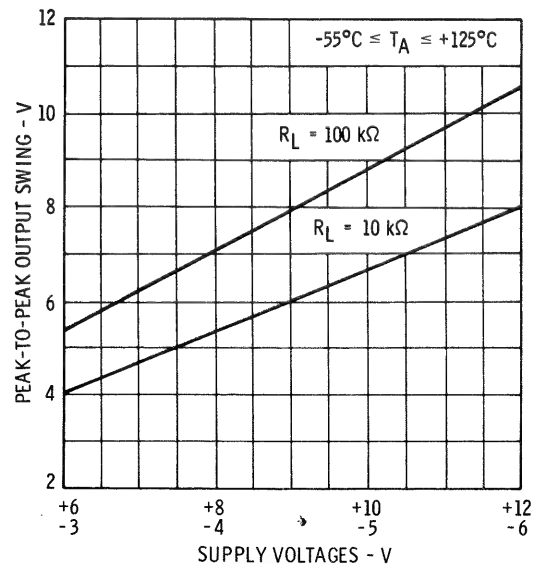
Fig. 7 Output Voltage Swing as a Function of Supply Voltages.

The variation of open-loop voltage gain with temperature is primarily a function of the temperature dependance of the transistor current gain, which has a positive temperature coefficient, and the transistor transconductance, which has a negative temperature coefficient. The variation in resistance values is negligible since, to a first order approximation, the gain depends only on resistor ratios. Since the transistor current gains obtained in the manufacture of the $\mu A702A$ are quite high (even at $-55°C$), the transconductance terms dominate, giving the gain characteristics shown in Figures 8 and 9. The gain falls off about 3 dB at $+125°C$ and rises 1.2 dB at $-55°C$. This small change makes the amplifier quite useful in applications requiring extreme closed-loop gain accuracy over a wide temperature range. As mentioned above, the voltage gain is strongly dependent upon the supply voltages. Figure 10 shows that the gain falls about 12 dB as the supplies are reduced from $+12V$, $-6V$ to $+6V$, $-3V$.
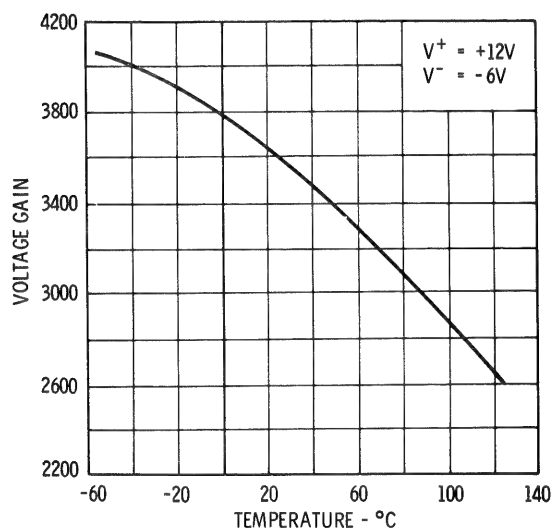
Fig. 8 Voltage Gain as a Function of Ambient Temperature for +12V, −6V Supplies.
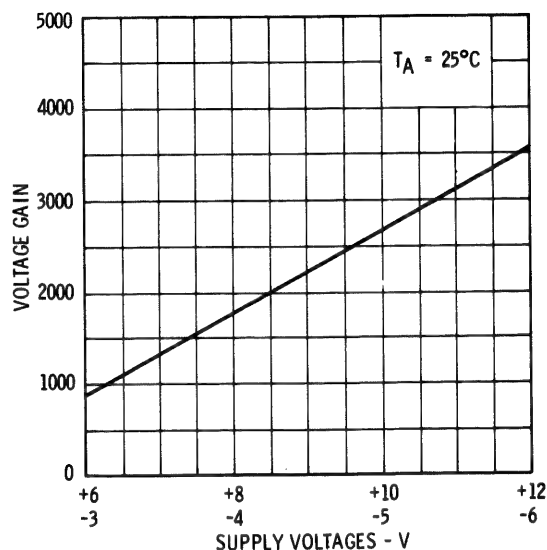
Fig. 10 Voltage Gain as a Function of Supply Voltages.

The input and output impedances and input bias current are direct functions of transistor current gain, and have the temperature dependance illustrated in Figures 11 through 13. Since the input

Fig. 9 Voltage Gain as a Function of Ambient Temperature for +6V, −3V Supplies.
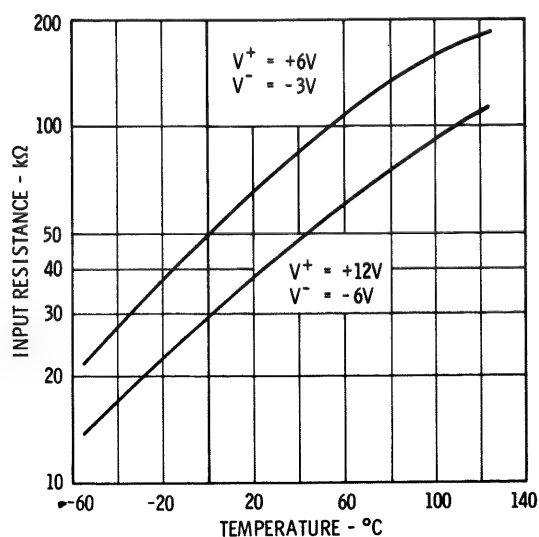
Fig. 11 Input Resistance as a Function of Ambient Temperature.
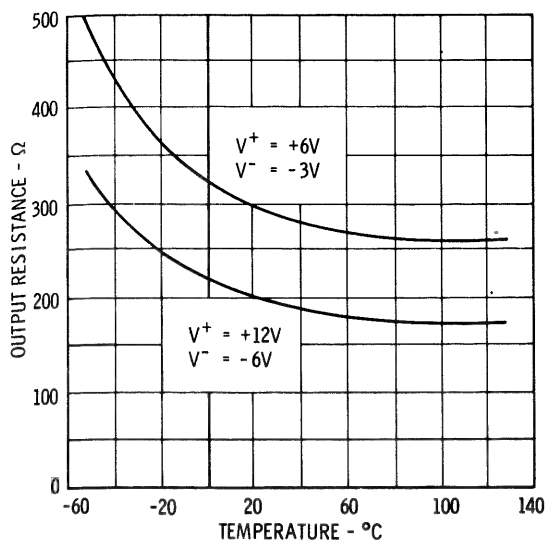
Fig. 12 Output Resistance as a Function of Ambient Temperature.
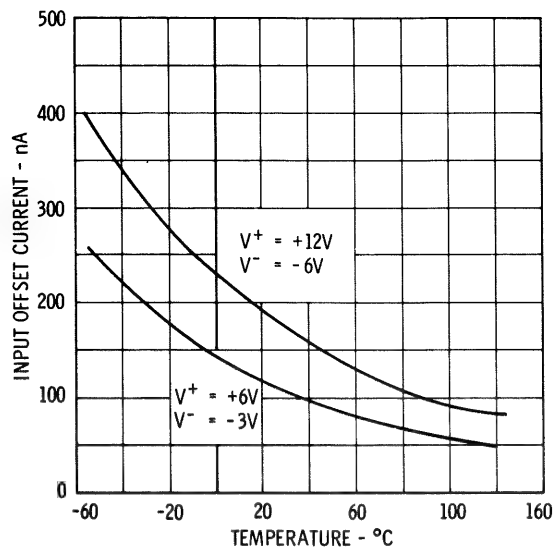
Fig. 14 Input Offset Current as a Function of Ambient Temperature.
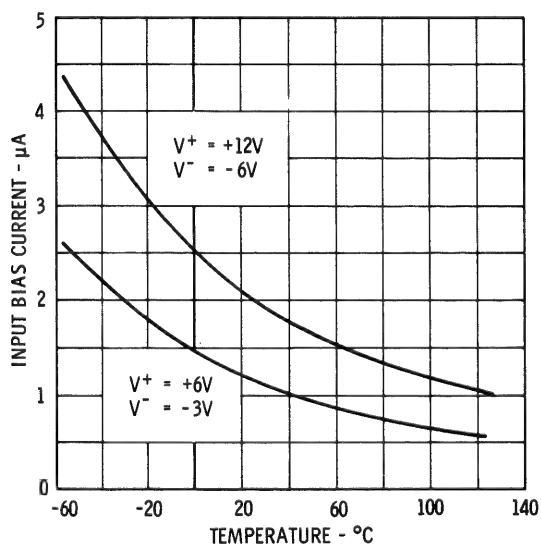
Fig. 13 Input Bias Current as a Function of Ambient Temperature.
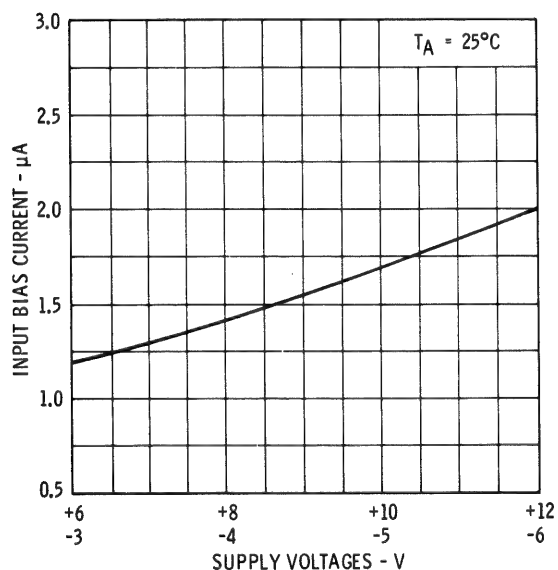
Fig. 15 Input Bias Current as a Function of Supply Voltages.

offset current is a function of the degree of match between the bias currents into the two inputs, it also increases with decreasing temperature as shown in Figure 14. Variation with changes in supply voltage is given in Figures 15 and 16.

The close matching of components in the input stages of the amplifier contributes to excellent common mode and supply voltage rejection ratios. The common mode rejection ratio changes less than 5 dB and the supply rejection ratio less than

41
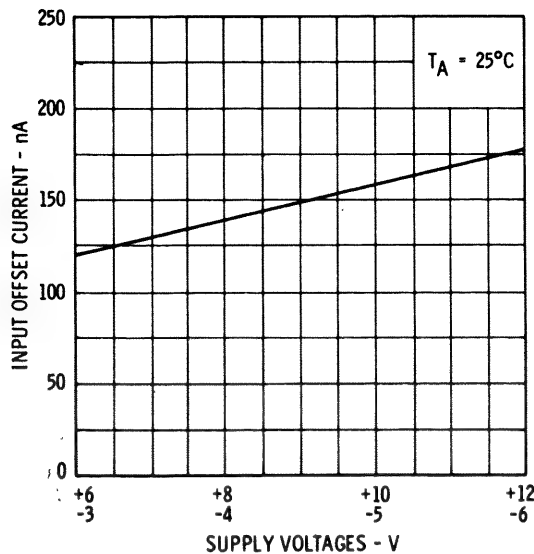
Fig. 16 Input Offset Current as a Function of Supply Voltages.
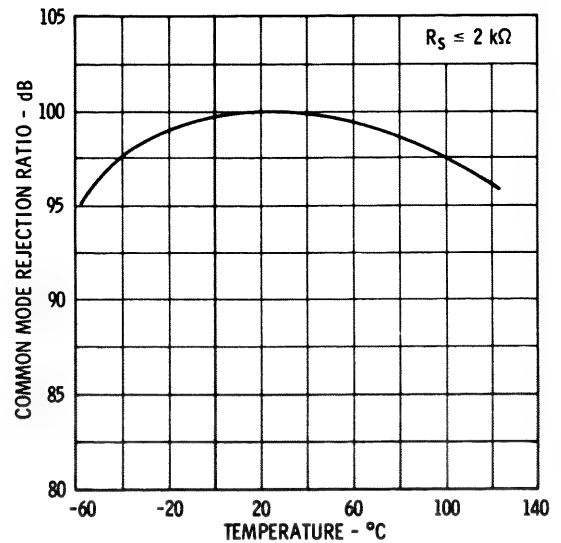
Fig. 18 Common Mode Rejection Ratio as a Function of Ambient Temperature.

$10 \, \mu V/V$ over the $-55°C$ to $+125°C$ temperature range, as can be seen from Figures 17 and 18. Due mainly to internal capacitance effects, the common mode rejection ratio of the amplifier falls off at high frequencies. Since the capacitance of the input stage has more effect with high source impedance, the rejection ratio is also a function of the circuit impedance. Figure 19 illustrates this relationship; the plot shows that excellent common mode rejection can be obtained at frequencies up to 1 MHz if low source resistances are used.
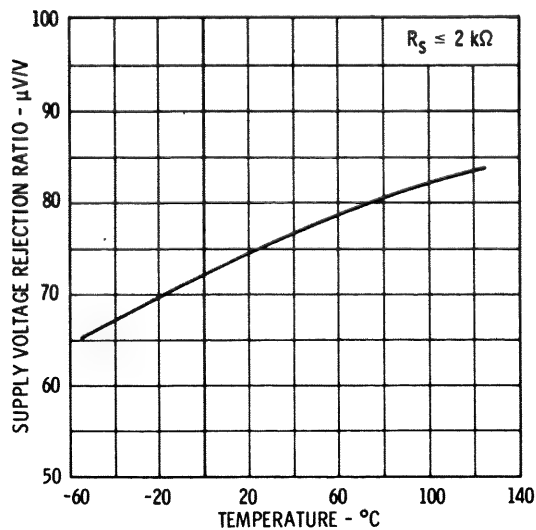
Fig. 19 Common Mode Rejection Ratio as a Function of Frequency.
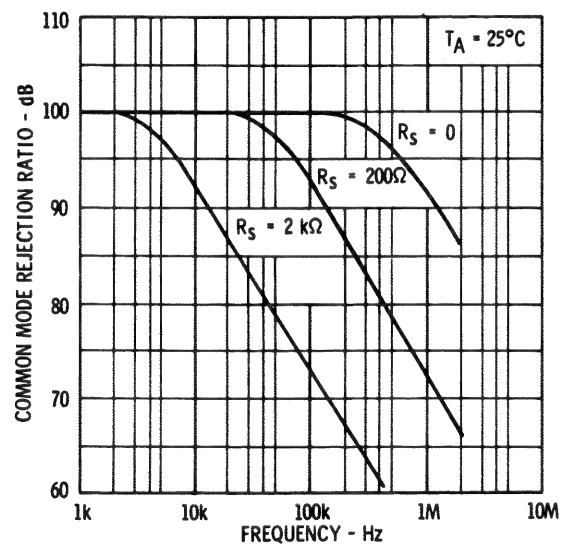
Fig. 17 Supply Voltage Rejection Ratio as a Function of Ambient Temperature.

The common mode rejection ratio is relatively independent of supply voltage. The maximum negative common mode range, however, does vary with supplies, as shown in Figure 20. The positive common mode limit remains constant since it is determined by the collector voltage of the input transistor, which is one V_{BE} above ground.

42
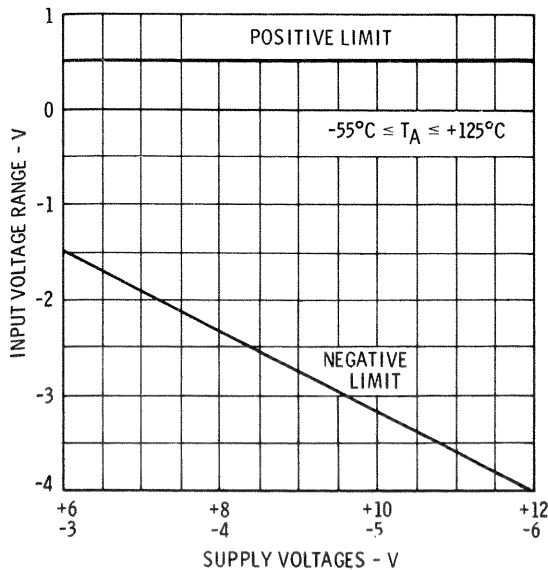
Fig. 20 Input Voltage Range as a Function of Supply Voltages.
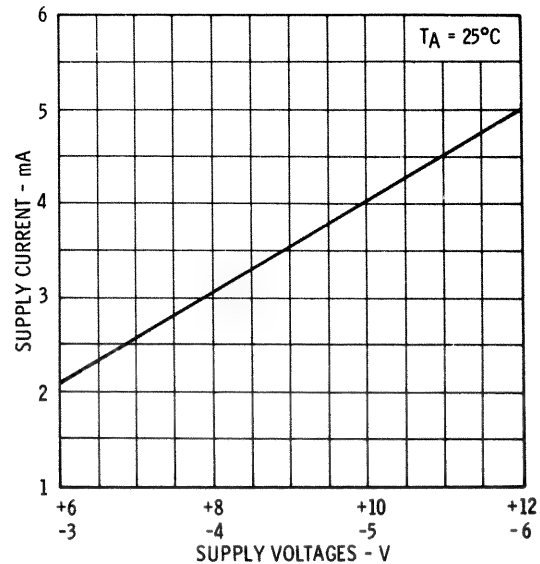
Fig. 22 Supply Current as a Function of Supply Voltages.

The effects of temperature and voltage upon the power supply current requirements of the amplifier are given in Figures 21 and 22. The curves apply to both positive and negative currents, as they are practically equal under quiescent conditions.

The input-referred noise voltage and noise current generated by the $\mu A702A$ over a frequency range of $10\,Hz$ to $1\,MHz$ are given in Figures 23 and 24. It may be seen from these graphs that at lower frequencies a $1/f$ (flicker noise) relationship dominates. As the frequency is increased, the curves level to an approximately constant value of noise energy which is due to shot noise only. The cross-over frequency, where the separate noise components contribute equally to the total noise, is about $5\,kHz$ for noise voltage and $80\,kHz$ for noise current.

Fig. 21 Power Supply Current as a Function of Ambient Temperature.

Fig. 23 Input Referred Noise Voltage for One Cycle Bandwidth as a Function of Frequency.
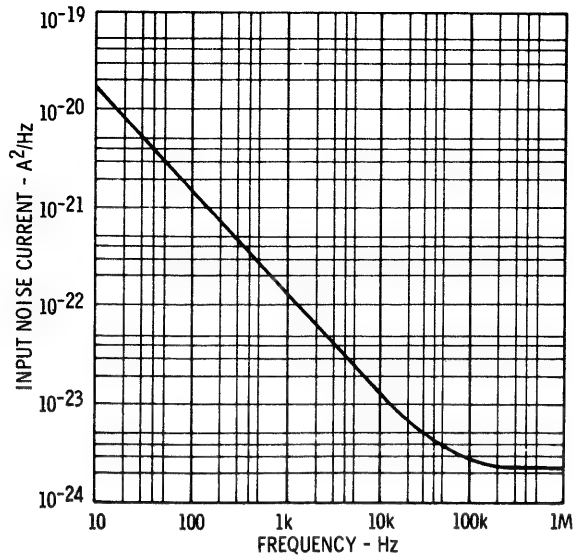
Fig. 24 Input Referred Noise Current for One Cycle Bandwidth as a Function of Frequency.

By comparing the noise voltage values with that contributed by the noise current flowing through the signal source resistance, R_S, it can be seen that if $R_S \leq 200\Omega$, the noise current contribution can be ignored; and if $R_S \geq 20\ k\Omega$, the noise current dominates and the noise voltage can be ignored. Figure 25 gives contours of constant noise figure as a function of frequency and source resistance. As the source resistance increases, so does the bandwidth over which the $1/f$ relationship predominates.
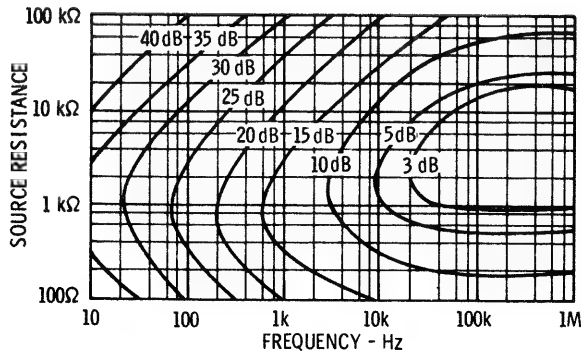
The noise contributed by an amplifier within a system depends upon the amplifier noise parameters, the source resistance, and the effective bandwidth. Figure 26 shows the total input-referred noise voltage of the μA702A as a function of source resistance for various passbands; the same information plotted in terms of noise figure is given in Figure 27. As the amplifier cutoff frequency is increased, the optimum source resistance for which minimum noise figure is obtained also increases from about $1\ k\Omega$ to $3k\Omega$. Minimum over-all noise figure is obtained with the wider bandwidths since, in this case, the additional effect of the $1/f$ noise has the least influence.
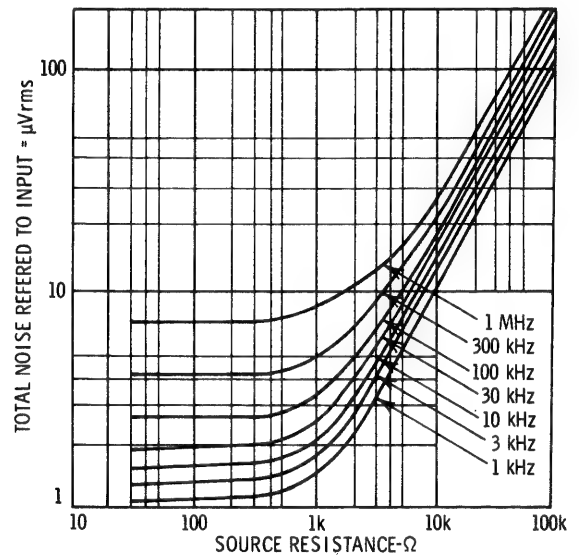
Fig. 26 Total Input Referred Noise as a Function of Source Resistance and Bandwidth.

Fig. 25 Noise Figure Contours.
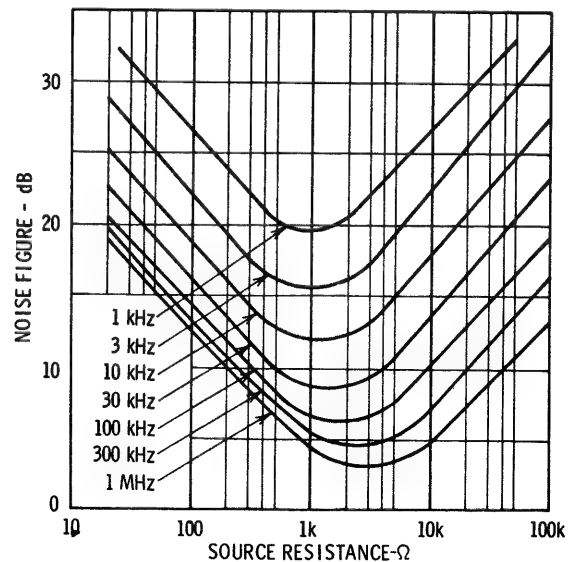
Fig. 27 Noise Figure versus Source Resistance and Cut-Off Frequency.

FREQUENCY COMPENSATION

The open-loop gain and phase responses of a typical μA702A amplifier are shown in Figure 28, including a straight-line approximation of the actual curve. The gain rolls off at the 1-*MHz* first break-frequency with a slope approaching 6 dB/octave; a second break occurs at approximately 4 *MHz*, and a third break at 40 *MHz*. The 180-degree phase shift frequency is about 14 *MHz*, so up to 34 dB of feedback may be applied without oscillation. It would not be practical to use this much feedback, however, as it is inevitable that the 180-degree phase shift will be exceeded by minor deviations in the amplifier or external circuitry. Therefore, the limiting phase for maximum feedback should be chosen less than 180 degrees by some definite margin to allow for variations in amplifier and circuit parameters.
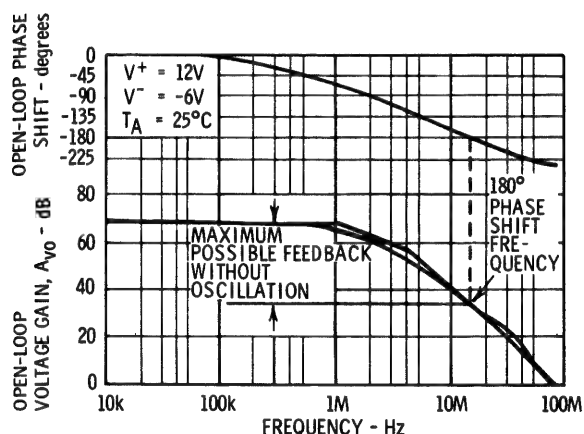
Fig. 28 Typical Open-Loop Gain and Phase Shift of the μA 702A.

A satisfactory circuit should have a minimum phase margin of about 45 degrees (less than 3 dB peaking in the closed-loop response). This reduces to 20 dB the amount of feedback that can safely be applied to the basic amplifier.

Since the amplifier response is limited by internal capacitances, little can be done to increase the amount of feedback without purposely narrowing the open-loop bandwidth. The simplest way of designing a feedback amplifier that is stable with large amounts of feedback is to shunt some signal point in the circuit to ground with a single, relatively large capacitor. If the roll-off due to this capacitor begins at a low enough frequency, the loop gain can be made less than unity before other circuit elements introduce additional phase shift. Since the maximum phase shift associated with a single R-C network is 90 degrees, the circuit cannot become unstable.

A point within the μA702A has been made available to facilitate this method of bandwidth narrowing (refer to the schematic diagram of the amplifier shown in Figure 3): a capacitor connected from the lag compensation terminal to ground attenuates the high frequency signals at the base of Q_7, thereby giving the necessary roll-off in response. Figure 29 shows the open-loop response of an amplifier using this frequency compensation, and gives curves for various closed-loop gains.
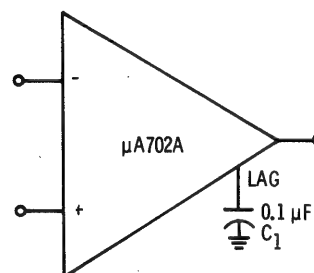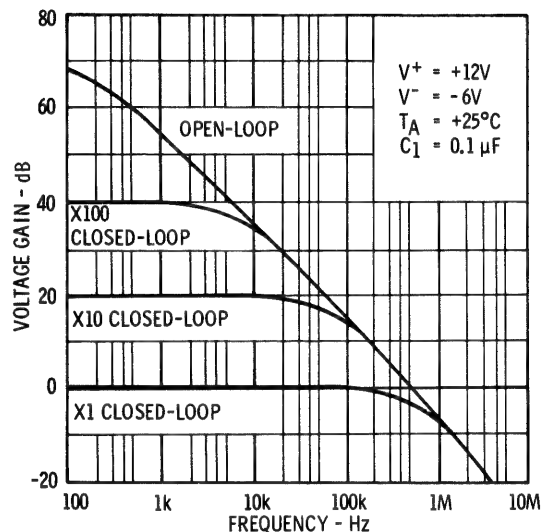

Fig. 29 Frequency Response of the μA 702A with Simple Lag Compensation.

As the closed-loop circuit cannot supply more gain than is available from the amplifier itself, the closed-loop response intersects and follows the open-loop gain curve at high frequencies, as in Figure 29. Clearly, this circuit does not give maximum closed-loop bandwidth. It is ideal for DC applications, however, since frequencies above a few hundred *Hz* are ordinarily of little interest. The early roll-off in high-frequency gain reduces the broad-band noise and makes the circuit less susceptible to any instability caused by capacitive loading or stray capacitances in the feedback circuitry.

Maximum feedback over wide bandwidths can be obtained by using the natural roll-off of the amplifier to provide part of the compensation. This technique is illustrated by the circuit and loop-gain response shown in Figure 30. The series R-C compensation network gives a roll-off in loop gain beginning at some lower frequency and breaking out at the natural roll-off frequency of the amplifier. The amplifier internal roll-off then provides the additional attenuation necessary to bring the loop gain through unity with an adequate phase margin. This scheme gives the widest possible bandwidth for any value of closed-loop gain.
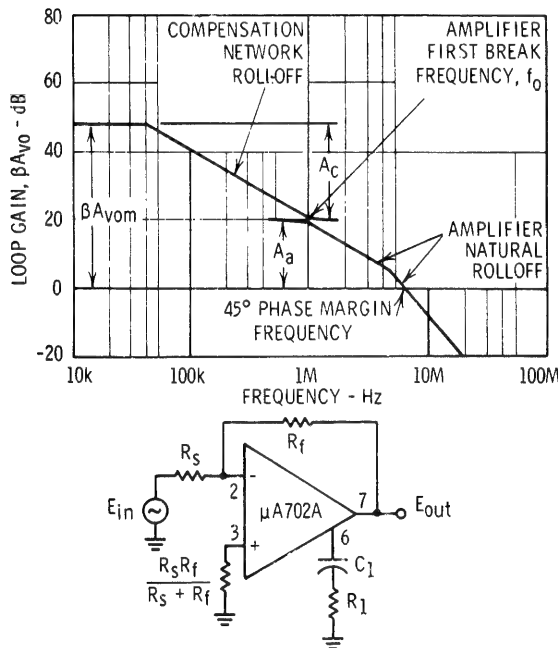
Fig. 30 Compensation for Maximum Bandwidth with Lag Network.

The values of the compensation components depend upon the loop gain, phase margin, and amplifier internal characteristics. The attenuation in loop gain from the compensation network is equal to the ratio of the internal resistance at the compensation terminal and the series compensation resistor; thus

$$A_c = \frac{R_i}{R_1} \tag{11}$$

where

A_c = attenuation in loop gain from compensation network

R_i = amplifier internal resistance at the lag compensation terminal

The total attenuation from both compensation and amplifier roll-offs must be equal to the low-frequency loop gain

$$\beta A_{vom} = A_c A_a \tag{12}$$

where

βA_{vom} = magnitude of low-frequency loop gain

A_a = attenuation in loop gain from the amplifier internal roll-off for a given phase margin

Therefore, the required value of compensation resistor is

$$R_1 = R_i \left(\frac{A_a}{\beta A_{vom}} \right) \tag{13}$$

The breakout frequency of the compensation network response should be made equal to the amplifier natural roll-off frequency for maximum feedback bandwidth, hence the value of the compensation capacitor is

$$C_1 = \frac{1}{2\pi f_o R_1} \tag{14}$$

where

f_o = first break frequency of the open-loop response

A generalized feedback circuit for the amplifier is shown in Figure 31. Single-ended signals may be applied to either input terminal if the resistor at the unused input is returned to ground. For minimum DC offset at the output, the total DC resistance to ground from each input should be equal. The loop gain for the circuit of Figure 31 is given by

$$\beta A_{vom} = \left(\frac{1}{1 + \frac{R_f}{R_s}} \right) \left(\frac{A_{om} R_{in}}{R_{in} + 2\frac{R_f R_s}{R_f + R_s}} \right) \tag{15}$$
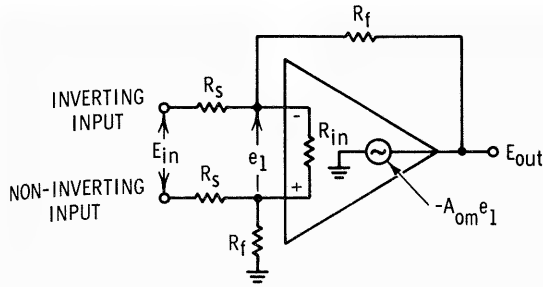
Fig. 31 General Feedback Circuit.

$$R_1 = 20 \ (1 + R_f/R_s) \ \Omega \qquad (17)$$

$$C_1 = \frac{0.01}{1 + R_f/R_s} \qquad \mu F \qquad (18)$$

This compensation will give stable closed-loop gain for the full production distribution of units.

Examples of the closed-loop response obtained using the recommended frequency compensation are given in Figure 32. The small-signal bandwidth
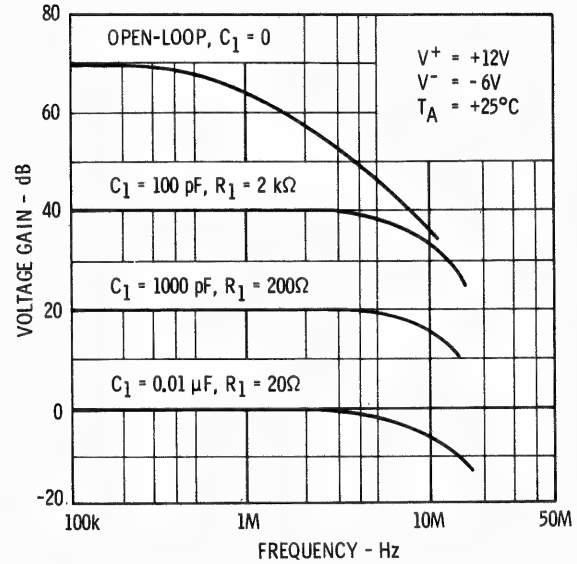

Fig. 32 Frequency Response for Various Closed-Loop Gains (Lag Compensation).

where

A_{om} = open-loop low-frequency gain measured with zero source resistances

R_{in} = input resistance

Equation (15) shows that the open-loop gain is decreased by source resistances that are larger than the amplifier input resistance. If the widest possible bandwidth is desired, this will affect the values of the compensation components. However, since R_{in} varies greatly with temperature, it is best to design the compensation network assuming that the loop gain is maximum; this ensures stability for all conditions — at the cost of some bandwidth — with high circuit resistances. This is also important in that high circuit resistances make stray capacitances more dominant. Therefore, using Eqs. (13) and (15), and assuming that

$$R_{in} >> 2 \frac{R_s R_f}{R_s + R_f}$$

the expression for the compensation resistor becomes

$$R_1 = R_i \frac{A_a}{A_{om}} \left(1 + \frac{R_f}{R_s}\right) \qquad (16)$$

Since variations in the terms R_i, A_{om}, and A_a are correlated to some degree in an integrated circuit, a compensation network design using individual limits for these parameters would be unnecessarily restrictive. It is better to specify the compensation taking the entire quantity $R_i \ (A_a/A_{om})$ as a single variable. Thus, the distribution of this quantity, rather than the distributions of the separate terms, should be used in determining the values of the compensation components. Measurement of a large number of circuits under varying conditions of feedback has shown that the following design equations are optimum for most applications:

can be expected to vary from 4 *MHz* to 10 *MHz* with less than 3 dB of peaking, depending upon the particular unit. For maximum bandwidth, the source and feedback resistors should be kept as small as possible. High resistances reduce the bandwidth because of finite amplifier input resistance and stray capacitance shunting the feedback resistor. If maximum bandwidth is not required, additional stability margin can be obtained by reducing R_1 and increasing C_1.

The frequency response of the μA702A is primarily a function of the collector-base capacitances of the integrated transistors, resistance values, and stage gains. Since these parameters are temperature-sensitive, the bandwidth will change with temperature. Even though the absolute value of the bandwidth varies, the ratios between the break frequencies stay fairly constant, and therefore the phase margin does not change appreciably.

Thus, the circuit will be stable over wide temperature ranges. The change in closed-loop bandwidth with temperature is approximately $-0.5\%°C$ for low source resistances, as shown in Figure 33. With high source resistances, the bandwidth variation is offset by the change in loop gain due to the temperature coefficient of the amplifier input resistance; hence, the relative change in closed-loop bandwidth is much less.
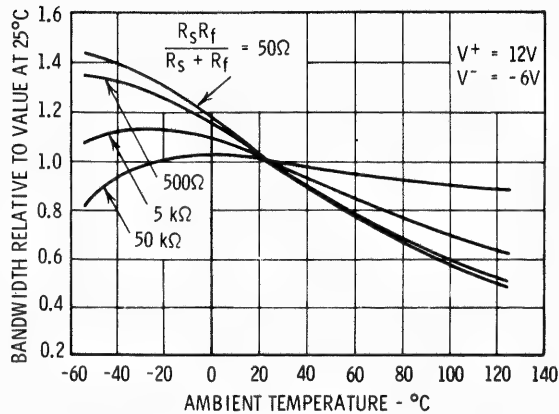

Fig. 33 Effect of Temperature on Response of a Lag-Compensated Amplifier.

The effect of negative supply voltage on bandwidth is shown in Figure 34. If much variation in voltage is expected, the values of the compensation network components, as given in Eqs: (17) and (18), should be adjusted to give an adequate phase margin for the largest supply voltage anticipated. Dividing R_1 and multiplying C_1 by a factor of 1.5 to 2 will guarantee stability for voltages up to $-9\,V$. The bandwidth is not significantly affected by the positive supply voltage.
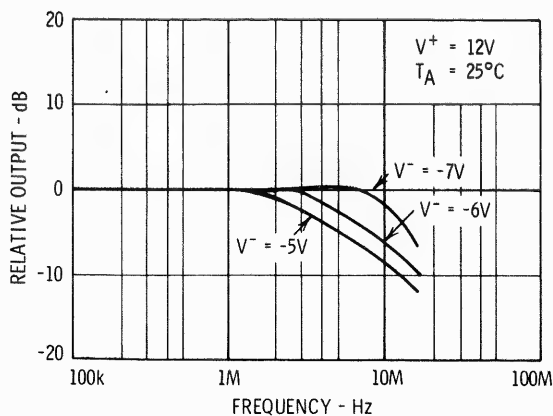
Fig. 34 Effect of Negative Supply Voltage on Response of a Lag-Compensated Amplifier.

Excessive capacitive loading at the output of a feedback amplifier may cause peaking and possible instability. The capacitance breaking with the amplifier output resistance produces additional phase shift at the unity loop gain frequency, decreasing the phase margin. Since the compensation network is at the base of the output transistor, it reduces the high-frequency output impedance and makes the circuit less sensitive to capacitive loading. The effect of load capacitance on a unity-gain amplifier is shown in Figure 35. Selection of the compensation network values for stability with high capacitive loading may be achieved in the same manner as for supply voltage variations.
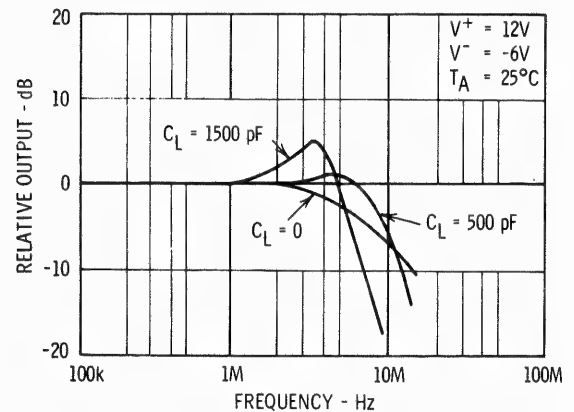
Fig. 35 Effect of Load Capacitance on Response of a Unity-Gain Lag-Compensated Amplifier.
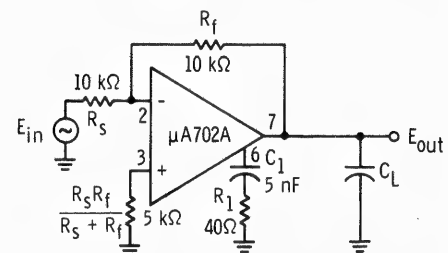
A disadvantage of frequency compensation near the output of the amplifier is that the maximum high-frequency output voltage swing is reduced by the compensation network. Figure 36 shows how the maximum sinusoidal output swing varies with frequency for different lag compensation networks. Because there is a limit to the amount of current available at the compensation terminal to charge the capacitor, the output swing falls with increasing frequency and amounts of compensation. Overdriving the stage results in a triangular output waveform; the maximum rate-of-change of output, or slew rate, is given in Figure 37 for the compensation networks determined from Eqs. (17) and (18) as a function of closed-loop gain.
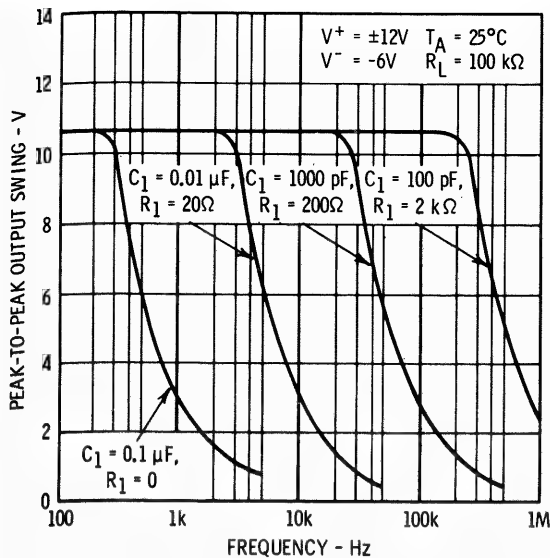
Fig. 36 Output Voltage Swing as a Function of Frequency for Various Lag Compensation Networks.
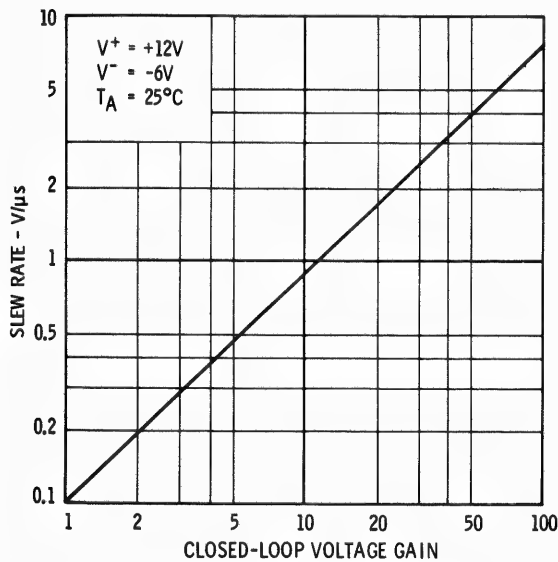

Fig. 37 Slew Rate as a Function of Closed-Loop Voltage Gain (Lag Compensation).

LEAD/LAG COMPENSATION

An additional compensation terminal has been included on the $\mu A702A$ to provide a leading phase shift in the open-loop response and thus increase the useful bandwidth by about two octaves. Connecting a small capacitor across the lead-lag frequency compensation terminals (see Figure 3) effectively moves the second break point in the open-loop frequency response to a much higher frequency. This gives the frequency response

shown in Figure 38; about 30 dB of feedback may be used for a 45-degree minimum phase margin. Thus, 10 dB more feedback can be obtained than for lag compensation only, and the bandwidth is about four times as large. The optimum value for the lead compensation capacitor is about 50-100 pF.
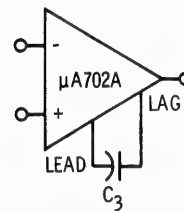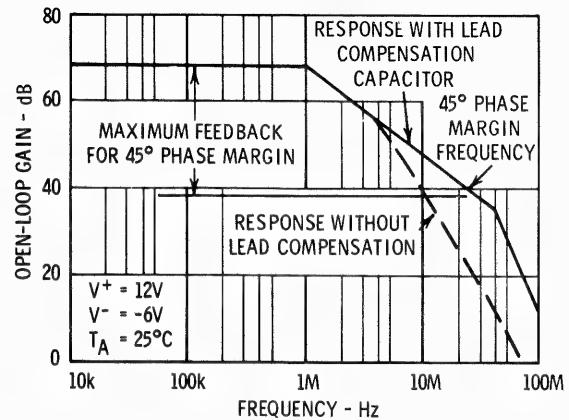
Fig. 38 Open-Loop Response of $\mu A702A$ with Lead Compensation.

Closed-loop gains less than 40 dB require additional lag compensation. In order to obtain a high slew rate, the compensation should be placed at a low-level point in the circuit where the required rate-of-change of signal across the compensation capacitor is small. Connection of the network across the input terminals, as in Figure 39, permits the full output swing capability of the amplifier to be utilized to frequencies in excess of 500 kHz. The attenuation in loop gain from the input compensation network is given by
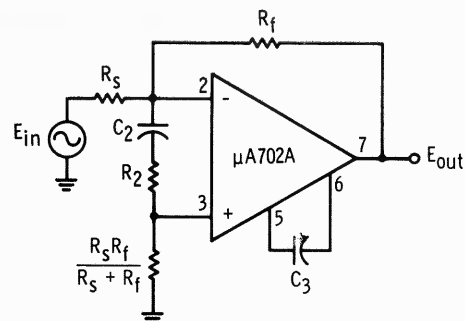
Fig. 39 Amplifier with Lead-Lag Compensation.

$$A_c = \left(\frac{2\frac{R_s R_f}{R_s + R_f}}{R_2} \right) \left(\frac{R_{in}}{R_{in} + 2\frac{R_s R_f}{R_s + R_f}} \right) \qquad (19)$$

for

$$R_{in} >> R_2 << 2\frac{R_s R_f}{R_s + R_f}$$

From Eqs. (12), (14), (15), and (19), the compensation components are

$$R_2 = 2R_f \frac{A_a}{A_{om}} \qquad (20)$$

$$C_2 = \frac{A_{om}}{4\pi f_o R_f A_a} \qquad (21)$$

These expressions show that input compensation gives another advantage in addition to full output swing capability: the compensation is independent of the amplifier input resistance. This means that changes in input resistance will not affect the closed loop bandwidth. Also, there will be less spread in bandwidth from unit to unit since the variations caused by R_i are eliminated. The experimentally determined optimum design equations for the lag compensation components are:

$$R_2 = 20R_f \quad \Omega \qquad (22)$$

$$C_2 = \frac{0.01}{R_f} \quad \mu F \qquad (23)$$

where R_f is in $k\Omega$.

Examples of the closed-loop response obtained using both lead and lag compensation are shown in Figure 40. The small-signal bandwidth can vary from 12 MHz to 40 MHz, depending upon the open-loop gain and bandwidth of the particular unit. With the large bandwidths possible using the compensation, it is extremely important to keep the impedance levels low to avoid undesirable effects from stray capacitance. Only 0.5 pF across a 30-$k\Omega$ feedback resistor, for example, will reduce the bandwidth to 10 MHz.
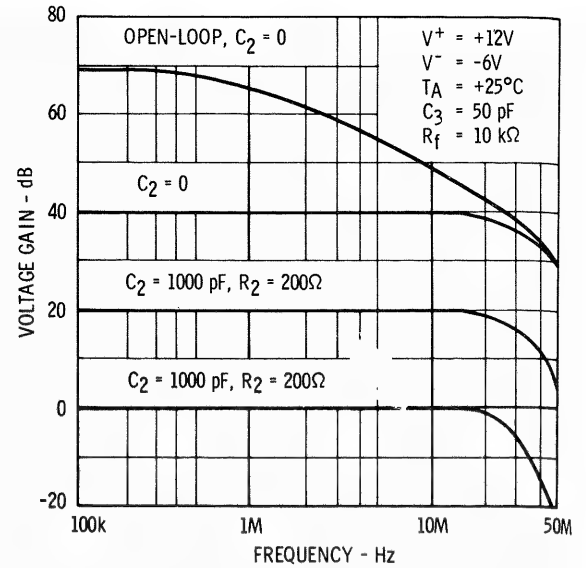
Fig. 40 Frequency Response for Various Closed-Loop Gains (Lead-Lag Compensation).

The slew rate and output voltage swing characteristics are given in Figures 41 and 42. The load capacitance on the amplifier must be kept low to obtain this performance; otherwise, the load capacitance becomes the limiting factor in determining slew rate.
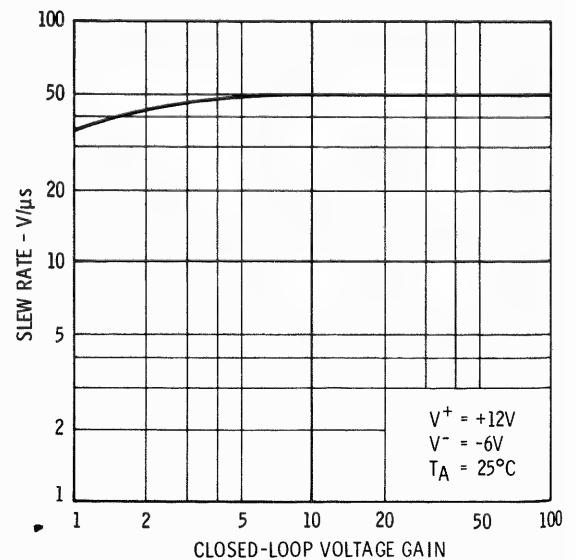
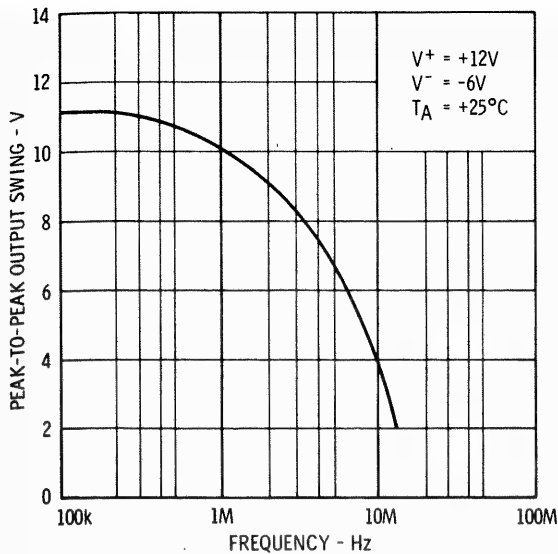Fig. 41 Slew Rate as a Function of Closed-Loop Voltage Gain (Lead-Lag Compensation).

Fig. 42 Output Voltage Swing as a Function
of Frequency with Lead-Lag
Compensation.

Fig. 44 Effect of Negative Supply Voltage on
Response of a Lead-Lag Compensated
Amplifier.

The relative change of bandwidth with temperature is shown in Figure 43. The independence of bandwidth from source and input resistances is clearly evident. The effect of negative supply voltage, Figure 44, is about the same as for output lag compensation.
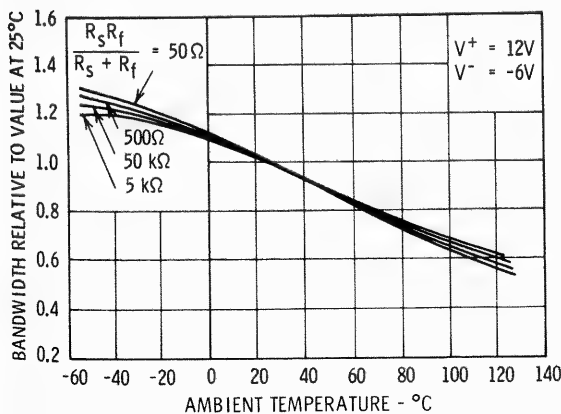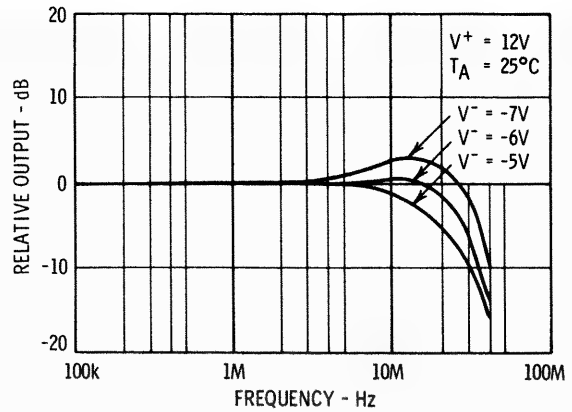
Since the bandwidth is so much larger, however, the circuit is considerably more sensitive to capacitive loading. The peaking due to load capacitance (see Figure 45) may be reduced by shunting the feedback resistor with a very small capacitor or by increasing the lead capacitor to about 500 pF. This is effective if the load capacitance isn't too large and is relatively constant. For load capacitances greater than 100 pF, it is best to increase the phase margin by dividing R_2 and multiplying C_2 by a factor of 2 or more.

Fig. 43 Effect of Temperature on Response of a
Lead-Lag Compensated Amplifier.
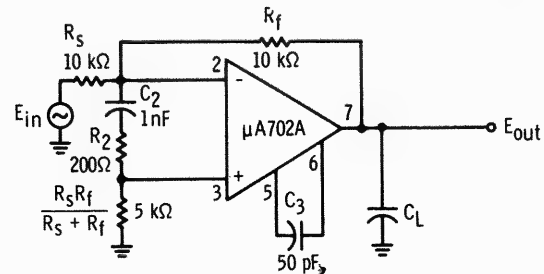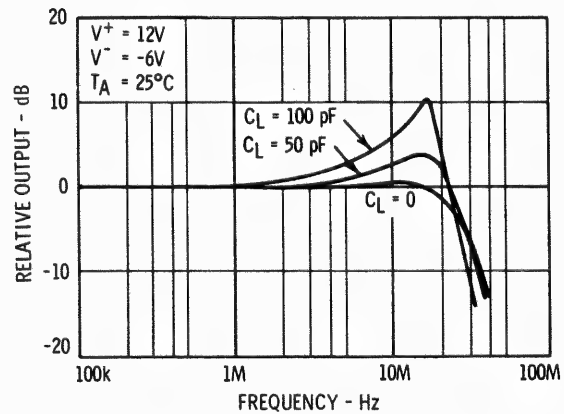
Fig. 45 Effect of Load Capacitance on Response
of a Unity-Gain Lead-Lag Compensated
Amplifier.

It should be pointed out that the noise characteristics of the amplifier are also dependent upon the positions of the compensation network. The best characteristics are obtained with the compensation at the output, since the noise and signal are attenuated to the same extent. Compensation at the input, on the other hand, makes the signal-to-noise ratio worse because the R-C compensation network acts only on the signal, while not attenuating the noise introduced by the amplifier. It is possible to reach a compromise between noise and slew rate by using R-C networks at both input and output; the roll-off points of the two networks should be chosen to synthesize a composite 6dB/octave function similar to that of Figure 30. The proportion of compensation contributed by each network is selected according to the relative importance of noise and slew rate in the particular application considered.

STABILITY PRECAUTIONS

Most oscillation problems encountered in the use of the μA702A are caused by poor circuit layout and inadequate power-supply bypassing. It should be kept in mind that the amplifier is potentially unstable up to almost 100 MHz since it has greater than unity gain below this frequency. Therefore, in connecting the amplifier to the outside world, care should be taken to make sure parasitic oscillations do not occur. This applies to DC circuits as well as to 30-MHz amplifiers.

As with any high-gain feedback amplifier, power-supply bypassing is of particular importance. Positive feedback through excessive impedance in the power supplies may cause very high frequency internal oscillations in the amplifier. This type of oscillation generally makes itself known through unreasonable DC performance; i.e., the output null may be extremely sensitive to power-supply voltage changes, common-mode inputs, or signal polarity. Bypassing the power supplies at the amplifier socket with 0.01 to 0.1 μF low-inductance capacitors will eliminate this source of possible instability.

If the circuit layout is not neat, stray capacitance from the output to the inputs may cause excessive peaking in the response or even oscillations. Even with a neat layout, the unavoidable stray capacitance may cause problems if the source resistances are high. This may be cured by using an inverting amplifier configuration and bypassing the non-inverting input to ground with 50 to 100 pF. If the compensation network is at the input, however, this remedy cannot be used, but in this case the network reduces the effective input impedance so that stray capacitance is less critical.

Some difficulty may be experienced when thermal tests are performed on the amplifier. The capacitive coupling between the long leads from the thermal test jig to the external circuit components can make the amplifier hard to stabilize. Under these circumstances, it is mandatory to keep the leads as short as possible, with connections to the external circuitry made immediately outside of the temperature chamber. The frequency compensation network should be very conservative, and, if necessary, may be mounted directly on the amplifier socket with the power-supply bypasses. The output should be monitored with a high-gain, wideband oscilloscope to make sure the setup is not oscillating before proceeding with the measurements.

LOW-VOLTAGE OPERATION

The compensation components for operation at +6, −3 V power supplies are readily calculated from the +12, −6 V values. The open-loop frequency response and internal impedances are fairly constant with supply voltage; the only important change is that the open-loop voltage gain is about 12 dB less. Hence, the proper values for the lag networks may be found by multiplying R and dividing C by a factor of 4. The 50-pF lead compensation capacitor remains the same. This procedure yields essentially the same bandwidths and stability margin as for high-voltage supplies.

PREVENTION OF INPUT LATCH-UP CONDITIONS

From the circuit diagram of Figure 3, it can be seen that if the input voltage on the inverting input terminal exceeds $2V_{BE}$, the input stage transistor will saturate. If this happens, the circuit will still have a gain, but the inverting input will now be a non-inverting input. It is important, therefore, to ensure that large output swings cannot saturate the input stage through the feedback network, as this can result in positive feedback and a latch-up condition. If the feedback path from the output has a sufficiently low impedance, the resulting current flowing through the collector-base junction of Q_3 and the emitter-base junction of Q_4 can reach levels at which permanent damage may occur.

To get into a latch-up condition, the maximum common-mode voltage on the input terminal must be exceeded, and enough current must be supplied to saturate the input stage (a current nearly equal to the collector current of Q_1 would be required). In general, this is not a problem if the closed-loop gain is greater than 10 or if the feedback resistor between the output and inverting input terminals is greater than $50\,k\Omega$. If there is any question, the latch-up condition can be positively eliminated by connecting a limiting diode between the inverting input terminal and ground, as shown in Figure 46(a).

To determine whether a certain feedback configuration can produce latch-up, the equivalent circuit in Figure 46(b) can be used. The maximum output voltage of the amplifier is about $1\,V$ less than the positive supply voltage (V^+); the minimum current that will saturate the input stage is $200\mu A$, and the minimum input voltage for saturation is $0.5V$. Therefore, sufficient conditions for elimination of latch-up are

$$\frac{R_2(V^+ - R_1 I_{sat} - 1)}{R_1 + R_2} < 0.5\,V \qquad (24)$$

A circuit that is potentially prone to latch-up conditions is the integrator shown in Figure 47. If
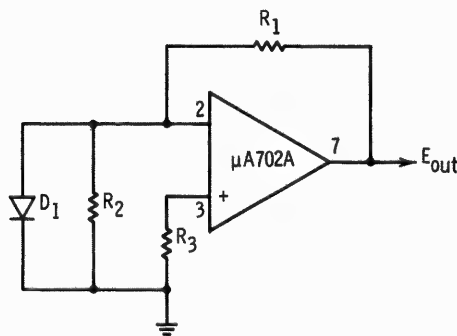
(a) Feedback Circuit and Limiting Diode
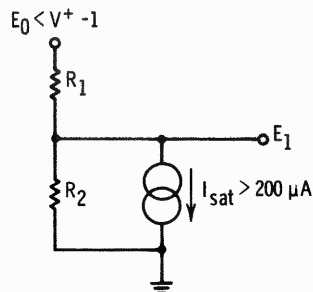
(b) Equivalent Circuit for Latching Condition

Fig. 46 Circuits Used to Determine Whether Limiting Diode is Needed to Prevent Possible Latch-Up Condition.
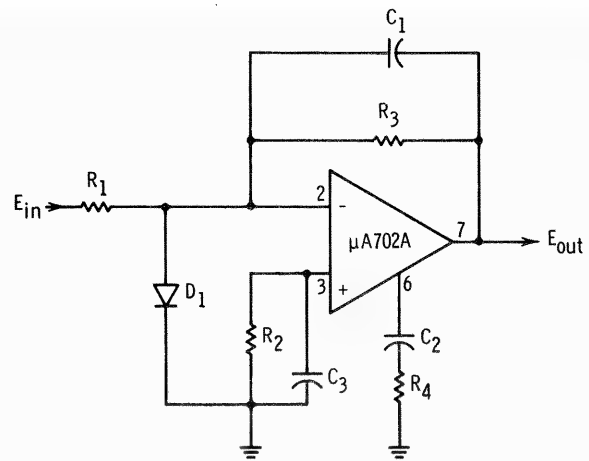
Fig. 47 The μA 702A Connected as an Integrator, Including an Input Clamping Diode to Prevent Latch-Up.

a clamping diode (D_1) is not used on the input, it is possible for an output transient to drive the amplifier beyond its positive common-mode limit through the integrating capacitor C_1. This can result in latch-up of the amplifier wherein excessive current is driven from the output emitter-follower through the collector-base junction of Q_2 and the emitter-base junction of Q_4. This current can reach destructive levels if the integrating capacitor is more than ten times larger than the frequency compensating capacitor on pin 6. The clamping diode, however, completely eliminates the problem by preventing latch-up, and a sufficiently large compensating capacitor will limit the peak diode current to a reasonable value.

Another circuit with a very similar problem is shown in Figure 48. Diodes can be connected across
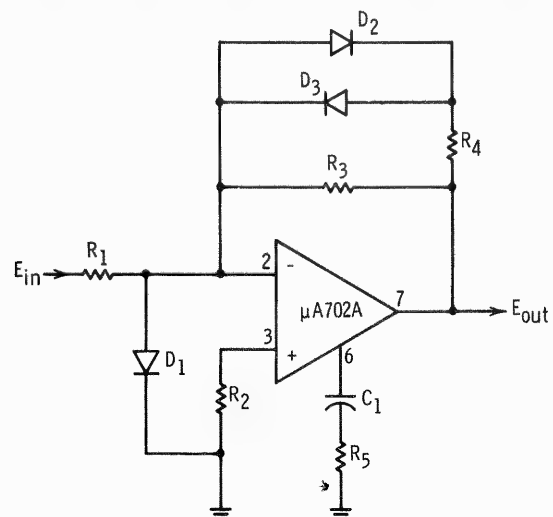

Fig. 48 Circuit Showing Use of Input Clamping Diode to Prevent Larch-Up with Diode-Feedback Circuit.

the feedback resistor R_3 as indicated in the schematic to give a nonlinear (clipping) transfer characteristic. As with the previous circuit, however, it is possible to exceed the input common-mode range of the amplifier with an output transient if a limiting diode is not used on the input. It is also advisable to use a limiting resistor (R_4) to prevent excessive current through D_1.

GENERAL CIRCUIT PRECAUTIONS

The previous section described how input latch-up and consequent circuit malfunction may be guarded against by the use of diodes at the input terminal. A diode used in a similar configuration is a useful means of protecting the input where there is risk of large input transients. Figure 44
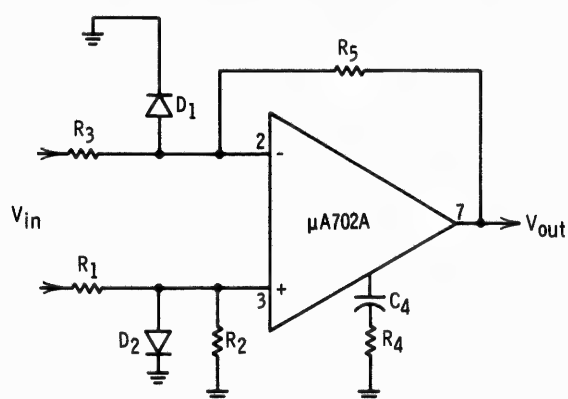
Fig. 49 Input Transient Protection.

shows an example where the μA702A, used as a differential amplifier, is protected against positive transients at both inputs. Additional diodes connected with reversed polarity would provide negative transient protection, although as can be seen from the specifications, these would not normally cause damage unless they exceeded $-5V$ in magnitude.
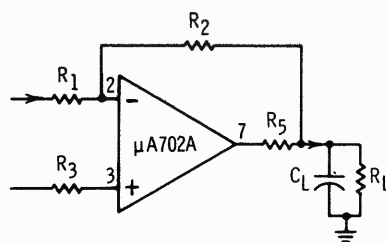
Certain precautions should be observed to ensure that no damage to the output stage occurs. As indicated by the data sheets, peak output current should not exceed 50 mA. This does not necessarily allow the output to be short-circuited with safety, even for short periods, since the current may well exceed this value, with consequent overheating and damage of the output transistor.

Figure 50 shows a circuit configuration that could result in excessive current from the amplifier. Unless a resistor (R_2) is inserted in series with the base of the following transistor, it is possible for the large output swing of the amplifier to saturate the transistor and drive a large current through the base-emitter junction to ground.
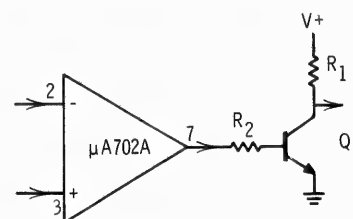
Fig. 50 Output Current Limiting.

There is also a possibility that excessive peak current may be delivered by the amplifier under certain conditions if the load is highly capacitive. In this case, the circuits shown in Figure 51 may be used for protection. In Figure 51(a), resistor R_5 in series with the output limits the peak current charging C_L. Bearing in mind that the typical open-loop internal impedance of the amplifier is 200Ω, an additional resistor of 270Ω should provide adequate protection for worst-case conditions. Another approach is shown in Figure 51(b): a capacitor with a value equal to or greater than one-tenth the value of the effective parallel load capacitance is connected between the lag compensation point and ground, thereby limiting the slewing rate to a value that prevents excessive output current. It should be noted that both the circuits restrict the bandwidth of the amplifier.

(a)
Series Resistance Limiting

(b)
Output Rise-time Limiting

Fig. 51 Peak Current Limiting with Capacitive Loads.

If the μA702A is used to drive logic circuits, it is important to limit the maximum output swing of the amplifier, both because damage might be caused to the input of the logic integrated circuits, and because excessive current might flow through the output transistor as a result of forward biasing any of the isolation PN junctions within the integrated circuit. Figure 52 shows an effective method for overcoming the above problems. The diode D_1 prevents negative excursions of the amplifier from exceeding approximately $-0.7V$ (the internal impedance of the amplifier for negative swings limits the output current to a safe value). The diode D_2 connected between the lag frequency compensation point (which is the base of the output emitter-follower) and the logic positive supply will prevent the output voltage from rising above that of the logic supply.

If the μA702A is used to drive RTL circuits, it is also necessary to insert a 640Ω resistor in series with the output. Under these circumstances, the fan-out of the μA702A is 5. A fan-out of up to 10 can be obtained by reducing the resistor at the output to 320Ω.

With the DTL family, the fan-out is limited to 1. A higher fan-out is available if a resistor is connected between the amplifier output and the power supply negative terminal. A 3.9 $k\Omega$ resistor should be used for a fan-out of 2 and a 2 $k\Omega$ for a fan-out of 3.
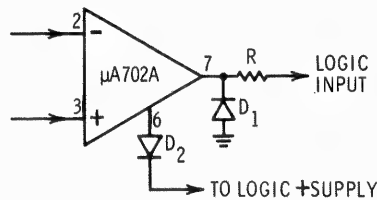
Fig. 52 Logic Compatibility.

THE µA709 HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

The µA709 is a high-gain, general purpose operational amplifier designed and constructed using the state-of-the-art techniques discussed in Chapter 2. The amplifier is intended for use in DC servo systems, high impedance analog computers, low-level instrumentation applications, for the generation of special linear and nonlinear transfer functions, and for many other general-purpose amplifier applications made feasible by the low cost and high performance characteristics of the circuit. It gives performance which is comparable to the best discrete component designs, yet it is relatively simple to build in monolithic form. It features low offset, high input impedance, large input common mode range, high gain, low power consumption and large output swing under load. The amplifier displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The suitability of the circuit for integration is indicated by the fact that it is constructed on a 55-mil-square silicon die using a six-mask Planar* epitaxial process which is nearly identical to that employed with common digital integrated circuits. A photomicrograph of an actual amplifier is shown in Figure 1.

INPUT STAGE

Darlington-input amplifiers have generally been used in microcircuits requiring high input impedance because of restrictions on maximum resistance values, which make it difficult to operate transistors at low collector currents. With DC amplifiers, the Darlington connection has the disadvantage of considerably higher offset and thermal sensitivity than a non-Darlington differential pair. In addition, input impedance and input currents vary as the square of the current gain with a Darlington connection, and so it does not provide a great performance advantage when full temperature range

*Planar is a patented Fairchild Process.
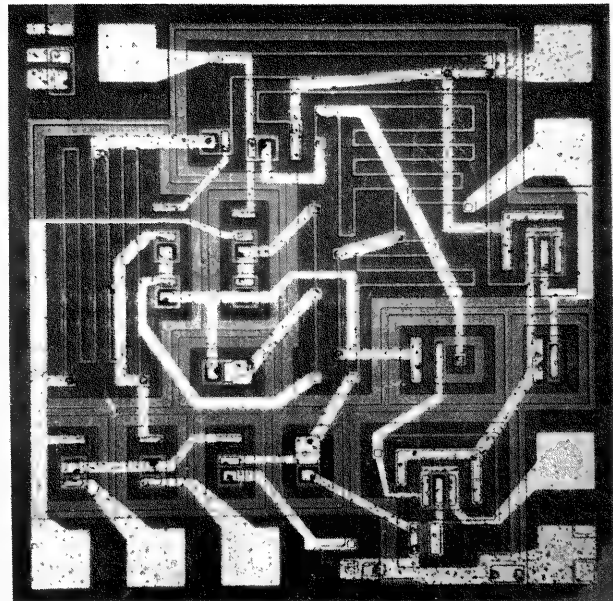
Fig. 1 Photomicrograph of the µA 709.

operation is considered. The described design is a departure from this conventional approach: the input stage is operated at low collector currents, but without requiring unusually large resistance values.

One unusual feature of the input stage is the current source for the emitters of the input transistors, shown in Figure 2. It makes use of the highly predictable difference in the emitter-base voltage of

$$\Delta V_{BE} = V_{BE10} - V_{BE11}$$

$$= \frac{kT}{q} \ln\left(\frac{I_{C10}}{I_{C11}}\right)$$

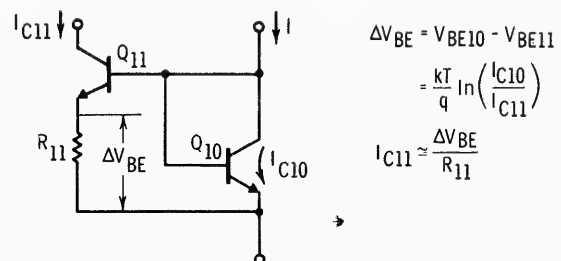$$I_{C11} \cong \frac{\Delta V_{BE}}{R_{11}}$$

Fig. 2 Simplified Schematic of Input Stage Current Source.

two identical transistors operating at different collector currents to form a microampere current source using resistances of only a few $k\Omega$.

With reference to Figure 2, a relatively large current (I) is passed through the diode-connected transistor, Q_{10}. Assuming large current gains for Q_{10} and Q_{11}, the collector current of Q_{10} will be equal to this current. The emitter-base voltage of Q_{10} is used to bias the current source, Q_{11}. The resistor in the emitter of Q_{11} determines the collector current of the device. This type of current source is described in detail in Chapter 2; but to give an example of its operation, it might be assumed that the biasing transistor (Q_{10}) is operating at 1 mA collector current and that it is desired to operate Q_{11} at 10 μA. For this ratio of collector currents, the emitter-base voltage difference between the two devices will be 120 mV at room temperature (60 mV decade). Therefore, it is only necessary to insert a 12 $k\Omega$ resistor in the emitter of Q_{11} to obtain the desired 10 μA collector current.

The differential input stage (Q_1 and Q_2) and its collector load resistors (R_1 and R_2) are shown in the complete schematic of Figure 5. The input stage operates at approximately 20 μA collector current. While the collector load resistors are relatively small for this current level, they do provide enough gain to make the effect of second stage offset small if the second stage is reasonably well balanced. Another interesting feature of this input stage is that the variation in current source current with temperature compensates almost exactly for the variation in input stage transconductance. As a result, the voltage gain holds constant, within a few percent, over the full operating temperature range of the circuit. In addition, the collector current of the current source is roughly proportional to the logarithm of the collector current of its biasing transistor. Since the collector current of the biasing transistor varies approximately as the supply voltage, the input stage operating level is practically unaffected by supply voltage changes.

SECOND STAGE

The second stage design is similar to that described in Chapter 5. A simplified schematic is shown in Figure 3. The input stage collectors are connected to the bases of the second stage transistors. The collector load resistors of the input stage, R_1 and R_2, are connected as shown. In the simplified schematic, Q_6 is the second stage amplifier, while Q_5 provides balanced biasing. Q_5 also serves
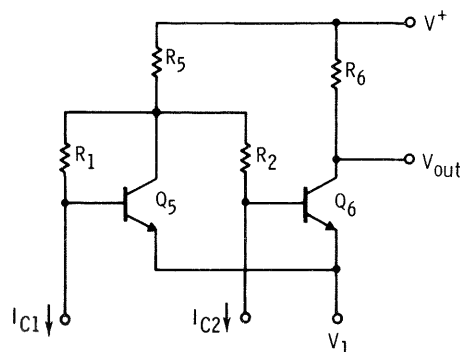
Fig. 3 Simplified Schematic of Second Stage.

as a unity gain inverter, delivering the full differential output of the input stage to the base of Q_6. This helps to minimize offset and thermal drift since the input stage has low gain because of the low-value collector load resistors. As pointed out in Chapter 5, this second stage design is extremely useful in going from a differential to a single-ended connection in that it provides excellent isolation to variations in supply voltage when R_5 and R_6 are equal.

The actual circuit employed is shown in Figure 5. A modified Darlington connection is used in the second stage to prevent loading of the input stage. This makes the second stage gain proportional to the predictable transconductance characteristic of the transistors, rather than to the current gain. A unique scheme is used to make the Darlington-connected second stage insensitive to high temperature leakages and stabilize it over the operating temperature range. This was discussed in Chapter 2, and, as is clear from Figure 4, uses the same principle as the input stage current source. The remaining details of the second stage are that an emitter-follower, Q_7, is used to keep the input stage collector currents out of the collector of Q_5. Additionally, a second emitter-follower, Q_8, is used to prevent loading of the second stage by the output stage.

OUTPUT STAGE

Level shifting to the output stage is accomplished using a lateral PNP, Q_9, which is made using what is usually an NPN base diffusion for an emitter. This is surrounded by a second base diffusion which serves as a collector. The normal NPN collector region is then the PNP base. This structure suffers from a rather wide base, displaying a low current gain (approximately 2). However, it has the distinct advantage that it can be made with the standard NPN process with no additional steps or control. The circuit is designed to operate satisfactorily with

$$\Delta V_{BE} = V_{BE5} - V_{BE15}$$

$$= \frac{kT}{q} \ln\left(\frac{I_{C5}}{I_{C15}}\right)$$

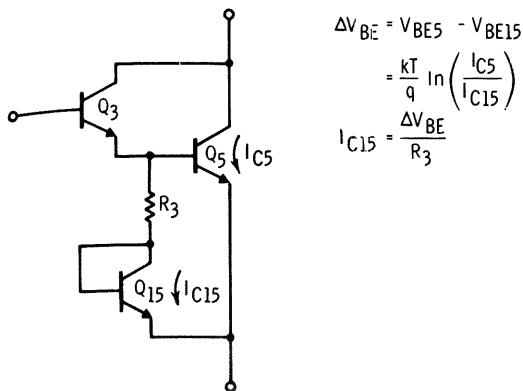$$I_{C15} = \frac{\Delta V_{BE}}{R_3}$$

Fig. 4 Schematic Illustrating Principle of the Modified Darlington Connection.

current gains lower than 0.2, and so the device presents no problem in that the PNP will work well enough as long as the junctions are good.

A complementary, class-B output stage is employed. The circuit has a built-in dead zone to prevent latch-up or runaway under overload conditions; each output transistor is positively turned off before the other is allowed to conduct. However, a

large amount of internal feedback (through R_{15}) not only gives a low output resistance but also makes the cross-over distortion almost indiscernible — even on the open loop transfer function. An additional advantage of this scheme is that the output stage quiescent current is held to a minimum, in accord with the design objective of low power consumption.

A vertical PNP is used in the output stage. This device uses the NPN base diffusion for an emitter and the P-type substrate of the integrated circuit for the collector (in the lateral PNP, this PNP action is suppressed by placing the N+ subcollector diffusion of the NPN underneath it). This PNP has a higher current gain than the lateral PNP, but it also presents no problem as far as device yields are concerned since it need only function as a diode to meet circuit requirements.

Although it is not clear from the schematic, the output stage is actually short-circuit-proof for a short period of time. This characteristic is derived from the fact that the output transistors (Q_{14}, Q_{13},
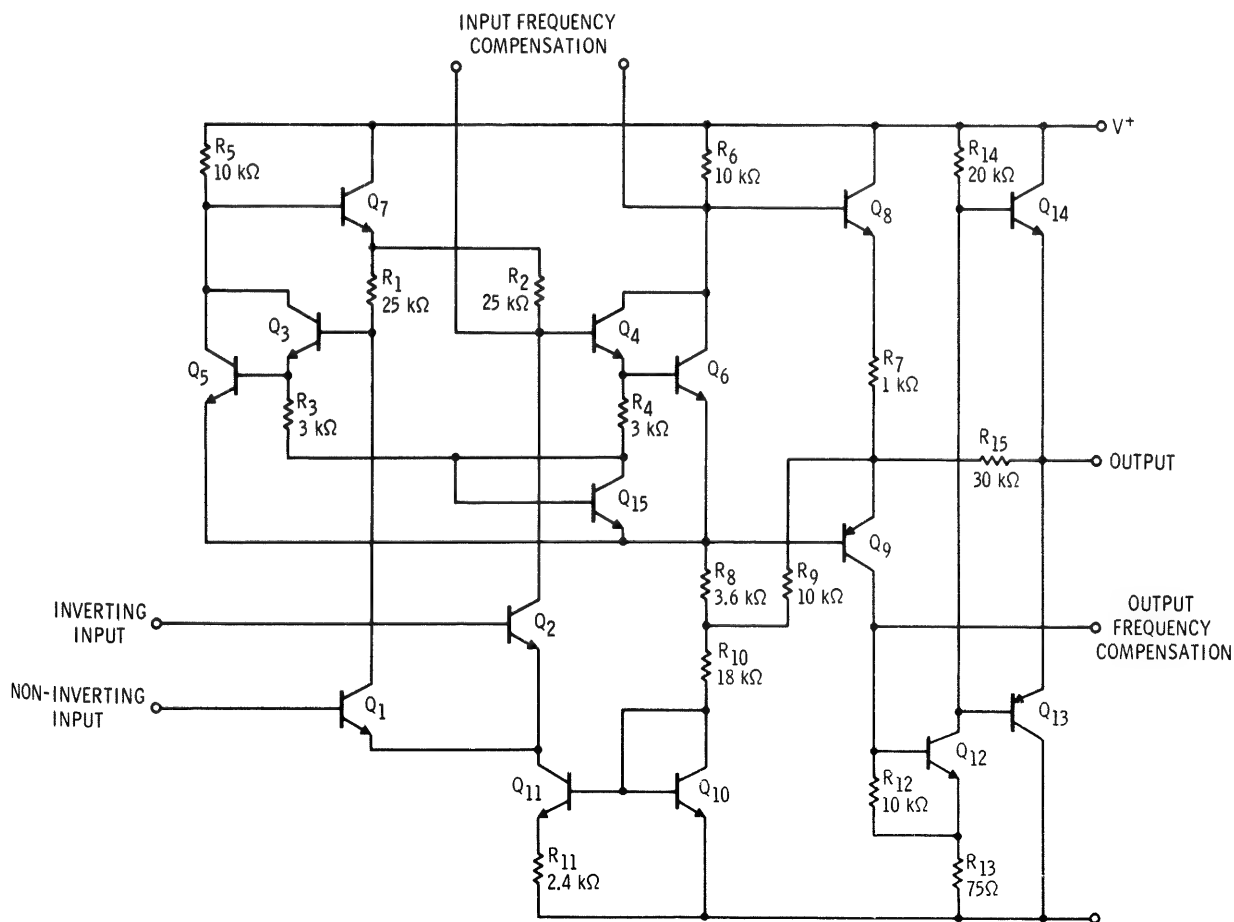
Fig. 5 Complete Schematic of the μA709

and Q_{12}) have small geometries (the whole integrated circuit is about the same size as the output transistors that would normally be used). The current gain of these devices is injection-efficiency limited at high current levels, and is relatively constant for a given process and geometry, falling off at high temperatures. As a result, this turns out to be a satisfactory method of short-duration current limiting.

Other details of the output stage are that R_{12} is used to make the circuit insensitive to leakages in Q_9 and Q_{12}. R_{13} reduces the internal loop gain of the output stage to stabilize the internal feedback. The gain of the output stage is essentially determined by the ratio of R_{15} to R_7, independent of the characteristics of the active devices.

PERFORMANCE

The versatility of the μA709 is enhanced by specification of its characteristics over a wide range of supply voltages and operating temperatures. Performance is guaranteed for supply voltages from $\pm 9V$ to $\pm 15V$, and useful performance can be obtained from $\pm 6V$ to $\pm 18V$. Symmetry of power supplies need not be maintained as long as the total voltage across the amplifier is between $18V$ and $30V$ and the inputs are operated within their common mode limits. Typical performance figures for the amplifier are summarized in Table I.

The excellent linearity and symmetry of output swing are illustrated by the voltage-transfer characteristics of Figure 6. Output voltage swing for different supplies and loading is shown in Figures 7 and 8.

As can be seen from Figure 9, the open-loop voltage gain is roughly proportional to supply voltage, and changes about 8 dB over the ± 9 to $\pm 15V$ range. The ± 2 dB variation with temperature, illustrated in Figure 10, is due primarily
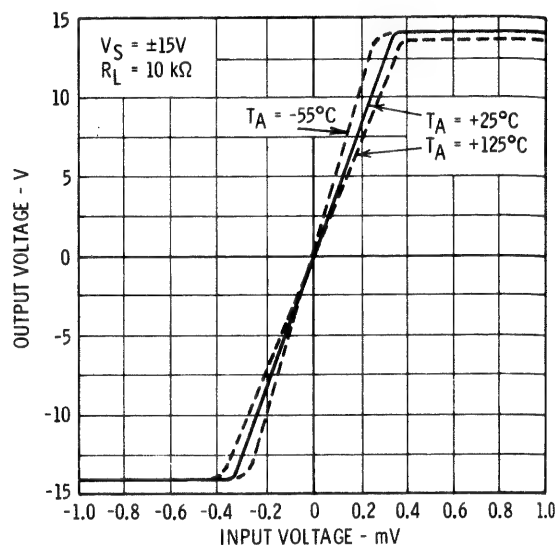
Fig. 6 Voltage Transfer Characteristic.

TABLE I
TYPICAL ELECTRICAL CHARACTERISTICS

Parameter	Conditions $(T_A = +25°C, \pm 9 \text{ V} \leqslant V_S \leqslant \pm 15 \text{ V}$ unless otherwise specified	Value	Units
Input Offset Voltage	$R_S \leqslant 10 \text{ k}\Omega$	1.0	mV
Input Offset Current		50	nA
Input Bias Current		200	nA
Input Resistance		400	kΩ
Output Resistance		150	Ω
Power Consumption	$V_S = \pm 15$ V	80	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ		
Rise Time	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ,	0.3	μs
	$C_2 = 200$ pF, $R_2 = 50$ Ω		
Overshoot	$C_L \leqslant 100$ pF	10	%
Average Temperature Coefficient			
of Input Offset Voltage	$R_S = 50$ Ω	3.0	μV/°
	$R_S \leqslant 10$ kΩ	6.0	μV/°
Large-Signal Voltage Gain	$V_S = \pm 15$ V, $R_L \geqslant 2$ kΩ, $V_{out} = \pm 10$ V	45,000	
Output Voltage Swing	$V_S = \pm 15$ V, $R_L \geqslant 10$ kΩ	± 14	V
	$V_S = \pm 15$ V, $R_L \geqslant 2$ kΩ	± 13	V
Input Voltage Range	$V_S = \pm 15$ V	± 10	V
Common Mode Rejection Ratio	$R_S \leqslant 10$ kΩ	90	dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10$ kΩ	25	μV/

Fig. 7 Output Voltage Swing as a Function of Supply Voltage.

Fig. 9 Voltage Gain as a Function of Supply Voltages.

Fig. 8 Output Voltage Swing as a Function of Load Resistance.

Fig. 10 Voltage Gain as a Function of Ambient Temperature.
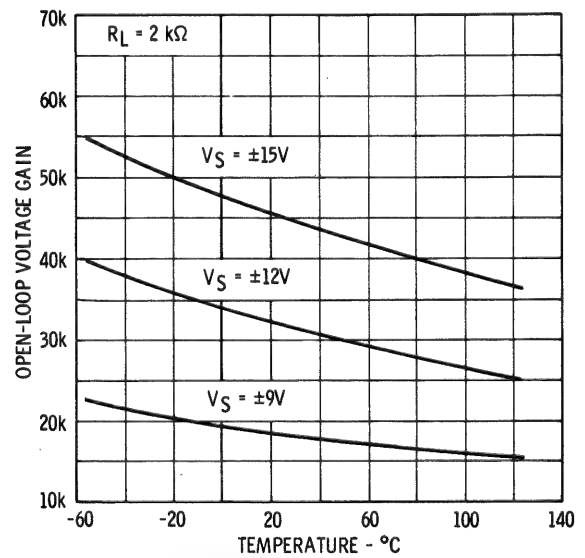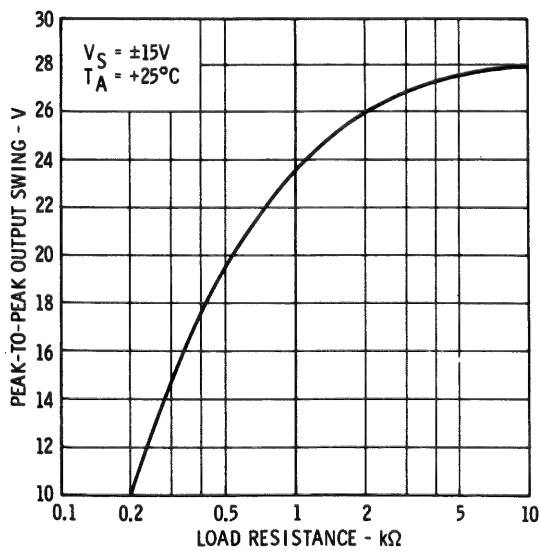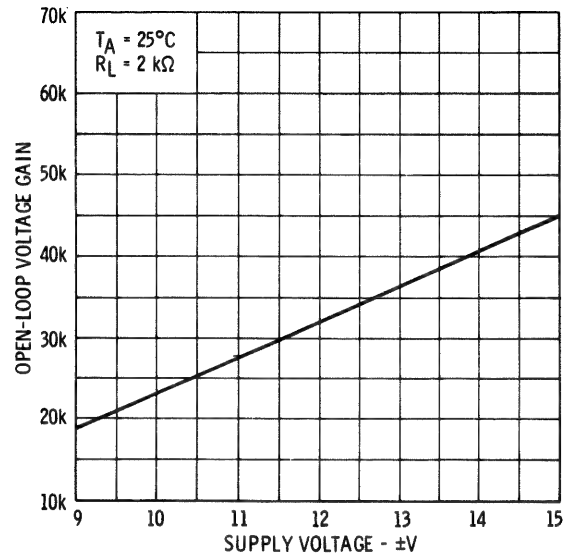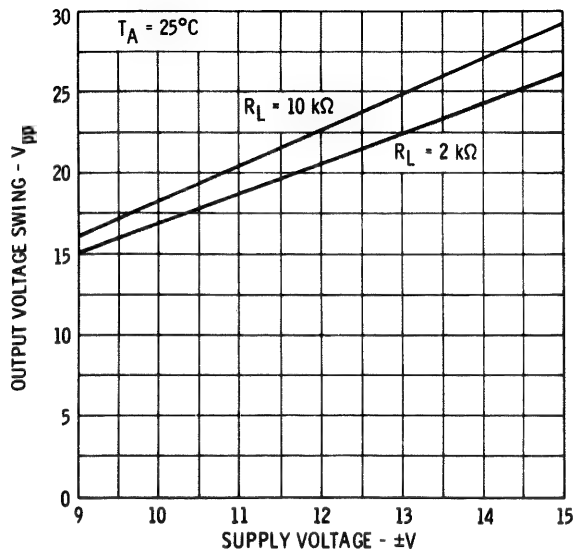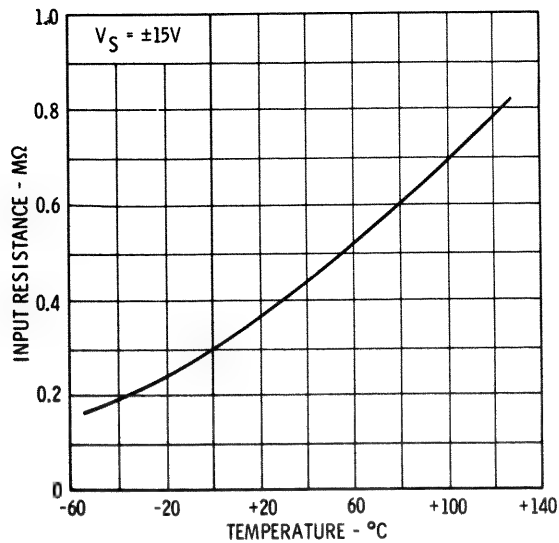
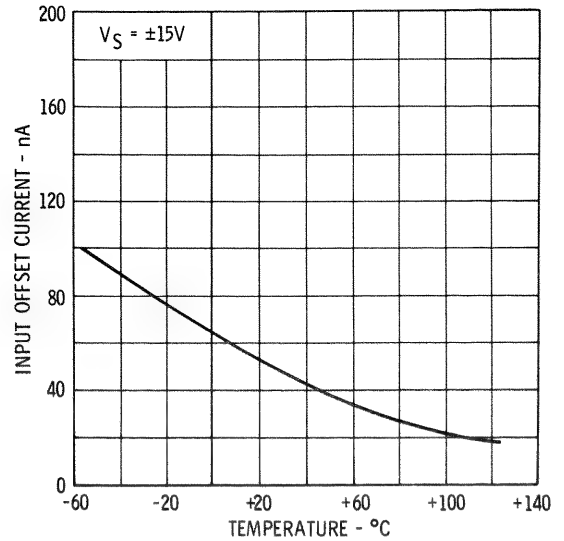Fig. 11 Input Resistance as a Function of Ambient Temperature.

Fig. 13 Input Offset Current as a Function of Ambient Temperature.

to the change in transconductance of the second stage, since the gains of the input and output stages are essentially independent of temperature.

Since the transistor current gain decreases at low temperatures, the input resistance, input bias current, and input offset current have the temperature dependence shown in Figures 11 through 13. Owing to the logarithmic relationship between supply voltage and the operating currents of the input stage, the bias current changes very little with supply voltage (Figure 14).
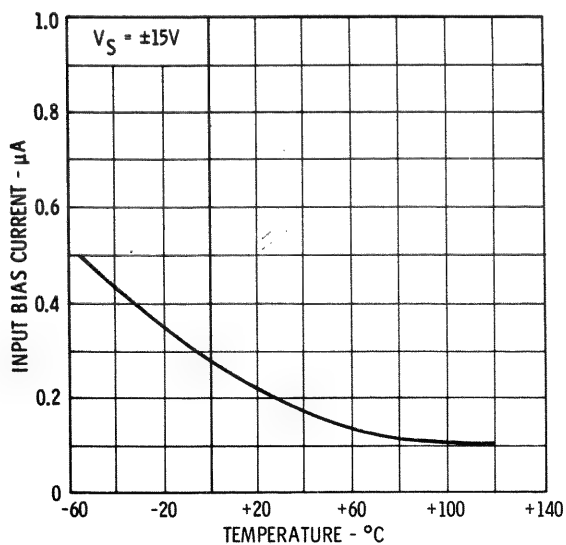
Fig. 12 Input Bias Current as a Function of Ambient Temperature.
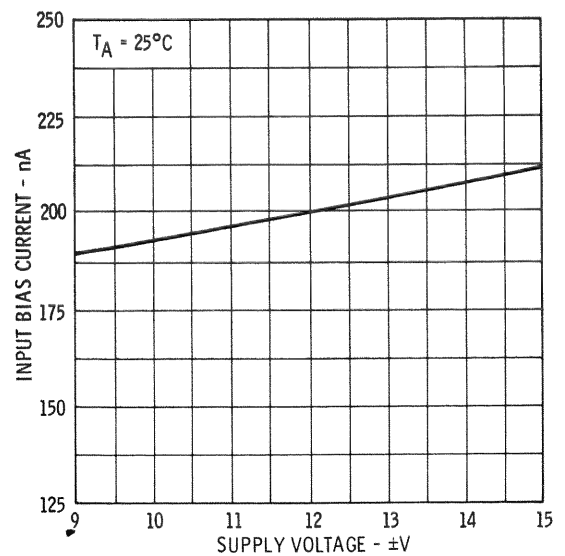
Fig. 14 Input Bias Current as a Function of Supply Voltage.

The common mode voltage limits are determined by saturation of the input transistors in the positive direction, and by saturation of the current source transistor in the negative direction. Because of the unique biasing method used for the current source (Q_{11}), the negative common mode limit is about $2V$ above the negative supply for all supply voltages. The positive common mode limit, however, is a function of supply voltage, as shown in Figure 15. The common mode rejection ratio is measured with a symmetrical input signal with a peak-to-peak value equal to twice the positive common mode range. Typical common mode input impedance is about 300 $M\Omega$.

Fig. 16 Power Supply Current as a Function of Supply Voltage.

Fig. 15 Input Common Mode Voltage Range.
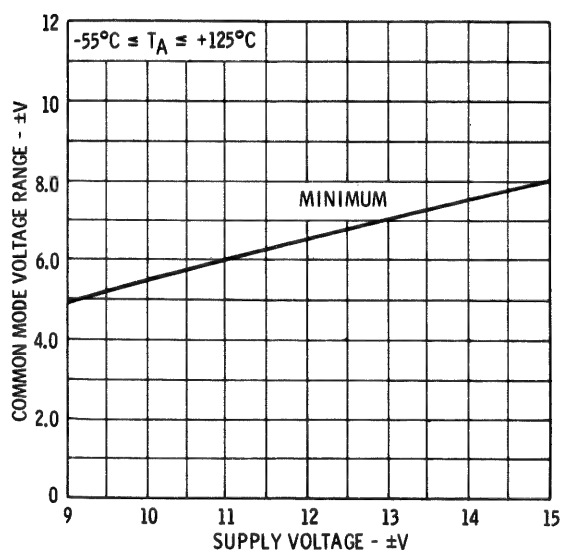
Fig. 17 Power Supply Current as a Function of Ambient Temperature.

The effects of supply voltage and temperature upon the power supply current are shown in Figures 16 and 17. The curves apply for both positive and negative supply currents since they are equal under quiescent conditions (no load). This current will vary approximately ± 0.75 mA as the output swings over its full dynamic range.

The excellent matching of components and the balanced design contribute to very low offset voltages and small changes of offset with supply voltage, as can be seen from the figures in Table I. The change of offset voltage for supply voltage variations (supply voltage rejection ratio) is specified

for the worst-case condition of both supplies increasing or decreasing simultaneously. Figure 18 shows the change of offset produced when one supply is varied while the other is held constant.

A convenient method of nulling the offset voltage of the $\mu A709$ is shown in Figure 19. Resistor R_1 simulates a current source at the collector of input transistor Q_2; adjustment of R_2 unbalances the collector currents in Q_1 and Q_2 such that zero

differential voltage is produced between the bases of Q_3 and Q_4. This nulls the input offset voltage and, at the same time, approximates the condition for minimum drift. It should be noted that stability of the adjustment depends upon the stability of the power supply.

The input-referred noise voltage and noise current produced by the amplifier are given in Figures 20 and 21 for a frequency range of $10\,Hz$ to $100\,kHz$.

Fig. 18 Offset Voltage Change as a Function of Supply Voltage.

Fig. 20 Input Noise Voltage as a Function of Frequency.
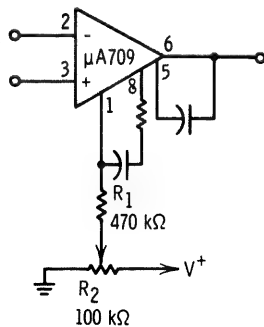
Fig. 19 Method for Offset Nulling.
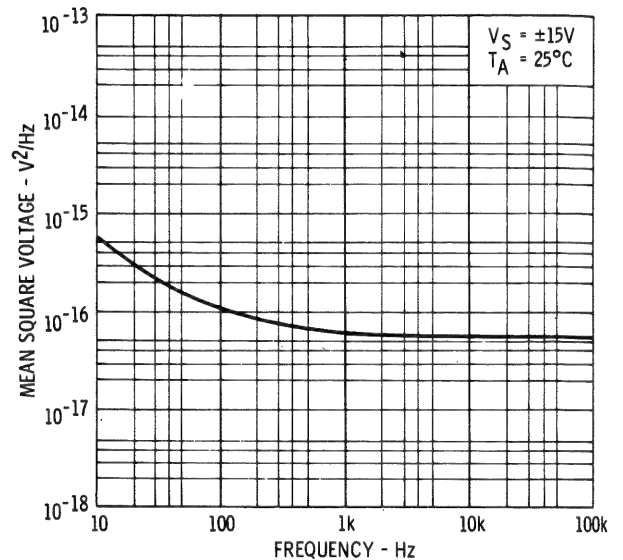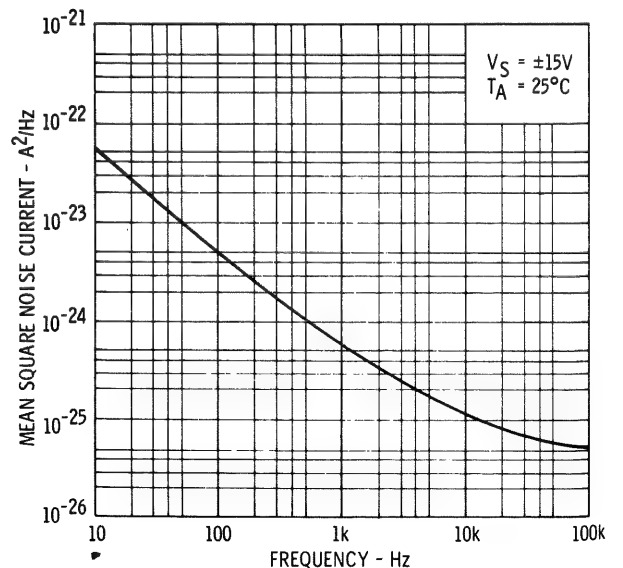
Fig. 21 Input Noise Current as a Function of Frequency.

The break point for 1/f noise is about 100Hz for the noise voltage and 10kHz for the noise current. Figure 22 illustrates the spot noise figure contours as a function of frequency and source impedance.

Figure 23 is included to aid the designer in estimating the noise performance to be expected as a function of source resistance and pass band. It shows the total broadband input-referred noise as a function of source resistance for various bandwidths; Figure 24 is the same data plotted in terms of noise figure.
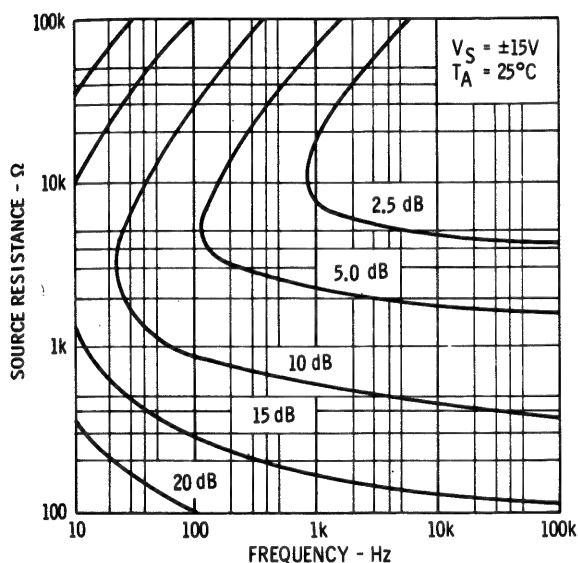
Fig. 22 Spot Noise Figure Contours.
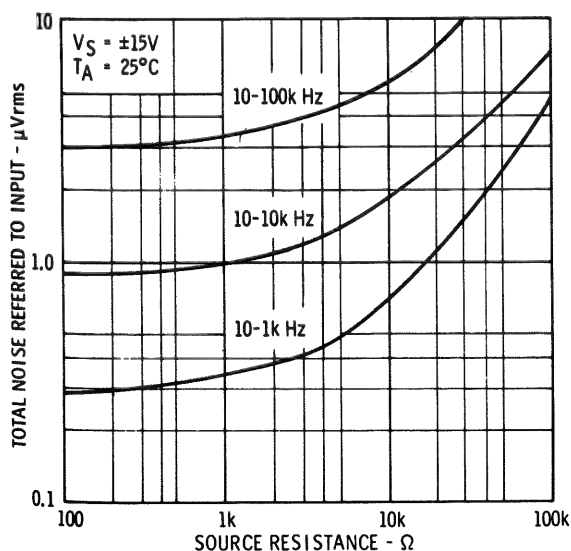
Fig. 23 Broadband Noise for Various Bandwidths.
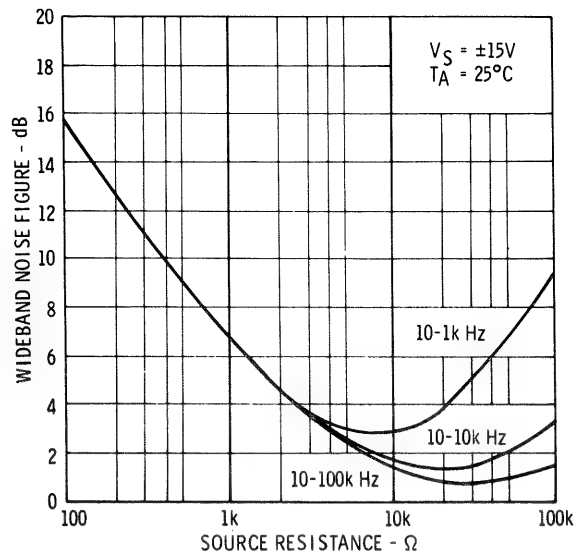
Fig. 24 Wideband Noise Figure for Various Bandwidths.

FREQUENCY COMPENSATION

According to feedback theory, an amplifier will be unstable if the high-frequency loop gain is greater than or equal to unity when the phase shift reaches 180 degrees. Since the natural response of the amplifier is limited by internal capacitances, it is usually necessary to shape the gain-phase characteristics with external compensation networks to achieve stability for any amount of feedback. The most common procedure is to synthesize a roll-off characteristic approximating that of a single R-C network; since the maximum roll-off associated with such a network (6 dB/octave) is 90 degrees, the circuit cannot become unstable.

With some amplifiers (such as the μA702A), large bandwidths can be obtained by using the natural roll-off of the amplifier to provide part of the compensation. This cannot be done with the μA709, however, because its gain falls off above 2 MHz at a rate approaching 18dB/octave. Without compensation, the amplifier may even oscillate open-loop due to stray capacitance and high gain. Figures 25 and 26 show the gain and phase characteristics obtained with minimum frequency conpensation. As can be seen, the amplifier can only be closed down to a gain of 50 dB for a 30-degree phase margin. Lower closed-loop gains require that the roll-off from the compensation networks begin at a low enough frequency to ensure that the loop gain will be less than unity before the amplifier introduces additional phase shift.
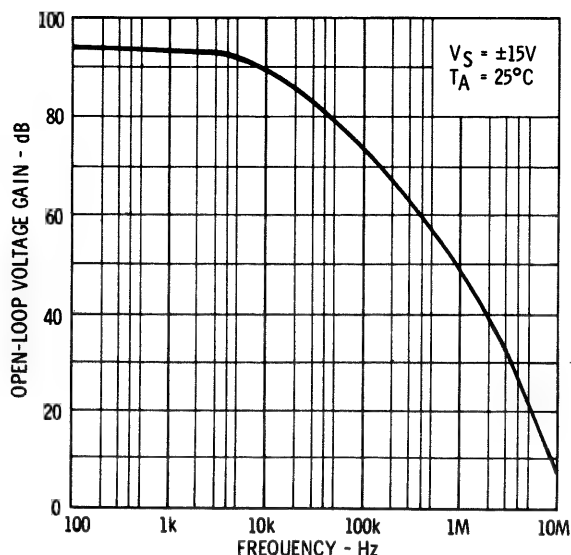
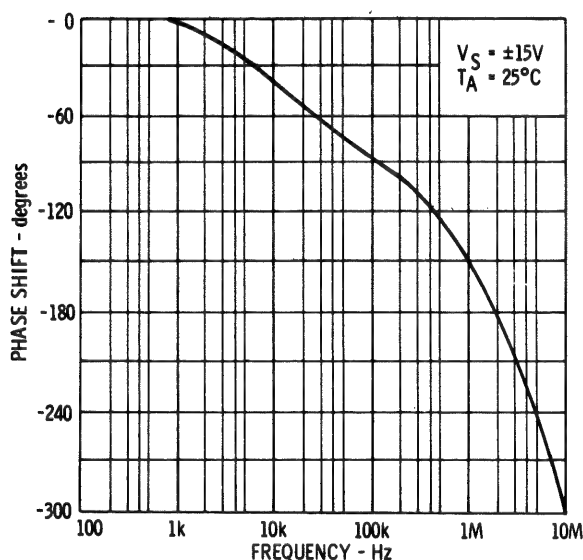Fig. 25 Open-Loop Frequency Response with Minimum Compensation ($C_1 = 10pF$, $C_2 = 3pF$).

Fig. 26 Open-Loop Phase Shift with Minimum Compensation ($C_1 = 10pF$, $C_2 = 3pF$).

COMPENSATION POINTS

Two sets of frequency compensation points have been provided for the μA709 since it is usually difficult to obtain compensation of more than 60 dB at one point. The points chosen (see circuit diagram of Figure 5) have quite high transfer resistances so that the amplifier can be fully compensated with small external capacitors. Figure 27 shows the general compensation networks required to stabilize the amplifier. Collector-to-base feedback around
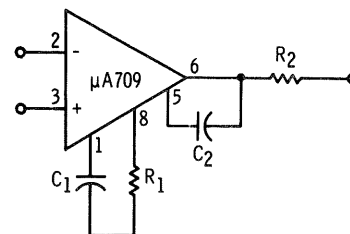
Fig. 27 Frequency Compensation Networks.

the second stage via $R_1 - C_1$ provides the first 60 dB of roll-off, and another feedback loop around the output stage gives the remaining compensation. The transfer resistance of the input compensation terminals varies from 1 to 2 $M\Omega$ and is typically 1.4 $M\Omega$; that of the output compensation varies from 10 to 80 $k\Omega$ and typically is 36 $k\Omega$. Relative change with temperature and supply voltage is given in Figures 28 and 29.

The output compensation feedback loop (emitter of Q_{14} to base of Q_{12} through C_2) has a dominant pole due to parasitic capacitance at the base of Q_{14}. When the amplifier is operated with capacitive loading, the second pole introduced at the emitter of Q_{14} may cause instability. Resistor R_{13} was included in the μA709 to make the circuit less sensitive to this, but it does not cure the oscillation for all combinations of resistive and capacitive loading. For capacitive loading, therefore, series compensation resistor R_{13} should be used to isolate the output compensation from the load; the output voltage swing is not significantly affected by this resistor since its value is only 50Ω.
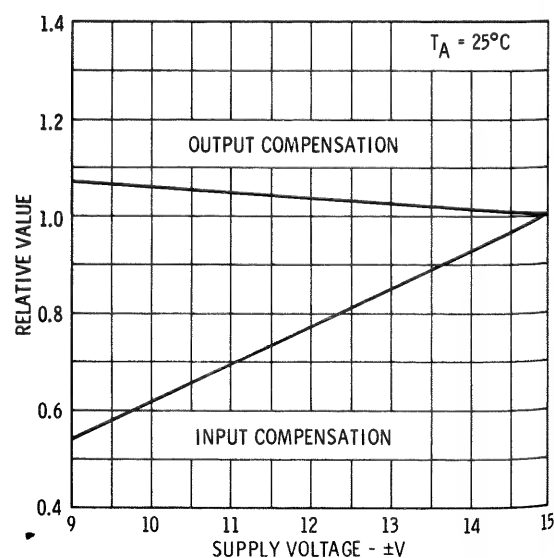
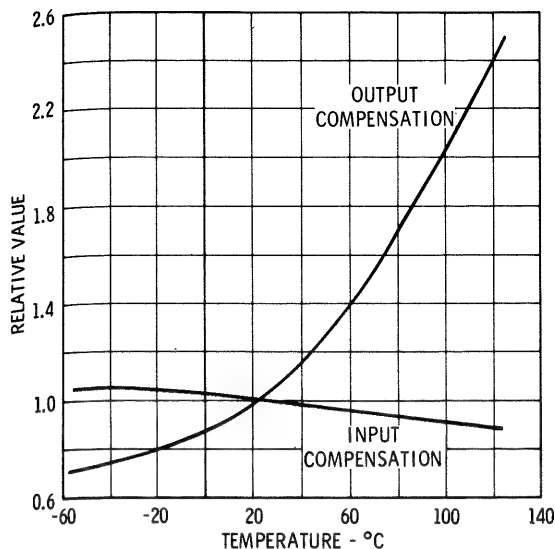Fig. 28 Compensation Terminal Impedance as a Function of Supply Voltage.

Fig. 29 Compensation Terminal Impedance as a Function of Ambient Temperature.

Fig. 30 Closed-Loop Response Using Recommended Compensation Networks.

RECOMMENDED NETWORKS

The frequency compensation networks used in a given application must provide stability for any $\mu A709$ selected from the full production distribution. The unit-to-unit variation of transfer resistance, open-loop voltage gain, and high-frequency phase shift must be taken into account, as well as the effects of temperature and power supply voltage. A design based on worst-case limits for each of these parameters, however, would be unnecessarily conservative since they are correlated to some degree in an integrated circuit. The change of gain with supply voltage, for example, is partially compensated for by a change in transfer resistance, and thus the closed-loop bandwidth is only slightly affected. Therefore, rather than having separate limits for each of these factors, it is better to consider the amplifier as a whole and specify the complete networks to be used to guarantee stability for the full distribution of units.

Figure 30 gives the networks recommended for frequency compensation of non-inverting amplifiers having closed-loop gains of 0, 20, 40, and 60 dB, along with the frequency responses obtained using these networks; values for intermediate gains can be found by interpolation. For inverting amplifiers, the capacitor values should be divided by the factor $(1 + R_s/R_f)$ to obtain the same bandwidths. The bandwidth can be expected to vary from 0.4 to 1.8 MHz with less than 1 dB of peaking, depending upon the particular unit. Figure 31 shows the corresponding open-loop frequency responses.

Fig. 31 Open-Loop Response Using Recommended Compensation Networks.

A simple test that indicates both closed-loop bandwidth and stability of a circuit using the recommended compensation networks is the small-signal step-function response. The rise-time of the output step (Figure 32) is related to the bandwidth by the approximate formula

$$\tau_r = \frac{0.35}{BW}, \tag{1}$$

and the overshoot is a measure of the stability. The effect of capacitive loading can also be included in the measurement. The significant advantage of transient response testing is that the combined effect of all factors upon stability is indicated by
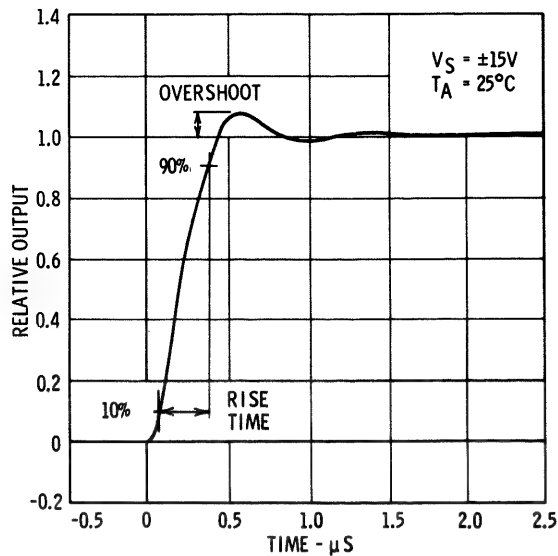
Fig. 32 Transient Response.

Fig. 33 Slew Rate as a Function of Closed-Loop Gain Using Recommended Compensation Networks.

one, easily-made test, including any correlation between the parameters. Rise times for production units can range from 0.2 to 1.0 μs for closed-loop gains of 60 dB or less, and the overshoot will be less than 30% with 100 pF capacitive loading.

RATE LIMITING

The response of an operational amplifier to large changes in input signal is not as fast as might be expected from the small-signal bandwidth. This is due to the early roll-off in open-loop gain caused by the compensation networks. A large step change in signal forces the feedback to overdrive the input stage as it attempts to correct for the slow rise time of the frequency-compensated stages. The clipped signal is integrated by the compensation capacitors, resulting in an output voltage that rises at a fixed rate. This rate limit, or slew rate, determines the speed with which the amplifier can respond to large signals. Figure 33 gives the slew rate of the $\mu A709$ as a function of closed-loop gain using the recommended compensation networks.

The maximum sine wave output that can be handled at high frequencies is also limited by slewing. When the rate of change of voltage required from the amplifier exceeds the slew rate, the output amplitude begins to fall off and the waveform becomes triangular. The peak undistorted sine wave output that can be obtained at a given frequency is given by

$$V_p = \frac{p}{2\pi f} \tag{2}$$

where p is the slew rate in $V/\mu s$, and
f is the frequency in MHz.
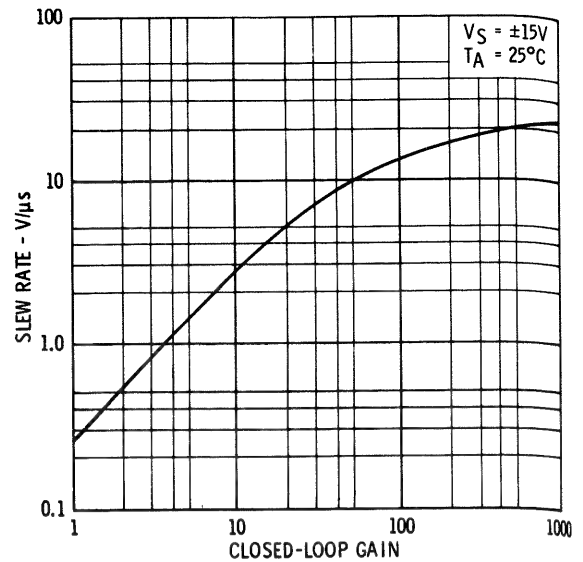
Curves of output voltage swing as a function of frequency are shown in Figure 34 for various compensation networks.
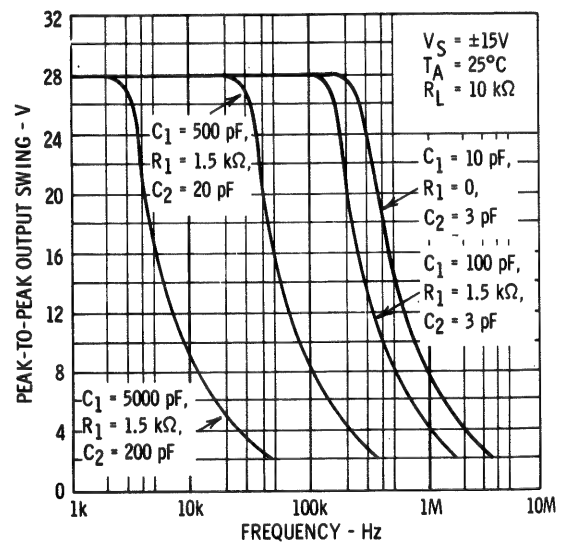
Fig. 34 Output Voltage Swing as a Function of Frequency for Various Compensation Networks.

SUPPLY VOLTAGE AND TEMPERATURE EFFECTS

All of the open-loop characteristics are functions of power supply voltage and temperature. The correlation between the various parameters, however, is such that the closed-loop performance is not affected as much as might be expected from the worst-case changes in individual open-loop parameters.

The relative change in closed-loop characteristics with supply voltage is shown in Figure 35. The decrease in open-loop voltage gain as the voltage goes from ±15V to ±9V is partially compensated by a corresponding decrease in input compensation transfer resistance; as a result, the closed-loop bandwidth changes less than 25%. The output compensation transfer resistance is not appreciably affected by supply voltage.
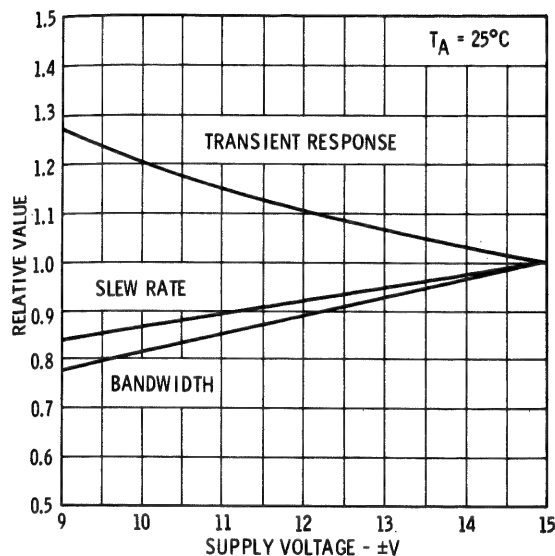

Fig. 35 Change of Characteristics with Supply Voltage.

The change in gain with temperature is also compensated for by the input transfer resistance, and so the closed-loop bandwidth varies only as the output transfer resistance. At −55°C, the bandwidth is about 37% higher than its room temperature value, and decreases to 55% at +125°C, as shown in Figure 36 (both Figures 35 and 36 apply for closed-loop gains of 60 dB or less).

GENERAL PRECAUTIONS

Use of the $\mu A709$ under certain operating conditions can result in abnormal performance or catastrophic failure of the device. Since the source of the problem is not always immediately evident, the most common difficulties will be pointed out below. The protection schemes described may not be necessary in a well-designed system using the $\mu A709$, but can be used to good advantage in breadboard and bench work, where accidents are more likely to happen.
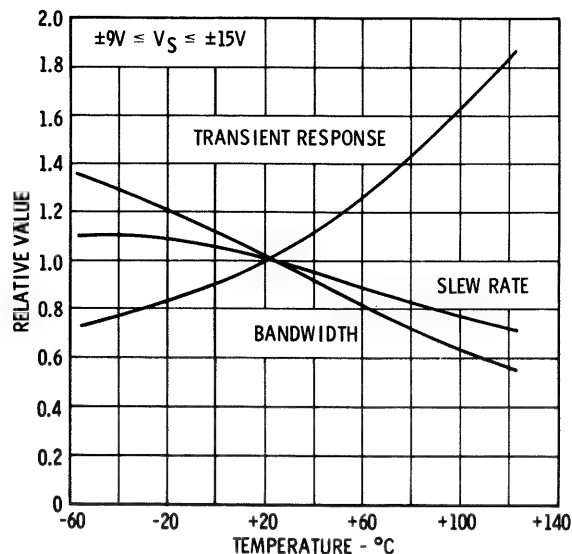
Fig. 36 Change of Characteristics with Ambient Temperature.

LATCH-UP

As mentioned previously, the common mode voltage limits of the $\mu A709$ are determined for negative inputs by saturation of the current source transistor, and for positive inputs by saturation of the input transistors. Exceeding the positive common mode limit of the device may cause damage to the inputs through excessive current. Even if the current is limited to a safe value, however, erratic operation can still result. If the transistor on the inverting input saturates, for example, it no longer acts as an inverting amplifier but makes a direct connection between the input and the base of the second stage transistor—thus becoming a non-inverting input. This results in positive feedback, and latch-up will occur if it is possible for the output voltage to hold the input stage in saturation through the feedback network.

With the voltage follower circuit of Figure 37, this tends to be a particular problem. It is easy for a transient to trigger latch-up, since the output is connected directly to the inverting input. One possible solution is to put a 33 $k\Omega$ resistor between the
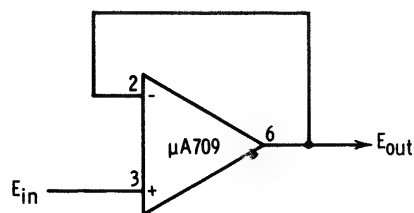

Fig. 37 Voltage Follower.

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output and input to limit the feedback current, but this increases the offset voltage. Another method that works in most situations is shown in Figure 38 (a). The output voltage is prevented from rising higher than the common mode limit (voltage at base of Q_4) by the diode clamp, D_1. This keeps the input transistor from going into saturation, and thus latch-up cannot occur. Even though external resistors are not required to prevent latch-up with this circuit, it is wise to include some resistance at each input for protection against differential transients, as discussed below. Up to 10 $k\Omega$ can be used without increasing the offset voltage above the guaranteed maximum.

A third method, Figure 38(b), uses a PNP transistor connected across the input terminals. In normal operation, the transistor is turned off because the voltage between inputs is only a few mV. When a transient or input signal exceeds the common mode range, the output of the amplifier goes into positive saturation. But the amplifier does not remain latched-up after the transient disappears; instead, Q_1 turns on and pulls the inverting input back into the common mode range.

DIFFERENTIAL INPUT VOLTAGE

Although the input common mode voltage range of the μA709 is $\pm8V$, the maximum voltage permitted between the inputs is limited to $\pm5V$. If one of the inputs is grounded, for example, the other can only be driven as high as $+5V$ or as low as $-5V$ without exceeding the limit. It is important to observe this maximum rating, since exceeding it could cause permanent degradation in the input offset current and input bias current by drawing excessive current in breaking down the emitter-base junctions of the input transistors. If the current becomes greater than about 50 mA, the junctions will short. The circuit can be protected by placing a pair of zener diodes (Figure 39(a)), or a pair of fast silicon diodes (Figure 39(b)), across the inputs—if the application does not require the $\pm5V$ differential input voltage range.

Some failures have been traced to the use of ungrounded soldering irons to install the amplifier. Line transients can feed through the insulation of the iron and destroy the unit by arcing over the emitter-base junctions. If the iron is grounded, the
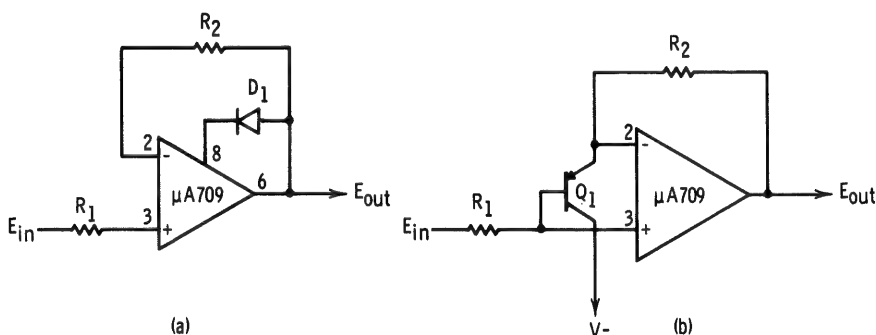

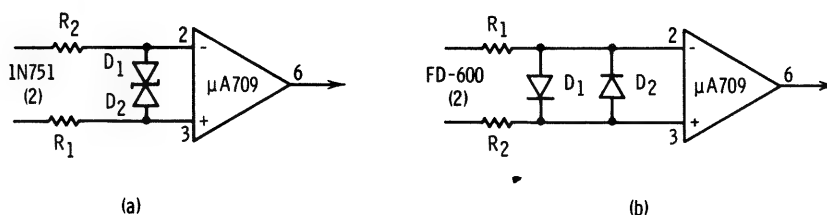Fig. 38 Protection Against Latch-Up.

Fig. 39 Protection Against Input Breakdown.

circuit grounded or disconnected from any line-operated equipment, and the supply voltages removed, there should be no problem. This type of damage can also be caused by ungrounded test equipment and temperature-chamber transients.

Some common situations where input break-down may occur but not be immediately evident are shown in Figure 40. In (a), if a large voltage step is applied to the input, the output will try to follow, but can only change as fast as the slewing rate. During the time that the output is changing, the summing point will not be held at ground, and a voltage spike will develop. If this spike exceeds the 5V differential input limit, one of the emitter-base junctions of the input pair will break down and may be damaged, depending upon the current that flows.

In (b), if only the positive supply voltage is connected, the output will be high and the voltage developed at the summing point may exceed the breakdown voltage, depending upon the resistor ratios. The cases described in Figures 40(a) and (b) are particularly severe in the voltage-follower configuration.

The integrator connection of Figure 40(c) can cause trouble under certain conditions of capacitor charge and supply connection. If the integrating capacitor is charged to a high voltage and both supplies are suddenly disconnected or turned off, the voltage spike developed at the summing junction may break down the inputs. Another possibility arises if the capacitor is charged to the positive supply voltage and only the positive supply is disconnected. This produces a large spike at the summing point that may be more negative than the negative supply voltage. If this is the case, the emitter-base of the inverting input transistor may break down with current flow through the collector isolation diode of the current source transistor.

SUPPLY VOLTAGE POLARITY

Another point that is sometimes overlooked is the polarity of the power supply voltages. It is quite important that the negative supply terminal always be the most negative point in a monolithic integrated circuit. If the supply voltages are reversed, the isolation diode that normally separates the different elements in the circuit becomes forward-biased. This effectively puts a short between the power supplies, resulting in a large current (greater than 750 mA) that melts the aluminum metallized interconnections. If the possibility exists that the supplies could be reversed, either by accident or by a turn-on transient in the power supply set-up, the amplifier can be protected with a diode as shown in Figure 41. The negative supply voltage can be increased about 0.7V to compensate for the voltage drop in the diode, if desired.
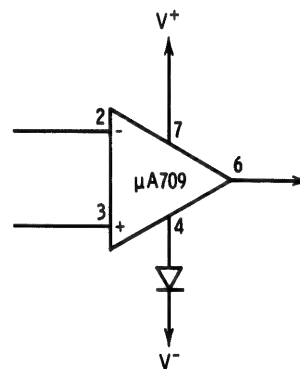

Fig. 41 Protection Against Power Supply Reversal.

MAXIMUM SUPPLY VOLTAGE

The maximum steady-state voltage that can be placed across the amplifier is 36V. Most devices from the production distribution can withstand surges up to 50V, but operation at such voltage

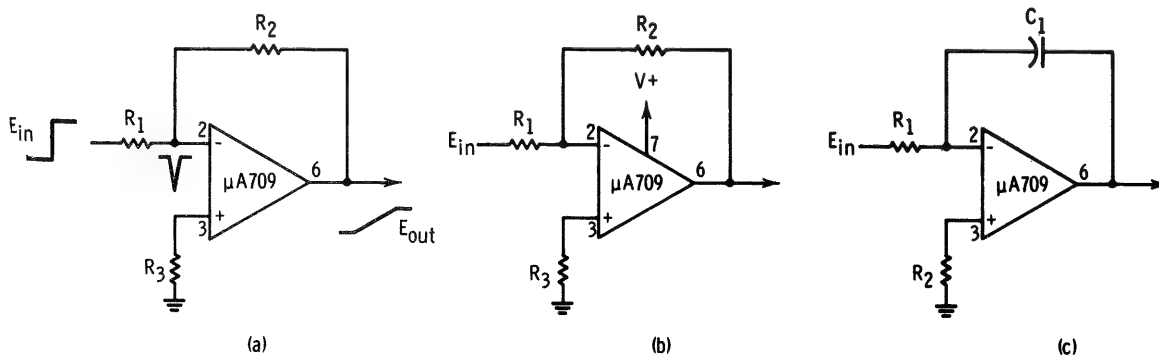(a)   (b)   (c)

Fig. 40 Circuits Where the Differential Input Voltage Range May Be Exceeded.

levels is neither recommended nor guaranteed. Protection against supply over-voltage can be accomplished with a 36V zener diode connected across the supplies (Figure 42).

OUTPUT SHORT-CIRCUIT

As mentioned previously, the output stage of the μA709 can withstand a short-circuit for a short period of time. The current gain of the output transistors is injection-efficiency limited at high current levels and falls off at high temperatures. This limits the short-circuit output current to about 75 mA for any condition of input drive. The length of time that the device can survive a direct short is a func-

tion of the internal power dissipation and tempera ture, and is at least 5 seconds at 25°C.

Protection against short-circuits to ground of any duration can be had by inserting a small resis tor in series with the output to limit the maximum power dissipation. At the expense of a 10% reduc tion in maximum output voltage swing (into a 2kΩ load), the 200Ω resistor shown in Figure 43 will completely short-circuit protect the amplifier for ambient temperatures to 75°C or case temperatures to 125°C. The resistor does not affect the normal operation of the circuit, since it is inside the feed back loop.
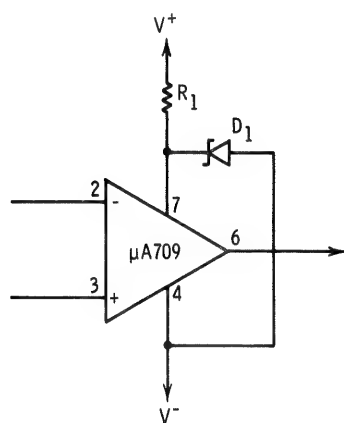
Fig. 42 Protection Against Power Supply Over-voltage.
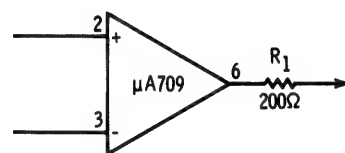
Fig. 43 Protection Against Output Short-Circuit.

THE μA710 & uA711 HIGH-SPEED COMPARATORS

CHAPTER 7

A differential voltage comparator is a high-gain, differential input, single-ended output amplifier. The function of the device is to compare a signal voltage on one input with a reference voltage on the other and produce a digital one or zero at the output when one input is higher than the other. A comparator is useful as a low-hysteresis, variable-threshold Schmitt trigger, a pulse-height discriminator, a voltage comparator in A/D converters, a zero-crossing detector, a threshold detector, an oscillator, a high noise-immunity digital line receiver, or in pulse-width modulator applications. A dual comparator, which will also be discussed, can be used as a core memory sense amplifier, a window discriminator in pulse-height analyzers, or a double-ended limit detector for automatic go/no-go test equipment.
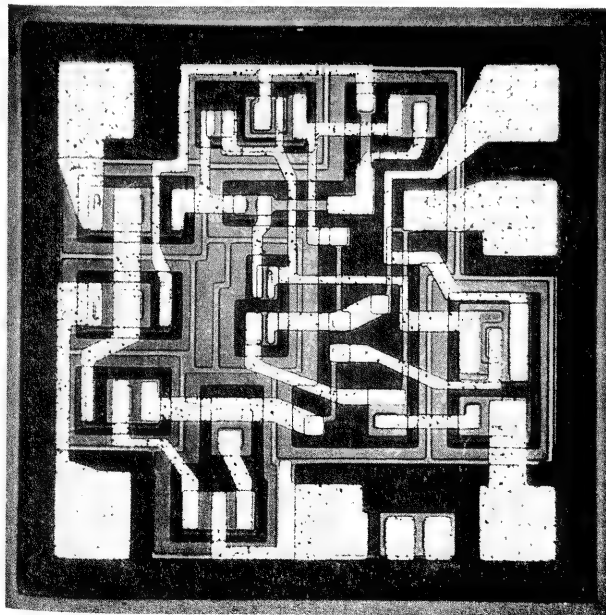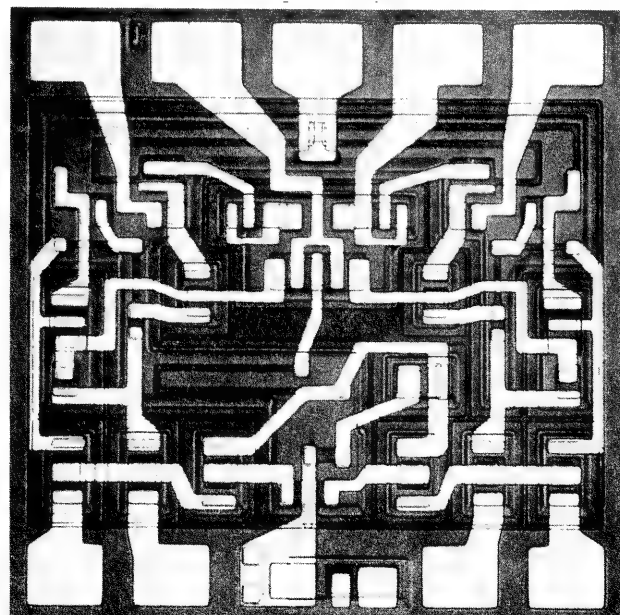
This chapter describes the design and performance of the μA710 high-speed differential comparator and the μA711 dual comparator. These comparators make use of the excellent component matching and low wiring capacitances available with monolithic construction. The devices have very stable DC characteristics over a wide temperature range, and response times superior to discrete-component circuits of comparable performance and power dissipation. Their simplicity and suitability for integration are demonstrated by the design analysis that follows, and by the fact that the μA710 is constructed on a 35-mil square silicon die while the μA711 dual comparator is constructed on a 40-mil square die — both using the standard Planar*-epitaxial process. Photomicrographs of the μA710 and μA711 are shown in Figures 1 and 2, respectively.

Fig. 1 Photomicrograph of the μA 710.

Fig. 2 Photomicrograph of the μA 711.

* Planar is a patented Fairchild process.

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CIRCUIT DESCRIPTION

A comparator is similar to a differential input operational amplifier, and, in fact, operational amplifiers are frequently used as comparators. In many applications, however, the comparator is expected to recover rapidly from saturation, which is its normal operating state. Additionally, the large output voltage swing desired for operational amplifiers is often a disadvantage when the comparator is used to drive low-level logic circuits.

The comparator described herein is designed to overcome the limitations of operational amplifiers used as comparators. It features extremely fast recovery from saturation and an output that is compatible with practically all integrated logic forms.

The operation of the comparator can be explained using the simplified schematic of Figure 3. A differential input stage (Q_1 and Q_2) is used for low offset. The emitters of the input stage are supplied from a current source (Q_9) to make their collector currents insensitive to the common mode input voltage. The second stage (Q_3 and Q_4) is basically the balanced biasing scheme described in Chapter 2. Variations of this useful circuit have

also been used in the μA702A and μA709 One feature of the second stage is that, under balanced conditions, the single-ended output is insensitive to changes in positive supply voltage. If the positive supply voltage is increased, the collector currents of both Q_3 and Q_4 will increase such that the voltage on the collector of Q_4 remains constant.

An emitter-follower is used at the output of Q_4 to give a high output-current capability. A zener diode (D_1) in the emitters of the second-stage transistors provides a large input-voltage range (the positive input-voltage limit is essentially equal to the voltage on the base of the second-stage transistors). An identical zener diode in the output emitter-follower (D_2) level-shifts the output back to a level compatible with logic circuits. Q_8 isolates the output from the diode-compensated bias divider for the input-stage current source. With the diode-connected transistor, Q_{10}, used to compensate for the emitter-base voltage of Q_9, the current source can operate with a small voltage drop across its emitter resistor, R_8. This gives a large negative input-voltage limit.

The complete schematic of the μA710 in Figure 4 shows the addition of Q_6 connected as a diode.
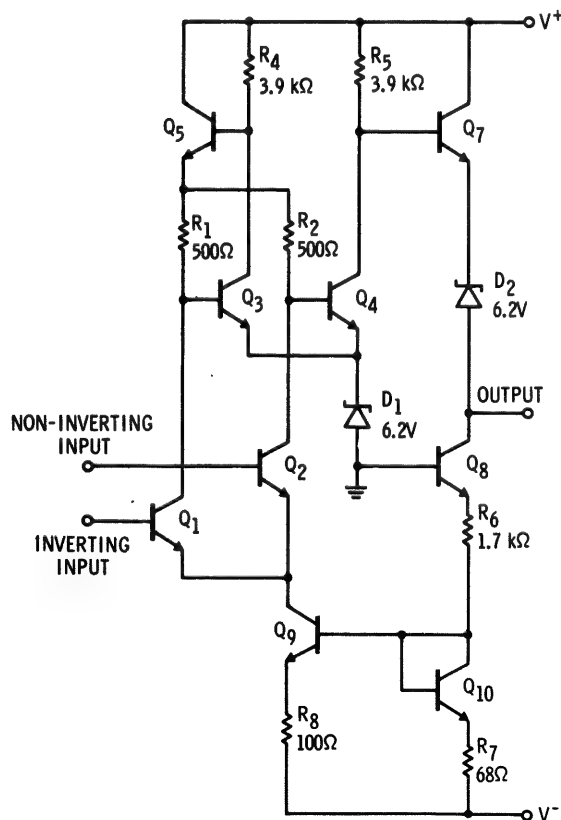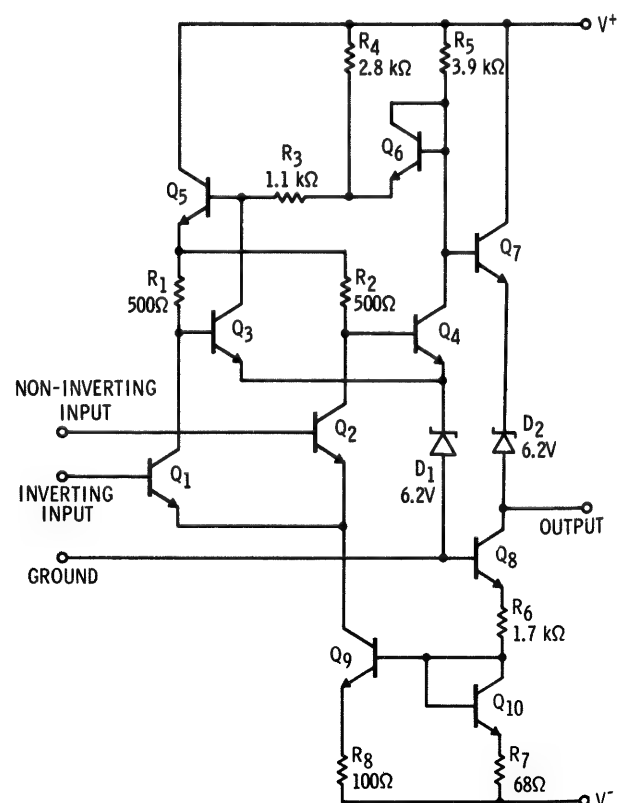

Fig. 3 Simplified Schematic.

Fig. 4 Complete Schematic of the μA 710.

This limits the positive output swing, both to increase speed and to provide compatibility with certain integrated logic families.

A schematic diagram of the μA711 dual comparator is shown in Figure 5. The outputs of two individual comparators are OR'ed at the emitter-followers. Only a single level-shifting zener diode and bias divider are used. Zener diodes on the bases of the output emitter-followers provide a method of disabling the individual channels: when the strobe terminal on one side is held down to ground level, the output of that side cannot rise. The strobe terminal can also be used to clamp the positive output swing, since the output voltage will always be at least one diode drop less than the voltage on the strobe terminal; hence, no clamping diode is used. The output sink-current capability of the μA711 is less than that of the μA710, both to reduce power dissipation and to allow a large number of μA711's to be wire OR'ed at the output.

Another difference between the μA710 and μA711 is that a transistor has been added in the second stage to reduce the base drive on Q_4 when it saturates. This action not only gives a lower power dissipation, but also reduces the storage time of Q_4. When the comparator is operating in the active region, the collector current of Q_2 produces a

voltage drop across R_6 that keeps Q_5 in a nonconducting state. Hence, Q_5 does not influence operation in the active region. With a large negative input, however, Q_2 is turned off and no longer produces this hold-off voltage across R_6, and Q_5 conducts. Q_5 can then conduct the entire current through R_4 with only a small voltage drop across R_2 and R_6. R_1 has a large voltage drop across it since the collector current of Q_1, which is nearly the entire collector current of Q_{11}, is flowing through it. This voltage drop across R_1 cuts off Q_3. Such a state of operation, with Q_5 conducting and Q_3 cut off, is illustrated in the simplified schematic of Figure 6. R_6 is eliminated, as the voltage drop across it is small enough to be neglected.
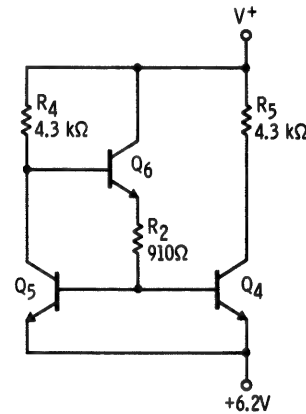
Fig. 6 Simplified Schematic Showing Operation of the Saturation Limiter Circuitry.
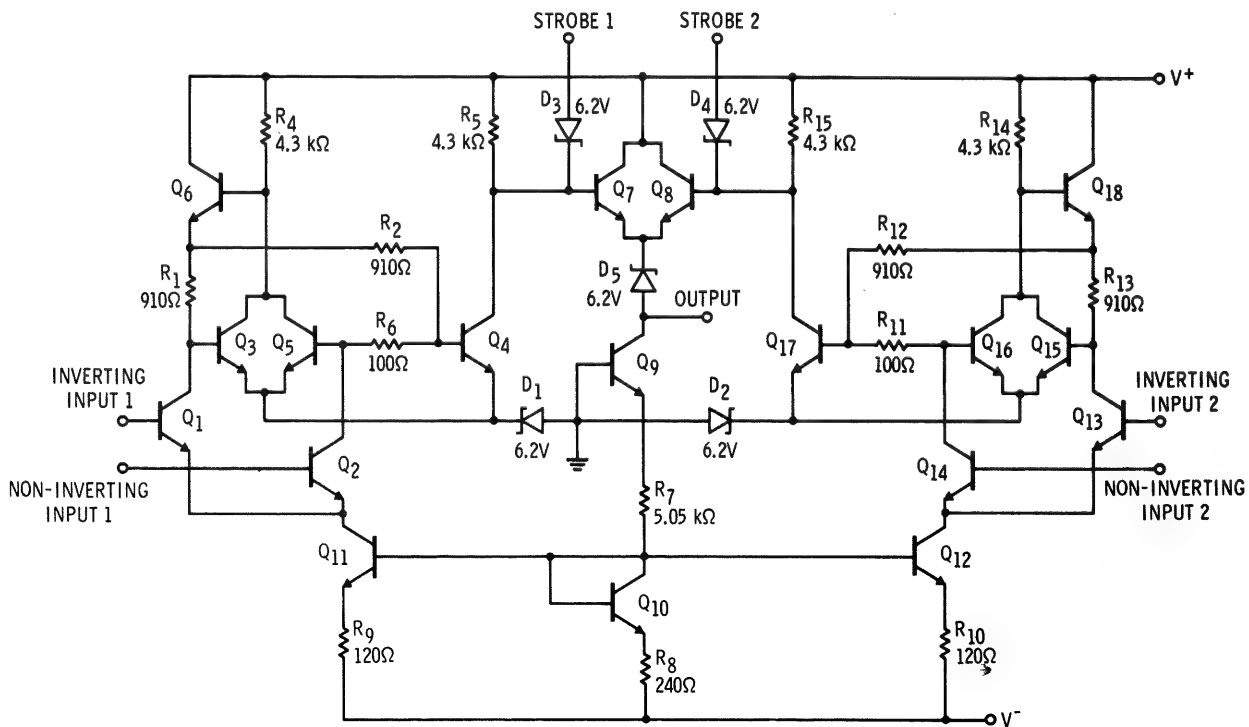
Fig. 5 Complete Schematic of the μA 711.

If it is assumed that Q_4 and Q_5 of Figure 6 are identical transistors, their collector currents will be equal since they are operating with the same emitter-base voltage. The collector current of Q_5 is determined by R_4 and the voltage drop across it. The collector-to-emitter voltage of Q_5 will be two emitter-base voltage drops (Q_5 and Q_6) plus the small voltage drop across R_2. The collector-to-emitter voltage of Q_4 will be equal to that of Q_5 since their collector currents are equal and R_5 is equal to R_4. To attain the proper negative output level, however, Q_4 should be made to saturate. This can be accomplished by making the emitter junction of Q_5 smaller than that of Q_4, so that Q_4 will conduct more current than Q_5 with the same emitter-base voltage (this is easily accomplished in a monolithic integrated circuit). With the proper ratio of device geometries, Q_4 can be made to go just barely into saturation, giving minimum storage time.

DESIGN ANALYSIS

The accuracy of a comparator is primarily dependent on component matching. Resistor values, the transistor current gains, emitter-base voltages, zener voltages, and even power-supply voltages may vary over an unusually wide range as long as certain parts are well matched. In the analysis, the simplified schematic in Figure 3 will be used, since the active region of the comparator, where the refinements of the μA710 and μA711 are inoperative, is under consideration here.

First, an expression will be obtained for the output voltage corresponding to zero input voltage. It is desired that this be equal to the threshold voltage of the logic circuit that the comparator drives so that the logic state changes as the differential input of the comparator goes through zero. It will be assumed that all the resistors are perfectly matched in ratio, that transistors are perfectly matched, and that the zener diodes are likewise matched, since these are all accomplished over a broad temperature range in a well-made integrated circuit. Further, it will be assumed that the transistor current gains are sufficiently large that the base currents can be neglected (although a more complete analysis will show that the base currents are insignificant if the transistors are reasonably well matched and the current gains are larger than about 10). Finally, it will be assumed in certain places that the emitter-base voltages of all transistors are the same regardless of the collector current, both because

this can be made true by suitably choosing the transistor geometries, and because a factor-of-two difference in collector current only results in an emitter-base-voltage variation of approximately three percent.

For zero differential-input voltage, the collector currents of the input-stage transistors, Q_1 and Q_2, will be equal since they are identical devices with the same emitter-base voltages. The collector current of the second-stage biasing transistor, Q_3, can be written as

$$I_{C3} = \frac{V^+ - V_Z - 1/2\, I_{C9} - 2V_{BE}}{R_4} \qquad (1)$$

Similarly, the collector current of the second stage amplifier transistor is

$$I_{C4} = \frac{V^+ - V_Z - V_{BE} - V_{OT}}{R_5} \qquad (2)$$

where V_{OT} is the output voltage.

For $R_1 = R_2$, these two currents will be equal because of the balanced configuration, thus

$$\frac{V^+ - V_Z - 1/2\, I_{C9}R_1 - 2V_{BE}}{R_4} = \frac{V^+ - V_Z - V_{BE} - V_{OT}}{R_5} \qquad (3)$$

With $R_4 = R_5$, Eq. (3) becomes

$$V_{OT} = V_{BE} + 1/2\, I_{C9}\, R_1 \qquad (4)$$

It is now necessary to determine the collector current of the current-source transistor, Q_9. The current in the compensated bias divider for Q_9 is

$$I_{C10} = \frac{V^- - 2V_{BE}}{R_6 + R_7} \qquad (5)$$

The collector current of Q_9 will be

$$I_{C9} = \frac{R_7}{R_8}\, I_{C10}$$

or

$$I_{C9} = \frac{R_7}{R_8} \left[\frac{V^- - 2V_{BE}}{R_6 + R_7} \right] \qquad (6)$$

Equation (4) now becomes

$$V_{OT} = V_{BE} + \frac{R_1 R_7}{2R_8} \left[\frac{V^- - 2V_{BE}}{R_6 + R_7} \right] \qquad (7)$$

It is significant that this equation is independent of the positive supply voltage and dependent on resistor ratios, not absolute values. Using the values in Figure 3,

$$V_{OT} = 0.7V_{BE} + 0.16\,V^- \qquad (8)$$

which gives a nominal output voltage of $1.4V$ with $V^- = 6V$ and zero input voltage. This is a good choice since the threshold voltage of standard logic circuits is between $0.7V$ and $1.7V$. Actually, the exact output voltage is only a secondary consideration since the voltage gain of the comparator is quite high (1700), so that the difference between a $1.4V$ and a $0.7V$ threshold is only about $400\mu V$ at the input.

It can be seen from Eq. (8) that the output offset voltage is dependent on the negative supply voltage. The differential of Eq. (8) is

$$\Delta V_{OT} = 0.16\Delta V^- \qquad (9)$$

It is evident from Eq. (9) that a 10% change in V^- would give an offset change of 60 μV for a gain of 1,700. The sensitivity of offset to production variations of V_{BE} in Eq. (8) is in the order of 20 μV, which is totally negligible.

The above analysis has assumed that all resistors are perfectly matched in ratio. In a practical microcircuit, however, some mismatches are to be expected. Table I shows the effect of a 10% change in individual resistor values on the input offset voltage. It can be seen that the matching of R_1 with R_2 is by far the most significant, giving a 2.5 mV offset for a 10% mismatch. However, matches of about 2%, which would give a 0.5 mV offset, are normally obtained in an integrated circuit. Therefore, the mismatching normally seen does not cause significant imbalance. Similarly, it can be shown that the current-gain mismatches usually obtained do not greatly affect offset except in the input stage, where the offset current is determined by the current-gain match.

Finally, the effect of temperature on the output offset voltage (V_{OT}) should be considered. From Eqs. (7) and (8), it can be seen that the only temperature-sensitive parameter is V_{BE}, since resistors hold their initial room-temperature ratios exceedingly well over a wide temperature range. It should be noted, however, that this temperature sensitivity is in the right direction to help compensate for the

TABLE I

CHANGE IN INPUT-REFERRED OFFSET VOLTAGE FOR A 10% DECREASE IN INDIVIDUAL RESISTOR VALUES

RESISTOR	NOMINAL VALUE (Ω)	CHANGE IN OFFSET VOLTAGE
R_1	500	+2.4
R_2	500	−2.4
R_4	3900	−0.24
R_5	3900	+0.04
R_6	1700	+0.05
R_7	68	−0.05
R_8	100	+0.05

temperature sensitivity of threshold voltage in logic circuits. Since the temperature variations of logic threshold voltage do not have a significant effect on offset, this is not too important; but at least the temperature sensitivity indicated by Eq. (8) improves rather than degrades the performance of the comparator.

The next step in the analysis is to obtain an expression for the voltage gain so that the factors influencing this parameter can be determined. In the analysis, the output conductance of the transistors will be neglected and they themselves considered to be unilateral. This does not introduce any appreciable error when double-diffused silicon transistors are used at relatively low voltages, as they are here. The terms employed to describe the transistors are the AC current gain and the idealized transconductance obtained by differentiating the expression

$$I_C = I_S\,exp\left(\frac{qV_{BE}}{kT}\right) \qquad (10)$$

which gives

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT} \qquad (11)$$

where I_C is the DC collector current, q is the charge of an electron, k is Boltzmann's constant, and T is the absolute temperature. The emitter contact resistance, which is responsible for the difference between the actual and the ideal transconductance, will also be considered. These parameters were chosen to describe the transistors because

they are easily related to mask design and processing variables.

With reference to Figure 3, the differential voltage gain of the input stage is

$$A_{V1} = \frac{R_2}{\frac{kT}{qI_{C1}} + R_{E1}} \qquad (12)$$

where R_{E1} is the emitter contact resistance of Q_1.

The voltage gain of the second stage amplifier (Q_4) is likewise

$$A_{V2} = \frac{R_5}{\frac{kT}{qI_{C4}} + R_{E4}} \qquad (13)$$

The second-stage configuration delivers the full differential gain of the input stage to the second-stage amplifier. Consequently, the over-all gain will be the product of A_{V1} and A_{V2}. The second stage, however, does load the input stage to some degree. The input resistance of the second stage is

$$R_{IN4} = \left[\frac{kT}{qI_{C4}} + R_{E4} \right] h_{fe} \qquad (14)$$

Hence, the over-all gain is

$$A_{VO} = A_{V1}A_{V2} \left[\frac{R_{IN4}}{R_2 + R_{IN4}} \right]$$

$$= \frac{R_2 R_5}{\left[\frac{kT}{qI_{C1}} + R_{E1} \right] \left[\frac{R_2}{h_{fe}} + \frac{kT}{qI_{C4}} + R_{E4} \right]} \qquad (15)$$

The input-stage collector current is one-half the current-source current, I_{C9}, given by Eq. (6), while the second-stage collector current, I_{C4}, is given by Eq. (2).

The sensitivity of the voltage gain to transistor current gains can be estimated by assuming typical values for other variables and plotting gain as a function of h_{fe} (see Figure 7). The figure shows that the gain is not greatly affected by h_{fe} variations as long as h_{fe} is above a minimum value. It is also interesting that the gain given by Eq. (15) is dependent only on resistor ratios if $R_E << kT/qI_C$ (which is certainly true for acceptable transistors).

An exact analysis of the temperature dependence of gain is quite cumbersome, but considerable insight into the functioning of the device can be obtained by looking at the effect of temperature on the individual terms in Eq. (15). The variation in resistance values can be neglected since, to a first-order approximation, the gain depends only on resistor ratios. The factors that do cause a significant temperature variation of gain are the current gain, which has a positive temperature coefficient, and the transconductance terms, which have a negative temperature coefficient. For high current gains, the transconductance terms dominate, giving a negative temperature coefficient of gain; but for lower current gains, the temperature coefficient could be positive because of the dominance of the current-gain term. In this case, the temperature coefficient of gain would be positive at low temperatures where the current gain is low but negative at high temperatures where the current gain is higher. Figure 8 shows the gain variation with temperature for a typical μA710.

Using Eq. (15), the change in gain with change in positive supply voltage can be determined by

$$\frac{\partial A_V}{\partial V^+} = \frac{R_2 R_5 \frac{kT}{qI_{C4}^2} \frac{\partial I_{C4}}{\partial V^+}}{\left[\frac{kT}{qI_{C1}} + R_{E1} \right] \left[\frac{R_2}{h_{fe}} + \frac{kT}{qI_{C4}} + R_{E4} \right]^2} \qquad (16)$$
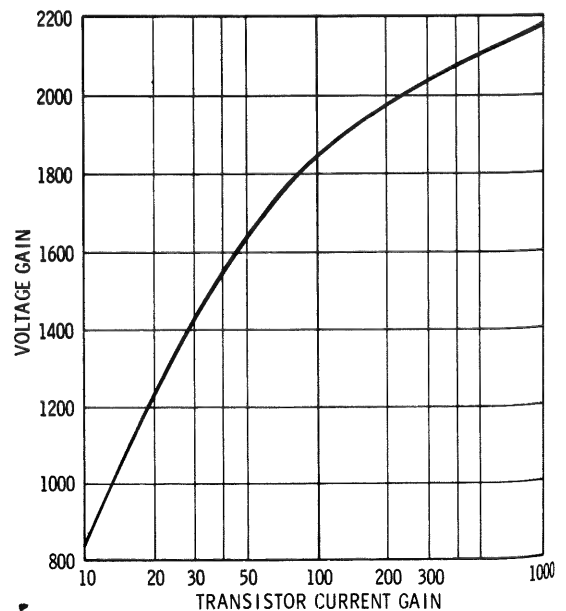
Fig. 7 Calculated Voltage Gain as a Function of Transistor Current Gain.
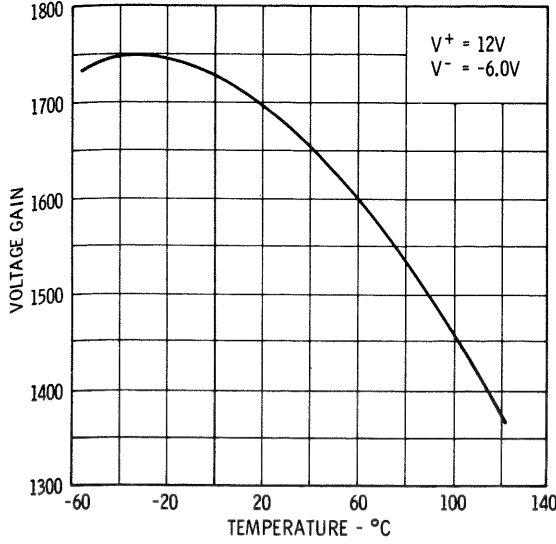
Fig. 8 Voltage Gain as a Function of Ambient Temperature.

Substituting Eq. (15),

$$\frac{\partial A_V}{\partial V^+} = \frac{A_{VO}\dfrac{kT}{qI_{C4}{}^2}\dfrac{\partial I_{C4}}{\partial V^+}}{\dfrac{R_2}{h_{fe}} + \dfrac{kT}{qI_{C4}} + R_{E4}} \qquad (17)$$

From Eq. (2),

$$\frac{\partial I_{C4}}{\partial V^+} = \frac{1}{R_5}$$

and Eq. (17) becomes

$$\frac{\partial A_V}{\partial V^+} = \frac{A_{VO}}{\left(V^+ - V_Z - V_{BE} - V_{OT}\right)} \cdot \frac{\dfrac{kT}{qI_{C4}}}{\left(\dfrac{kT}{qI_{C4}} + \dfrac{R_2}{h_{fe}} + R_{E4}\right)} \qquad (18)$$

where Eq. (2) has been substituted for one of the I_{C4} terms. The second factor in Eq. (18) is the ratio of the actual second stage gain to the idealized transconductance-limited gain and has a value less than one (typically 0.6 but less for low-gain devices). Hence,

$$\frac{\partial A_V}{\partial V^+} < \frac{A_{VO}}{V^+ - V_Z - V_{BE} - V_{OT}} \qquad (19)$$

Similarly, the change in gain with changes in negative supply voltage can be determined:

$$\frac{\partial A_V}{\partial V^-} = \frac{R_2 R_5 \dfrac{kT}{qI_{C1}{}^2}\dfrac{\partial I_{C1}}{\partial V^-}}{\left[\dfrac{kT}{qI_{C1}} + R_{E1}\right]^2 \left[\dfrac{R_2}{h_{fe}} + \dfrac{kT}{qI_{C4}} + R_{E4}\right]} \qquad (20)$$

With Eq. (15) substituted,

$$\frac{\partial A_V}{\partial V^-} = \frac{A_{VO}\dfrac{kT}{qI_{C1}{}^2}\dfrac{\partial I_{C1}}{\partial V^-}}{\dfrac{kT}{qI_{C1}} + R_{E1}} \qquad (21)$$

Taking $I_{C1} = \dfrac{I_{C9}}{2}$, where I_{C9} is given by Eq. (6),

$$\frac{\partial I_{C1}}{\partial V^-} = \frac{R_7}{2R_8 (R_6 + R_7)} \qquad (22)$$

Hence,

$$\frac{\partial A_V}{\partial V^-} = \left(\frac{A_{VO}}{V^- - 2V_{BE}}\right)\left(\frac{\dfrac{kT}{qI_{C1}}}{\dfrac{kT}{qI_{C1}} + R_{E1}}\right) \qquad (23)$$

where one of the I_{C1} terms has been replaced by $I_{C9}/2$, given by Eq. (6). The second term of Eq. (23) is, like that of Eq. (18), the ratio of the actual input stage gain to the idealized gain. Therefore,

$$\frac{\partial A_V}{\partial V^-} < \frac{A_{VO}}{V^- - 2V_{BE}} \qquad (24)$$

Equations (18) and (24) give the maximum gain changes that can be expected for a change in supply voltages. From the derivation of these equations, it can be seen that the decrease in gain for a decrease in supply voltages will be least for the lowest gain device, which is good since it is only

desired to maintain a minimum gain with a comparator. Figure 9 shows the variations in gain with supply voltages measured on a typical device.
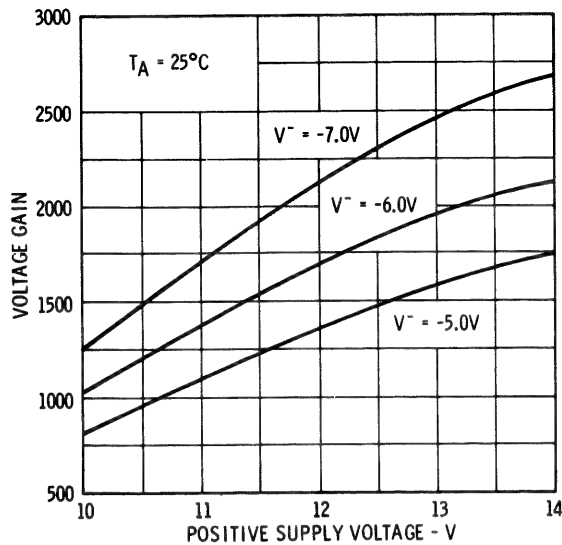
Fig. 9 Voltage Gain as a Function of Supply Voltages.

PERFORMANCE

Typical electrical chacteristics of the comparator are summarized in Table II, which illustrates the excellent matching and performance available with present-day monolithic construction.

The transfer function of a comparator describes its operation in quite general terms. The transfer function of the μA710 is given in Figure 10, and the μA711 in Figure 11.

As shown in Figure 12, the power dissipation varies with signal level and is therefore specified on the data sheet as a maximum for the entire range of input-signal conditions. Figures 13 and 14 show the power consumption as a function of temperature for the μA710 and μA711, respectively. Note that, although the μA711 performs almost the same function as two μA710's, its power consumption is only 45% higher.

TABLE II

TYPICAL PERFORMANCE FIGURES FOR THE μA710

PARAMETER	CONDITIONS $(T_A = +25°C, V^+ = 12.0V, V^- = -6.0V$ unless otherwise specified)		UNITS
Input Offset Voltage	$R_S \leqslant 200\Omega$	0.6	mV
Input Offset Current		0.75	μA
Input Bias Current		13	μA
Voltage Gain		1700	
Output Resistance		200	Ω
Output Sink Current	$\Delta V_{in} \geqslant 5$ mV, $V_{out} = 0$	2.5	mA
Response Time [Note 3]		40	ns
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$:			
Average Temperature Coefficient of Input	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$	3.5	μV/°C
Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$	2.7	μV/°C
Input Offset Current	$T_A = +125°C$	0.25	μA
	$T_A = -55°C$	1.8	μA
Average Temperature Coefficient of Input	$T_A = 25°C$ to $T_A = +125°C$	5.0	nA/°C
Offset Current	$T_A = 25°C$ to $T_A = -55°C$	15	nA/°C
Input Bias Current	$T_A = -55°C$	27	μA
Input Voltage Range	$V^- = -7.0V$	±5.0	V
Common Mode Rejection Ratio	$R_S \leqslant 200\Omega$	100	dB
Differential Input Voltage Range		±5.0	V
Positive Output Level	$\Delta V_{in} \geqslant 5$ mV, $0 \leqslant I_{out} \leqslant 5.0$ mA	3.2	V
Negative Output Level	$\Delta V_{in} \geqslant 5$ mV	−0.5	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{in} \geqslant 5$ mV, $V_{out} = 0$	1.7	mA
	$T_A = -55°C$, $\Delta V_{in} \geqslant 5$ mV, $V_{out} = 0$	2.3	mA
Positive Supply Current	$V_{out} \leqslant 0$	5.2	mA
Negative Supply Current		4.6	mA
Power Consumption		90	mW

Fig. 10 μA 710 Voltage Transfer Characteristic.

Fig. 11 μA 711 Voltage Transfer Characteristic.

Fig. 12 μA 711 Power Consumption as a Function of Signal Level.

Fig. 13 μA 710 Power Consumption as a Function of Ambient Temperature.

Fig. 14 μA711 Power Consumption as a Function of Ambient Temperature.
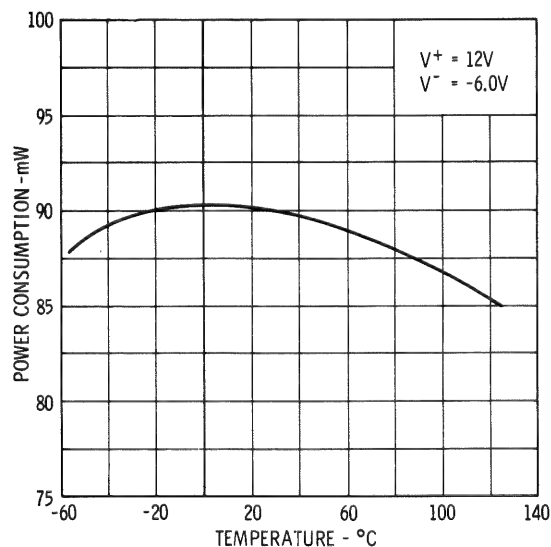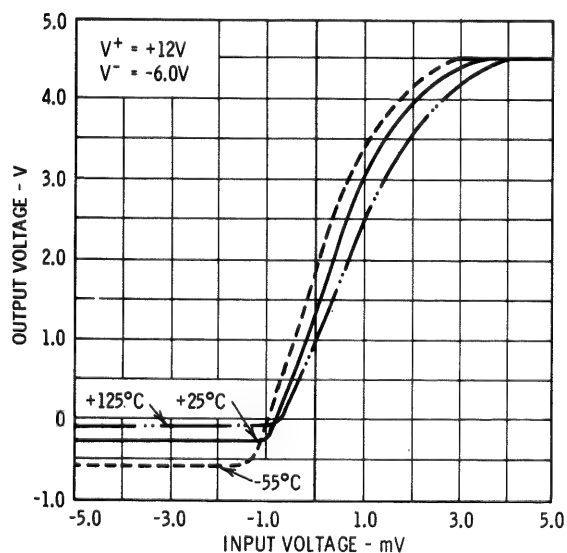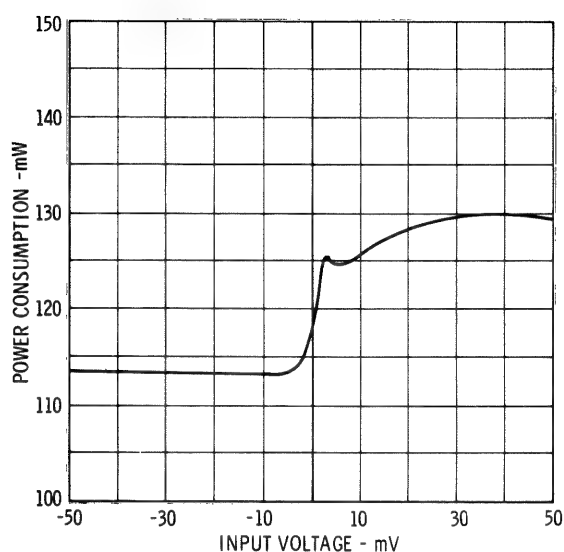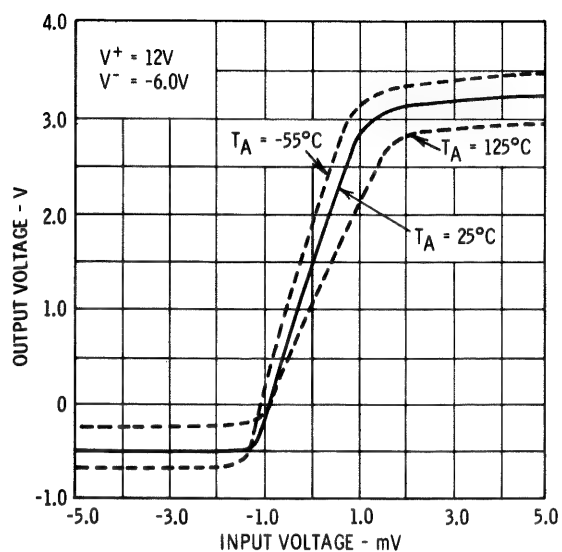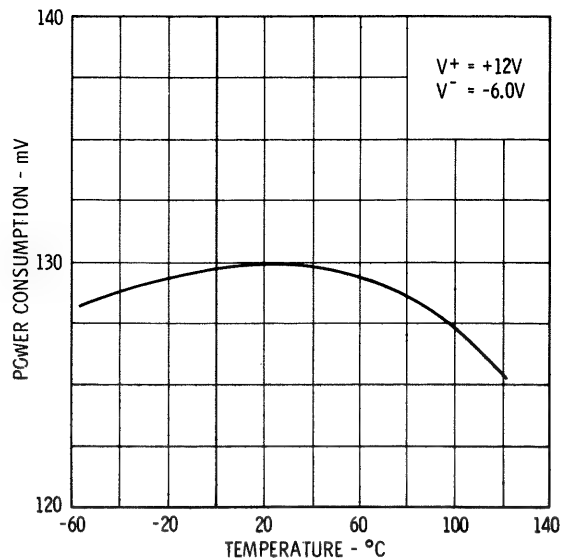
Fig. 15 Output Voltage Levels as a Function of Ambient Temperature.

The questions to be answered by a set of specifications, in addition to the usual ones of supply voltage, power dissipation and absolute maximum ratings, are (1) the accuracy with which the comparator can distinguish between the input signal and the reference signal, and the effect of source resistance on accuracy; (2) how rapidly the comparator can make this distinction and what influence the speed of a decision has on accuracy; and (3) the ability of the comparator to drive different types of logic loads.

DC ACCURACY

The first question can be disposed of by defining the input offset voltage as the voltage required between the comparator input terminals to drive the output to the threshold voltage of the logic. This is in contrast to the definition for an operational amplifier, which is designed to have zero output for zero input. When the output is at the logic threshold voltage, a very small change in input voltage will cause the output of the logic circuit to swing from zero to a one state. It is not necessary for the comparator output to swing from the zero to one state as this does not provide any additional logic output, only more noise immunity. The output offset voltage of the comparator has approximately the same temperature coefficient as the threshold of the logic, as displayed in Figure 15.
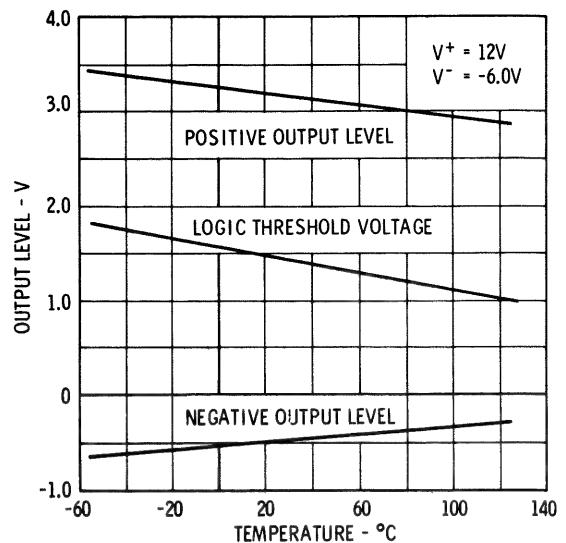
The fact that the output of the comparator matches the logic allows a lower gain with no loss in accuracy and permits the gain of the logic circuit to be multiplied by the gain of the comparator in determining over-all resolution. This gives, for example, an equivalent gain of 50,000 when the μA710 is operated with Fairchild $DT\mu L$. This is important in that additional gain stages would not only complicate the comparator, but make it slower as well. This combined gain is high enough, with practically all logic circuits, that the voltage gain does not usually need to be considered in determining DC accuracy — the offset voltage alone is enough.

The effect of source resistance on the accuracy can be taken into account by adding to the offset voltage the additional differential offset produced by (1) the offset current flowing through the source resistors when the DC resistances seen by the two input terminals are equal, or by (2) the input bias current when the input resistances are very much different. The variations of input offset current and bias current with temperature are given in Figure 16 and 17, respectively. To eliminate the necessity of using worst-case values for offset voltage and offset current, the offset voltage is specified on the data sheet for the case where the resistances on each input are equal to or less than a given amount.

Fig. 16 Input Offset Current as a Function of Ambient Temperature.
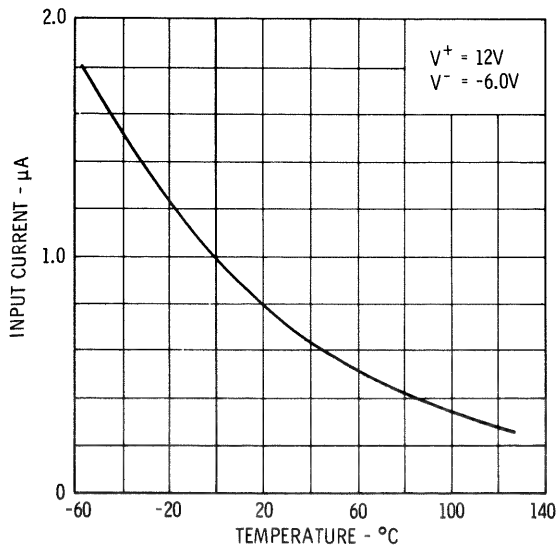
Fig. 17 Input Bias Current as a Function of Ambient Temperature.

The use of input resistance to determine loading is not valid with a comparator. The input impedance varies rapidly as the differential input voltage goes through zero, and is in excess of $1M\Omega$ for input voltages greater than a couple hundred mV. What should be considered is the effect of the input current, which alternately switches between the two input terminals for large differential input voltages. The maximum change in input current is from zero to twice the quiescent bias current specified on the data sheet.

RESPONSE TIME

The second question is a little more difficult, as response time can be defined in many ways. A worst-case situation would be where the comparator is used to determine the height of a large pulse. A good example is the situation in which a DC reference signal (say 0.1 volt) is applied to one comparator input and a step function is applied to the other.
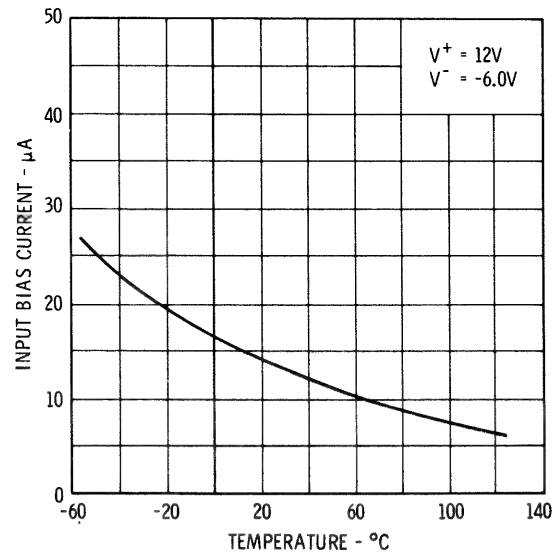
Before the step function is applied, the comparator is completely saturated in one direction by the reference voltage (the comparator will actually reach complete saturation with less than $100mV$ across the input terminals). Some time after the step function arrives, the comparator output will reach the logic threshold voltage if the step height differs from the reference voltage only by the offset voltage. In the absence of overshoot, however, this length of time would supposedly be infinite, or at least difficult to determine. Therefore, the response time must be measured with some additional voltage overdrive in order to have any real meaning. That is, the input step height must be increased by some amount over that required to bring the output from saturation to the logic threshold voltage. The response time can then be defined as the interval between the application of the input step and the time when the output crosses the logic threshold voltage. The error encountered in making the decision within this period of time is then the amount of overdrive required. This definition eliminates offset voltage from the speed measurement in order to provide more flexibility in the interpretation of a specified parameter. This response time will be relatively independent of the step height and reference voltage as long as they are in excess of 100 mV. Smaller step heights will give faster response times since the comparator will not be thoroughly saturated.

Figure 18 gives the response time of the μA710 for a 100 mV input step and overdrives of 2, 5, 10, and 20 mV with a positive-going output. The response times are 65, 40, 28, and 20 ns, respectively, for these overdrives. For smaller input steps, the response time will be somewhat faster for the same overdrive since the internal circuitry of the comparator will not be completely saturated before the pulse is applied. Larger input steps do not materially affect response time since the comparator does not go any deeper into saturation with input voltages larger than 100 mV. Measurement of response time in the above manner permits a determination of how much input-referred error is encountered when the comparison is made in a short time interval.
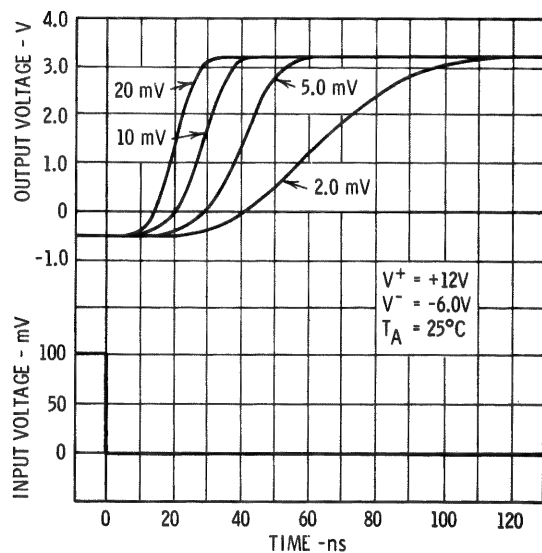
Fig. 18 Response Time for Various Input Overdrives.

With the μA711, the speed of the strobe circuitry is also important. Strobe release time can be defined as the time required for the output to rise to the logic threshold voltage after a positive step function has been applied to the strobe terminal (the strobe signal does not actually have to be a step function as long as it is faster than the measured strobe release time). This definition assumes a DC input signal that will give a positive output when the strobe is released. When the strobe voltage returns to zero, it will drop the voltage on the base of the output emitter-follower at a speed which is limited only by the fall time of the strobe voltage. Therefore, the strobe fall time is not pertinent.

The strobe release time of the μA711 is shown for various input conditions in Figure 19. The O mV curve is for an input condition that would put the output at the logic threshold voltage under DC conditions. The curve below that is for 1 mV less input voltage, and gives an indication of the feed-through of the strobe pulse when the comparator is barely turned off (it is necessary to wire the comparator into the circuit minimizing the stray capacitance between the strobe terminal and the inputs in order to keep this feed-through small). The 2 mV and 5 mV curves represent actual operating conditions and give strobe release times of 14 ns and 10 ns, respectively. In these curves, the output does not rise to the maximum output level because of the clamping action of the strobe circuitry when a low-amplitude strobe pulse is used. The test conditions shown are representative of the case where the comparator is used with Fairchild $RT\mu L$.
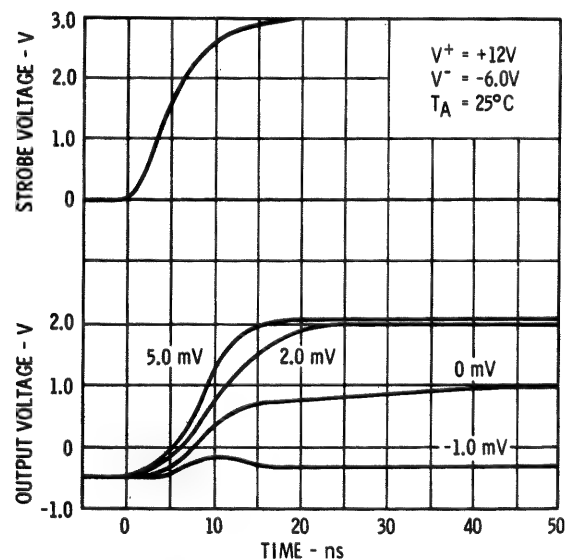
Fig. 19 Strobe Release Time for Various Input Overdrives.

Where time strobing is used in the design of sense amplifiers using the μA711, it often becomes necessary to stretch the strobed output pulse of the sense amplifier in order to make it wide enough to be transmitted over a reasonable line length and trigger the storage circuits. The most straight-forward way of accomplishing this is to use a one-shot multivibrator. However, the accuracy requirements for the stretched pulse do not warrant going to

the complexity of a one-shot, and thus much simpler methods can be used. Figure 20 shows a possible alternative. Loading the comparator with a capacitor on the output will stretch the output pulse. This occurs because the output emitter-follower can charge the load capacitance rapidly, but the output current sink gives a limited rate of discharge. Normally, the strobe width is sufficient to trigger the logic circuits, the only fear being that the pulse will be degraded by cable capacitance. With the μA711, however, the capacitances encountered in transmission make the output pulse longer rather than shorter, so no discrete capacitor need be used. In the test circuit for Figure 20, an external resistor is connected between the output and the negative supply to give the μA711 a fan-out of one with DTL. This gives considerably less pulse stretching than would be seen with the μA711 alone, and somewhat more than would be obtained with a μA710 alone, due to the difference in sink currents.

strobe pull-down time is shorter than the release time on the base of the output emitter-follower, since a negative-going strobe pulse into the zener diode will forcibly pull down that point. Therefore, the response time for a negative-going output will always be faster than that for a positive output, which depends on the delay time of the input stage and the storage time of the second stage, as well as the feedback and output capacitances of the second stage. Thus, the positive response time is the one that is specified since it is most indicative of overall device performance; the negative-going response times are limited more by the characteristics of the load than by those of the circuit, and are described by Figure 20.

The DC common mode rejection ratio of the comparator is typically 100dB, which makes the comparison accuracy quite independent of the actual level of the signals being compared. Figure 21 shows its variation with ambient temperature.

Fig. 20 Output Pulse Stretching with Capacitive Loading.

Fig. 21 Common Mode Rejection Ratio as a Function of Ambient Temperature.

It is worthwhile to point out here that the response time and the strobe release time for negative-going outputs were not described previously because they are limited by this pulse stretching characteristic. For a negative-going output, the storage time of the second stage is eliminated; additionally, the second-stage transistor is able to discharge its output capacitance faster than the collector load resistor can charge it. Similarly, the

For very high-speed signals, a more significant parameter is the common mode rejection at high frequencies. If this is expressed in terms commonly used in connection with differential amplifiers, it is difficult to interpret for a comparator. However,

Figure 22 shows a pulse test and its result, which demonstrates that the comparator is affected little by fast common mode signals, even in the center of its active region. That is, the error encountered due to any reasonable high-frequency common mode signals is small with respect to the offset voltage and speed resolution. At any time other than when the comparison is being made, common mode signals can be completely neglected.
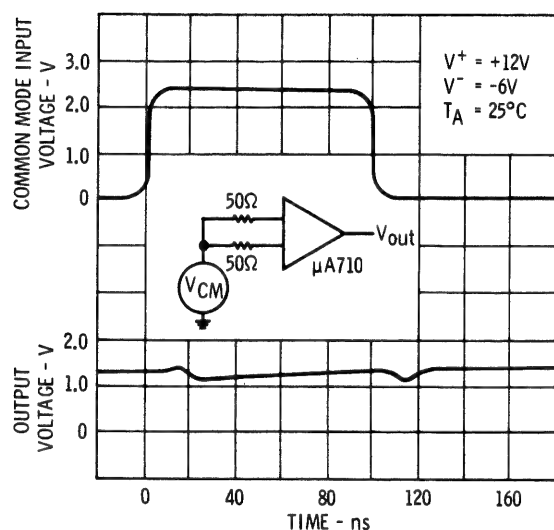
Fig. 22 Common Mode Pulse Response.

LOGIC COMPATIBILITY

Specification of logic compatibility can be approached by ensuring that the comparator can drive the logic into full saturation under worst-case conditions. After this is done, it is necessary to take into account only the difference between the threshold voltage of the logic used and the logic threshold specified for the comparator to determine the influence on offset voltage. With most standard logic circuits the effect of differing logic threshold voltages on offset is less than $1\ mV$, so even this can be neglected in the majority of applications.

In general, performance is guaranteed by specification of positive and negative output levels, with and without load, which are compatible with the logic used. The following information is useful in establishing the limitations of the comparator, the circuitry to be used, and the operating conditions under which the comparator is to be specified.

When operated with standard resistor-transistor logic (Fairchild $RT\mu L$), the comparator is roughly equivalent to a buffer element and can drive a large fan-out. However, since the comparator operates from a higher supply voltage than a buffer, the internal dissipation with a one-level output can become excessive. In addition, the large output current available from the comparator can overdrive the logic and cause excessive storage. For these reasons, it is advisable to insert a resistor in series with the output of the comparator to limit the current. Recommended values with both the $\mu A710$ and $\mu A711$ are $1.5\ k\Omega$ for a fan-out of one, 510Ω for a fan-out of two and 270Ω for a fan-out of three. A small ($100pF$) capacitor can be connected in parallel with this resistor to increase the speed of the logic.

Essentially the same rules apply for low power resistor-transistor logic. Recommended values of series resistance are $4.7k\Omega$ for a fan-out of one, $2.2k\Omega$ for a fan-out of two, and $1.3k\Omega$ for a fan-out of three. Again, a small capacitance can be added across the resistor for increased speed.

When operating with diode-transistor logic (Fairchild $DT\mu L$), the limiting factor is the ability of the comparator to supply the required sink current. The $\mu A710$ can drive a $DT\mu L$ fan-out of one, but an external $3.6k\Omega$ resistor must be added between the output and the $-6V$ supply for a fan-out of two, and a $2.2k\Omega$ resistor must be used for a fan-out of three. With the $\mu A711$, at least four devices must be OR'ed before they can provide enough sink current for a $DT\mu L$ fan-out of one. If a single comparator is used to drive a $DT\mu L$ circuit, a $5.6k\Omega$ resistor must be inserted between the output terminal and the $-6V$ supply for a worst-case fan-out of one. For a fan-out of two, a $2.4k\Omega$ resistor must be used.

With transistor-transistor logic (Fairchild $TT\mu L$) the same rules regarding sink current used with $DT\mu L$ must be followed. The high-level reverse current encountered with $TT\mu L$ can be disregarded because both the $\mu A710$ and $\mu A711$ are able to supply considerable current in this direction and because the permissible fan-out is low, being restricted by the available sink current.

Both the μA710 and the μA711 can be used to drive complementary-transistor logic (Fairchild $CT\mu L$) directly. The fan-out, however, is limited to one, or perhaps two, by the ability of the comparator to supply the required current at the output high level.

The one remaining point to be covered on logic compatibility is the strobe of the μA711. In the low state, it is necessary to sink 1.2 mA, typically, at the strobe terminal to hold one side of the comparator off. This current is required only if the side being held off is turned on internally. Hence, if the comparator is used in an application where only one side can be on at a time, it is only necessary to provide sink current for one strobe—otherwise, it is necessary to sink 2.4 mA to hold both sides off. In the high state, the strobe does not load the logic appreciably. The high level required to release the strobe depends on the type of logic used in that the output of the comparator will be clamped to a voltage that is one diode drop less than the strobe voltage.

Because of stray capacitance effects, it is not advisable to leave the strobe terminal floating, particularly in high-speed circuits. The strobe terminal should be connected to the logic supply voltage (or any other voltage less than $+6V$) if it is not being used.

BASIC COMPARATOR APPLICATION

The basic circuit for using the comparator is shown in Figure 23(a). A reference voltage between $\pm 5V$ is inserted on one input and the signal is inserted on the other. When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected. Figure 23(b) shows the general input/output characteristic.

a. CIRCUIT   b. TRANSFER FUNCTION
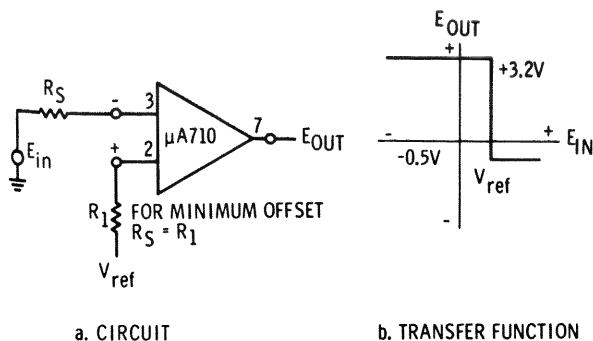
Fig. 23 The Basic Level Detector Circuit.

The circuit has a variety of uses. It can be employed as a voltage comparator in A/D converters, where one input is driven by the analog input signal and the other by a ladder network. It also has use as a tape or drum memory sense amplifier and threshold detector. Other applications include a high noise immunity buffer for going from high level logic into low level integrated circuits, or a pulse-shape restorer in digital circuits.

In order to achieve maximum accuracy in the circuit of Figure 23, the DC resistance of the signal source (R_S) should equal the source resistance of the reference voltage (R_1). When this is done, the bias currents of the two inputs produce nearly equal drops across these source resistances, which should be made as low as possible, preferably less than 200Ω, for best performance. Any increase in offset is then due only to the offset current, which is usually more than an order of magnitude less than the bias current.

Although the input voltage range of the μA710 and μA711 is $\pm 5V$, the maximum voltage between the inputs is also $\pm 5V$. If one of the inputs is at $+5V$, for example, the other can only be driven as low as ground potential without exceeding the differential input voltage limit. It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and input bias current.

Exceeding the absolute maximum positive input voltage limit of the device ($+7V$) will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result. When the transistor on the inverting input saturates, for example, it no longer functions as an inverting amplifier stage; instead, it makes a direct connection between the input and the base of the second-stage transistor, so that the inverting input becomes a non-inverting input. The negative limit of the input voltage range is specified at $-5V$, but it is necessary to increase the negative supply voltage to $-7V$ to ensure that the input stage current source does not saturate at $-55°C$, causing improper operation.

Some attention to power supply bypassing is required with both the μA710 and μA711. These devices are multi-stage amplifiers with gain to several hundred *MHz*. Long, unbypassed supply leads or sloppy layouts can therefore cause oscillation problems. Bypassing with electrolytic or tubular paper capacitors is ineffective. What is recommended is that both the positive and negative supplies be bypassed to ground using low-inductance, disc-ceramic capacitors (0.01 μF) located as close as practical to the device. A neat physical layout, keeping the input away from the output, is also important. Additionally, the strobe of the μA711 should be kept away from the inputs if fast-rise strobe pulses are used. The strobe terminal, if unused, should not be left floating in high-speed circuits because of stray capacitive effects.

One side of a μA711 can be used in much the same manner as a μA710. However, the inputs of the unused side should be grounded so that the input current source transistor on that side does not saturate and disrupt the bias divider. It is also advisable to ground the strobe terminal to prevent interaction between the unused side and the active side.

Many other circuits using the comparators are given in the applications section, Chapter 13.

THE μA726 TEMPERATURE-STABILIZED TRANSISTOR PAIR

Monolithic integrated circuits can provide excellent DC amplifier performance due to the close component matching and thermal coupling inherent in the manufacturing method. Offset voltages of 1-2 mV and thermal drifts of 3-10 $\mu V/°C$ are possible without adjustment or compensation of circuit elements. These limits are imposed by the degree of match that can be obtained with an integrated transistor pair with reasonable yields. Improved drift performance requires either complicated temperature compensation adjustments, chopper stabilization, or temperature stabilization.

Temperature compensation adjustments should be avoided in an integrated circuit because adjustments on the chip are expensive and difficult to make; also, the testing necessary to verify their success requires methods that are not compatible with high-volume production. Chopper stabilization is a more realistic solution to low-drift DC performance, particularly if MOS FET's are used for the chopper circuitry. However, chopper-stabilized amplifiers are large and complex, have severe drawbacks with respect to overload recovery and reliability, and usually have only one input available.

Temperature stabilization of the critical components can be achieved by putting them in an oven or using individual heaters on each device package, but the heater power and size are often prohibitive. If, however, the critical components can be integrated in a single monolithic chip along with a temperature-regulator circuit for stabilization, significant advantages can be realized in terms of size, cost, and reliability. The μA726 is a device in which the most critical components of a DC amplifier, the input differential pair, are temperature-stabilized in this manner, achieving offset voltage drifts on the order of 0.2 $\mu V/°C$ over the full military temperature range.

CIRCUIT DESCRIPTION

A schematic diagram of the temperature-stabilized differential pair is given in Figure 1. The basic operation of the temperature-controller is
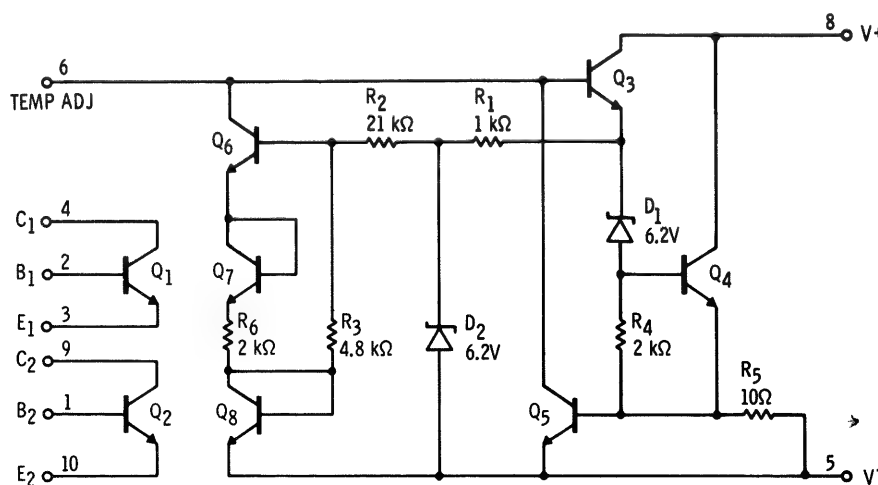
Fig. 1 Schematic of the μA 726.

as follows: changes in the chip temperature are sensed by Q_6 and Q_7, which develop a control voltage across an external temperature-control resistor connected to the collector of Q_6; this control voltage is applied to the base of Q_4 via Q_3 and D_1 and acts to change the collector current of Q_4 (and hence the power dissipation) in a direction such that the chip temperature remains constant. Q_4 is a large-geometry transistor designed to distribute the power dissipation evenly across one end of the chip to minimize thermal gradients between the differential pair transistors (Q_1 and Q_2) located at the opposite end of the chip (see the photomicrograph of Figure 2). Transistor Q_3 supplies the current for D_1 and R_1, and D_2 supplies the voltage divider R_2, R_3, and Q_8. Transistor Q_5 limits the initial turn-on current of the device to approximately 60 mA, so that the chip temperature stabilizes very rapidly, usually to within $1°C$ in less than one second. A curve of turn-on current as a function of time is shown in Figure 3.

In determining the amount of temperature control present in the circuit, it will be assumed that the matching of the resistors and active devices is perfect, and that the transistor current gains are high enough that the base currents can be neglected. This is normally accomplished over a wide temperature range in an integrated circuit, and is especially true for the $\mu A726$, where the chip temperature is held relatively constant. A simplified schematic of the temperature regulator is shown in Figure 4.
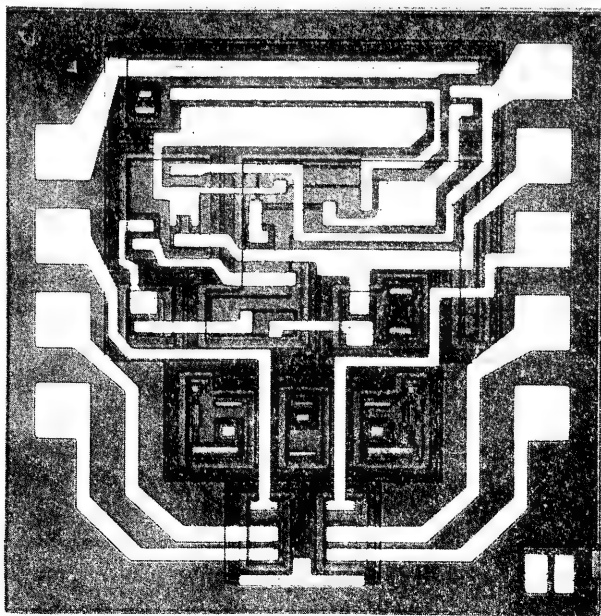
Fig. 2 Photomicrograph of the μA 726.
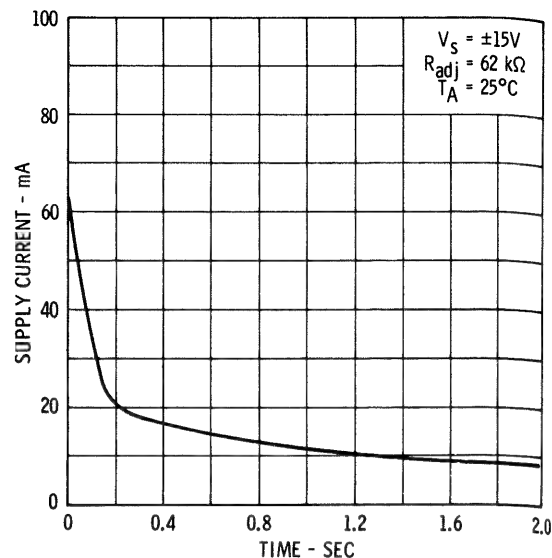
Fig. 3 Turn-On Current as a Function of Time.
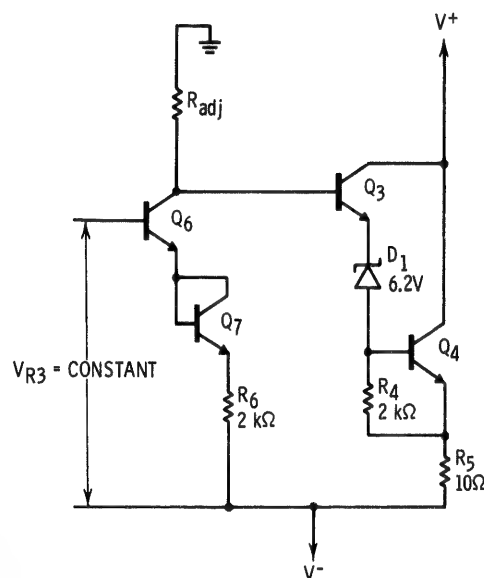
Fig. 4 Simplified Schematic of Temperature-Control Circuit.

Since the voltage across R_3 is held constant by zener D_2, chip temperature changes sensed by the base-emitter voltages of Q_6 and Q_7 (approx. $-2mV/°C$) produce a change in the collector current of Q_6 equal to

$$\Delta I_{C6} = -\frac{2}{R_6}\left(\frac{\Delta V_{BE}}{\Delta T_C}\right)\Delta T_C \qquad (1)$$

The control voltage developed across the external temperature-adjust resistor, R_{adj}, is transferred to the base of the power-dissipating transistor (Q_4) by a level-shifter composed of Q_3 and D_1. Hence

$$-\Delta I_{C6}R_{adj} = \Delta I_{C4}R_5 + \Delta V_{BE4} \qquad (2)$$

The change in base-emitter voltage of Q_4 for a change in collector current is

$$\Delta V_{BE4} = \frac{kT_c}{q} \ln\left(1 + \frac{\Delta I_{C4}}{I_{C4}}\right) \qquad (3)$$

and thus

$$\frac{2R_{adj}}{R_6}\left(\frac{\Delta V_{BE}}{\Delta T_C}\right)\Delta T_C = \Delta I_{C4}R_5 + \frac{kT_c}{q}\ln\left(1 + \frac{\Delta I_{C4}}{I_{C4}}\right) \qquad (4)$$

The power dissipation in Q_4 must compensate for any change in the ambient temperature; therefore

$$\Delta I_{C4}\,(V^+ - V^-)\,\Theta_{JA} = -\Delta T_A \qquad (5)$$

where Θ_{JA} is the chip-to-ambient thermal resistance, and it is assumed that $\Delta T_A >> \Delta T_C$. The change in chip temperature is then found from Eqs. (4) and (5):

$$\Delta T_C = -\frac{R_6}{2R_{adj}\left(\frac{\Delta V_{BE}}{\Delta T_C}\right)}\left[\frac{R_5\Delta T_A}{\Theta_{JA}\,(V^+ - V^-)}\right.$$

$$\left. -\frac{kT_c}{q}\ln\left(1 - \frac{\Delta T_A}{I_{C4}\Theta_{JA}\,(V^+ - V^-)}\right)\right] \qquad (6)$$

Eq. (6) is highly nonlinear for ambient temperatures approaching the chip temperature since large changes in V_{BE4} are required at low collector currents. This gives the characteristic shown in Figure 5, with a total change in chip temperature of 3°C for an ambient temperature range of −55°C to +125°C. Also shown in Figure 5 is the variation of power supply current with ambient temperature.

Supply voltage variations produce an approximate change in control current of

$$\Delta I_{C6} = \frac{\Delta V}{R_{adj}} \qquad (7)$$
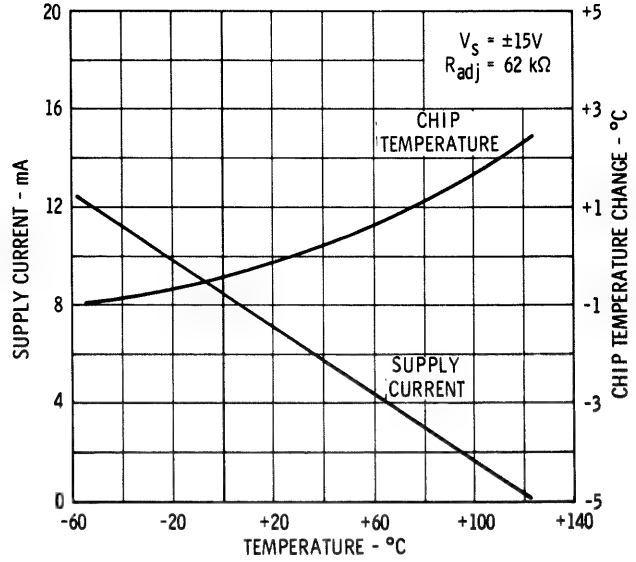
Fig. 5 Chip Temperature and Supply Current.

Hence from Eq. (1), the change in chip temperature will be

$$\Delta T_C = -\frac{R_6 \Delta V}{2R_{adj}\left(\frac{\Delta V_{BE}}{\Delta T_C}\right)} \qquad (8)$$

This is about 1°C/% for ±15V supplies, with R_{adj} connected to ground. For applications where operation to +125°C is not required, the temperature of the chip can be lowered and temperature control and supply rejection improved by increasing R_{adj}. Figure 6 shows the recommended value of R_{adj} as a function of maximum operating ambient
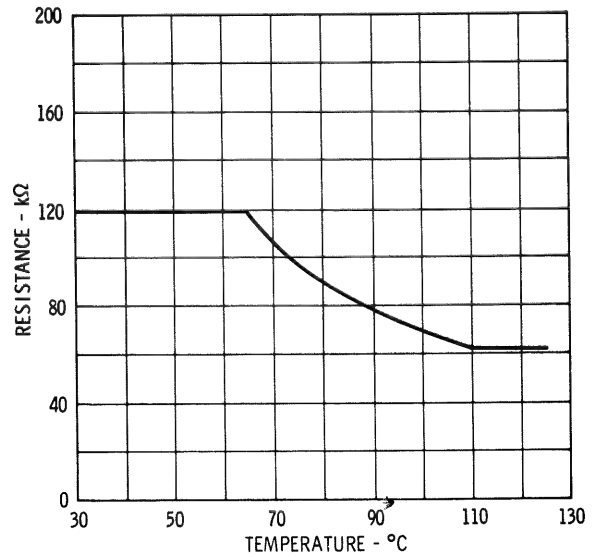
Fig. 6 Recommended R_{adj} versus Maximum Ambient Temperature.

temperature. Lowering the chip temperature decreases the initial voltage offset by about $1\%/°C$ and increases the current offset and input current by about $1\%/°C$ of chip temperature change. Improved temperature control can also be obtained by connecting R_{adj} to the positive supply voltage instead of ground; in this case, the value of the resistor should be increased by about a factor of 3 over the values shown in Figure 6.

PERFORMANCE

Because of the integrated temperature stabilization of the $\mu A726$, unprecedented drift performance can be achieved from the differential pair. Typical electrical characteristics are listed in Table I. By way of comparison, an unstabilized monolithic differential pair having the same initial offset($2.5mV$) will have an offset drift on the order of $10\mu V/°C$. The temperature control circuitry reduces this to about $0.2\mu V/°C$ – an improvement of almost two orders of magnitude. The temperature coefficients of the offset current and base current are also greatly reduced, both because of the temperature control and because the h_{FE} of the transistors is near its maximum value due to the elevated temperature of the chip.

Characteristic curves for the transistors are given in Figures 7 through 9; Figure 7 shows the characteristics at normal operating levels, Figure 8 illustrates operation at high collector voltages, and Figure 9 shows the saturation characteristics. The collector saturation resistance is high because of the topside collector contact required by monolithic construction, the high resistivity used to get good breakdowns, and the high operating temperature. A curve of current gain as a function of operating collector current is given in Figure 10. The current gain peaks at about $1mA$, but remains quite high all the way down to $10\mu A$.

There are several points that must be considered in order to achieve the excellent drift performance possible with the $\mu A726$. When used as the input stage of a DC amplifier, the tracking of the collector resistors, the loading from the input currents of the following stage, and the offset drift of the following stage all contribute to over-all input offset drift, in addition to that from the $\mu A726$ alone. The offset voltage of two matched transistors operating at different collector currents has been shown in previous chapters to be

TABLE I

TYPICAL ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS ($-55°C \le T_A \le +125°C$, $V_S = \pm15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)	VALUE	UNITS
Input Offset Voltage	$10\ \mu A \le I_C \le 100\ \mu A$ $V_{CE} = 5$ V, $R_S \le 50\Omega$	1.0	mV
Input Offset Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V	10	nA
Input Offset Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V	50	nA
Average Input Bias Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V	50	nA
Average Input Bias Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V	250	nA
Offset Voltage Change	$I_C = 10\ \mu A$, 5 V $\le V_{CE} \le 25$ V, $R_S \le 100$ kΩ	0.3	mV
Offset Voltage Change	$I_C = 100\ \mu A$, 5 V $\le V_{CE} \le 25$ V, $R_S \le 10$ kΩ	0.3	mV
Input Offset Voltage Drift	$10\ \mu A \le I_C \le 100\ \mu A$, $V_{CE} = 5$ V, $R_S \le 50\Omega$, $+25°C \le T_A \le +125°C$	0.2	$\mu V/°C$
Input Offset Voltage Drift	$10\ \mu A \le I_C \le 100\ \mu A$, $V_{CE} = 5$ V, $R_S \le 50\Omega$, $-55°C \le T_A \le +25°C$	0.2	$\mu V/°C$
Input Offset Current Drift	$I_C = 10\ \mu A$, $V_{CE} = 5$ V	10	pA/°C
Input Offset Current Drift	$I_C = 100\ \mu A$, $V_{CE} = 5$ V	30	pA/°C
Supply Voltage Rejection Ratio	$10\ \mu A \le I_C \le 100\ \mu A$, $R_S \le 50\Omega$,	25	$\mu V/V$
Low-Frequency Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \le 50\Omega$ BW = .001 Hz to 0.1 Hz	4.0	μV pp
Broadband Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \le 50\Omega$ BW = 0.1 Hz to 10 kHz	10	μV pp
Long-term Drift	$10\ \mu A \le I_C \le 100\ \mu A$, $V_{CE} = 5$ V, $R_S \le 50\Omega$, $T_A = 25°C$	5.0	$\mu V/week$
High Frequency Current Gain	f = 20 MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V	3.5	
Output Capacitance	$I_E = 0$, $V_{CB} = 5$ V	1.0	pF
Emitter Transition Capacitance	$I_E = 100\ \mu A$	1.0	pF
Collector Saturation Voltage	$I_B = 100\ \mu A$, $I_C = 1$ mA	0.5	V

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{I_{C1}}{I_{C2}} \right) \qquad (9)$$

Therefore, if the collector currents of the differential pair are unbalanced by any of the aforementioned factors, and if this unbalance changes with temperature, an equivalent input offset will be produced. The magnitude of the drift depends upon the gain of the stage and is given by

$$\Delta V_{OS} = \frac{kT_C}{q} \left(\frac{\Delta R_C}{R_C} + \frac{\Delta I_{b2}}{I_C} + \frac{\Delta V_{BE2}}{I_C R_C} \right) \qquad (10)$$

where

T_C is the temperature of the chip,
I_C is the nominal collector current,
R_C is the value of the collector load resistors,
ΔR_C is the change in collector resistors,
ΔI_{b2} is the change in the difference of the second stage input currents,
ΔV_{BE2} is the change in the offset voltage of the second stage.
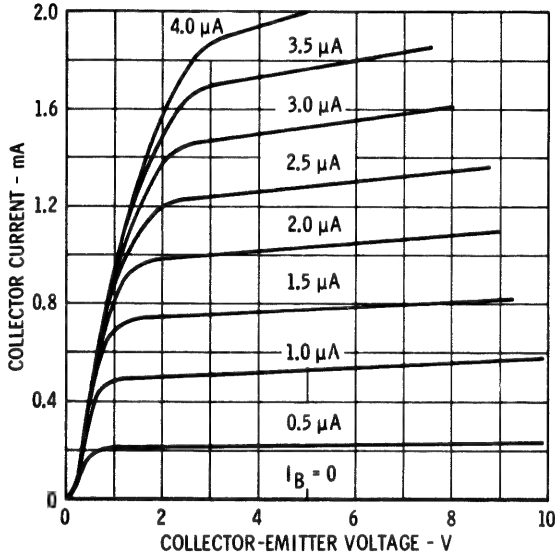
Fig. 7 Collector Characteristics—Active Region.
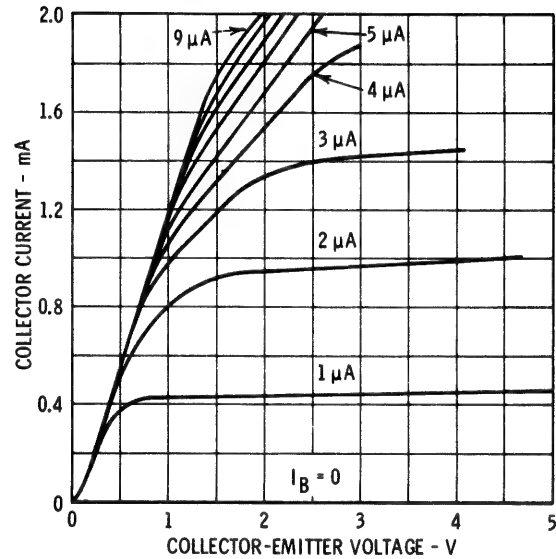
Fig. 9 Collector Characteristics—Saturation Region.
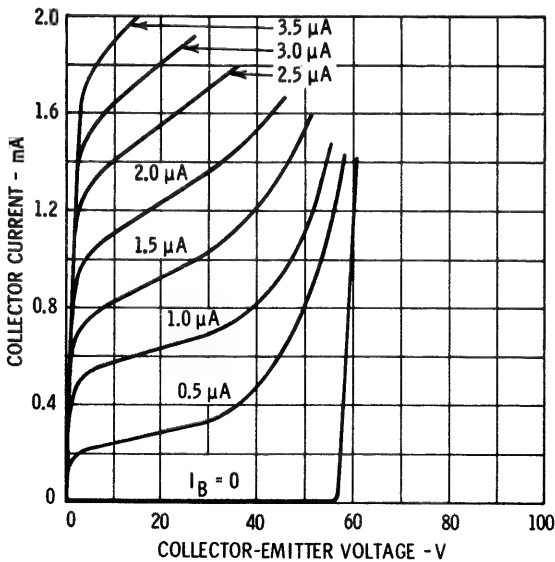
Fig. 8 Collector Characteristics—High Voltage.
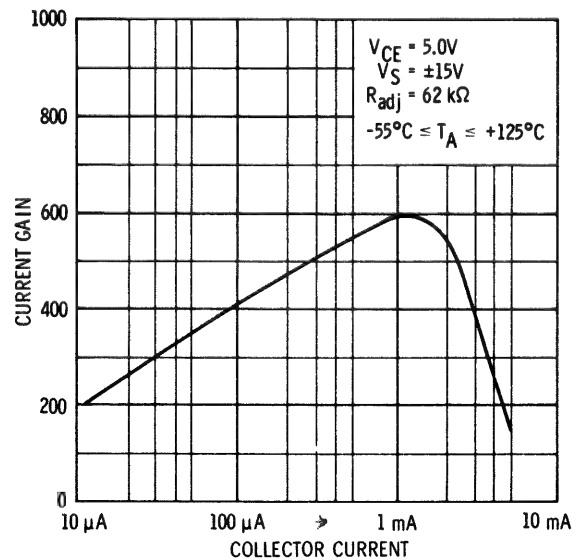
Fig. 10 Current Gain as a Function of Collector Current.

Another factor that can affect the offset drift is the actual physical layout and construction of the circuit in which the device is used. At very low drift levels, the thermo-electric voltage produced by two dissimilar metals in contact becomes significant, such as when the leads of the device are soldered to a copper circuit board. If the lead connections of the two bases and emitters are at the same temperature, these voltages cancel out and contribute little to the total drift. If, on the other hand, a thermal gradient exists between the connections (due to unequal air flow, unequal heat sinking, etc.) the differential voltage produced may be as high as $100\text{-}200\mu V$ over a large temperature range. It is important, therefore, to position the base and emitter connections such that they are at equal temperatures.

Since the temperature control requires that the power dissipated in the chip be inversely proportional to temperature, any significant power dissipated in the differential pair will reduce the maximum ambient temperature where the temperature regulation is effective. With a thermal resistance of $500°C/W$, this means that the total power dissipated by the transistor pair must be derated to zero at $+125°C$ at the rate of $2mW/°C$.

Circuits using the $\mu A726$ with monolithic operational amplifiers to form very low drift, high gain DC amplifiers are given in the Applications chapter.

THE μA716 FIXED-GAIN, LOW-DISTORTION AMPLIFIER

In general, the problems associated with the design and production of circuits intended for AC operation are more easily managed than in the DC amplifier case. Since production variations are a fact of life, and stable, repeatable over-all performance is desired, the use of a feedback system is justified. The feedback concept provides excellent control over the production variations typically encountered, and allows a low-distortion, fixed-gain amplifier to be produced at high yield and low cost.

The μA716 is designed for applications requiring a stable, fixed-gain device with voltage gains of 200, 100, 20, and 10. The design goals included an operating supply voltage range of 18-24V with a power output capability in excess of 100 mW when operated from a nominal 21-V supply. In addition, external capacitive coupling to the load was required to permit operation with either resistive

or transformer-coupled loads. This keeps DC bias currents out of the transformer windings, and thus permits small, low-cost transformers to be used. It was also desirable to provide some means whereby the output impedance of the amplifier could be set to some nominal value, typically 600Ω. Operation over the entire audio spectrum with at least 40 dB of feedback was also desired.

CIRCUIT DESCRIPTION

In order to satisfy the low-distortion requirement of the amplifier, an emitter-coupled pair is utilized for the input stage. This configuration gives a reasonably high voltage gain with very low distortion for the usual range of input voltages. The emitter-coupled pair also provides a convenient high-impedance, inverting input for the feedback network. In Figure 1, the feedback network $(R_{14}\text{-}R_{18})$ is a simple voltage divider connected to the base of Q_4.
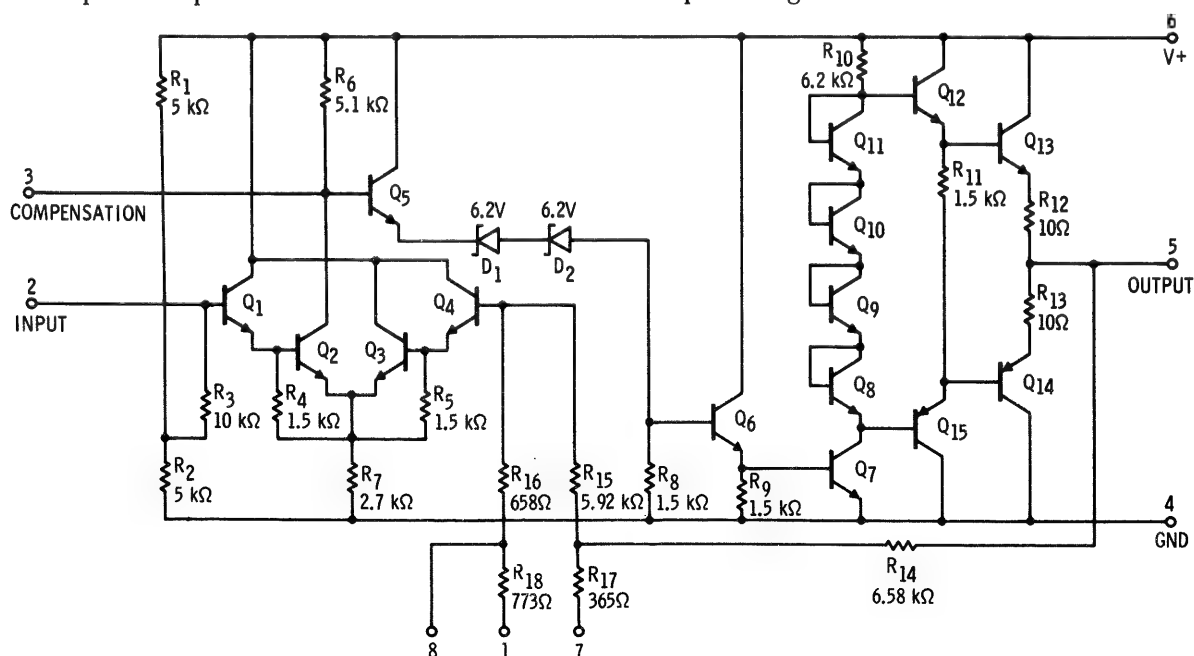
Fig. 1 Schematic Diagram of the μA716.

Since this node impedance is quite high (on the order of $400k\Omega$), negligible loading of the feedback network is realized. Connection of a decoupling capacitor to the appropriate terminal of the amplifier allows any one of the four gain options to be obtained.

Since a true Darlington connection reduces the voltage gain of the input stage by a factor of two, resistors R_4 and R_5 have been introduced between the base and emitter of Q_2 and Q_3. These resistors provide sufficient emitter current in Q_1 and Q_4 to cause the source impedance (as seen by Q_2 and Q_3) to become negligible so that no loss in gain is suffered. Use of resistors rather than current sources is justified, since common mode rejection is not a parameter of particular concern in this amplifier.

Approximate voltage gain of the input stage is given by the ratio of the effective load resistance and the sum of dynamic and contact resistances of devices Q_2 and Q_3. The effect of the source impedance is assumed negligible. Emitter-follower Q_5 decreases the loading due to the second stage on the collector resistance, R_6, so that the gain expression for the input stage is simply

$$A_{v1} = \frac{R_6'}{2 \left(\dfrac{1}{g_{m2}} + R_c \right)} \tag{1}$$

where

$R_6' =$ load resistance of Q_2, including effect of level shifter

$g_{m2} = \dfrac{qI_{C2}}{kT} =$ transconductance of Q_2 or Q_3

$R_c =$ emitter contact resistance of Q_2 or Q_3

This expression is true only for matched devices with equal collector currents in Q_2 and Q_3. Since these conditions are ideal, some departure from symmetry is to be expected with production devices.

DC level translation from the input stage to the output stage is accomplished by the use of zener diodes D_1 and D_2 and emitter-followers Q_5 and Q_6. The emitter-followers reduce the loading of the input stage and provide temperature stabilization of the translated voltage.

The simultaneous achievement of low-distortion, low standby current and large load current capability is provided by a complementary Class AB output stage ($Q_{12} - Q_{15}$). The diode-connected transistors ($Q_8 - Q_{11}$) offer excellent matching to the output devices, so the threshold is typically a few mV (open loop). In addition, their dynamic resistance is considerably below that of an equivalent resistor that would produce the same voltage drop, which means the voltage gain of the stage is determined essentially by R_{10}. The use of complementary devices ensures that the load is driven from a low impedance during both positive and negative signal excursions. The basic distortion mechanism in the output stage is the degradation in current gain of the output devices at large currents. With the large amount of feedback used, however, this is typically less than 0.6% for the highest gain option (200) at $150mW$ output power, and is considerably lower for the other gain options. Resistors R_{12} and R_{13} are provided to absorb any variation in bias voltage that may arise. Standby current in $Q_{13} - Q_{14}$ is typically $1mA$ and is less than $2mA$ for worst-case mismatch in transistor and diode forward voltage. In addition to providing some local bias feedback, the resistors prevent thermal runaway of the output devices under large internal dissipation conditions.

Voltage gain of the output stage and the level shifter is given by an expression similar to that for the input stage. Addition of a suitable constant to account for the non-ideal shift gain of unity is all that is necessary; thus

$$A_{v2} = \frac{KR_{10}'}{\dfrac{1}{g_{m7}} + R_c} \tag{2}$$

where

$K =$ level shifter gain

$R_{10}' =$ effective collector load on Q_7

OPEN-LOOP VOLTAGE GAIN

The general expression for the over-all open-loop voltage gain of the $\mu A716$ is given by the product of Eqs. (1) and (2); thus

$$A_{vo} = \frac{K g_{m2} g_{m7} R_6' R_{10}'}{2(1 + g_{m2}R_c)(1 + g_{m7}R_c)} \tag{3}$$

The value of each of the terms in the gain equation varies with temperature, supply voltage, and to some extent, output loading, since the current gain of the output transistors is a function of output current. The more dominant variations are those connected with the transistor transconductance, current gain, base-emitter voltage, integrated resistors and contact resistance. Unfortunately, most of the parameters of concern are not well defined in terms of temperature stability, so empirical relationships must be determined from measured data. The exceptions, of course, are the base-emitter voltage and the transconductance, which derive from the well-known exponential equation.

Using empirically derived expressions for resistor and current gain variations, a detailed analysis of the amplifier voltage gain was performed on a digital computer, including all effects due to temperature and supply voltage. Emitter contact resistance was taken as a parameter in the plots of voltage gain vs temperature, as were the room temperature current gains of the transistors. The results of six sets of calculations are shown in Figures 2 through 7 for emitter contact resistances of 0, 3.5, and 10Ω and PNP current gains of 30 and 10. Room temperature current gain of the NPN devices was assumed to be 50 for these calculations, and the load resistor was 600Ω. The plots cover the range

Fig. 2 Voltage Gain as a Function of Ambient
Temperature.

Fig. 4 Voltage Gain as a Function of Ambient
Temperature.
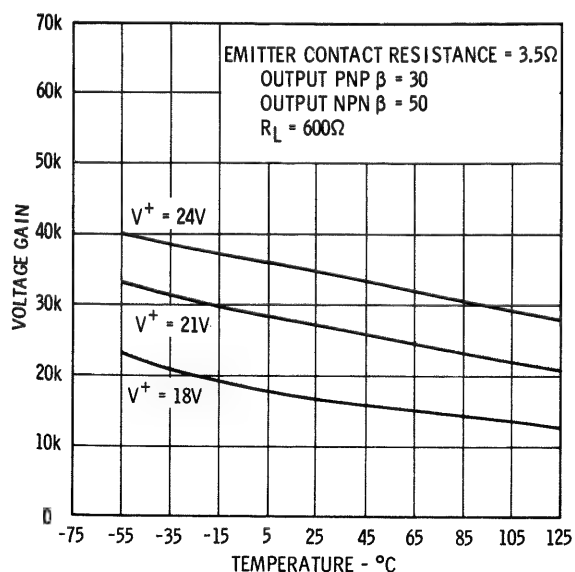
Fig. 3 Voltage Gain as a Function of Ambient
Temperature.
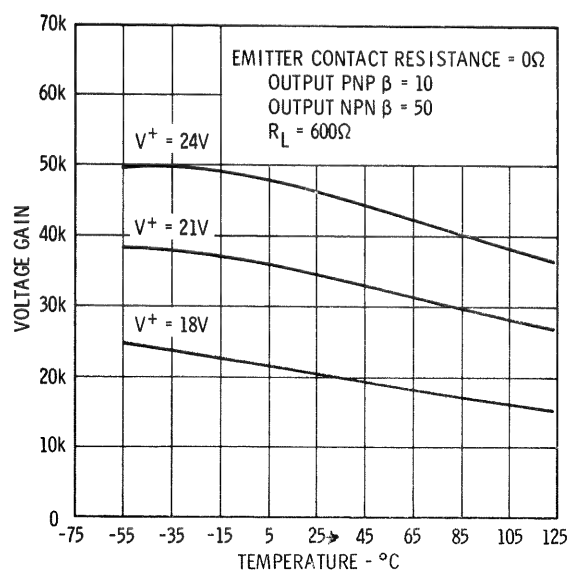
Fig. 5 Voltage Gain as a Function of Ambient
Temperature.
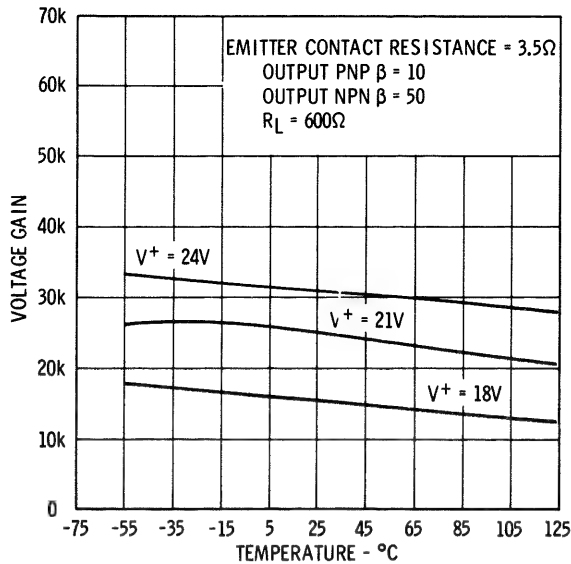
Fig. 6 Voltage Gain as a Function of Ambient Temperature.
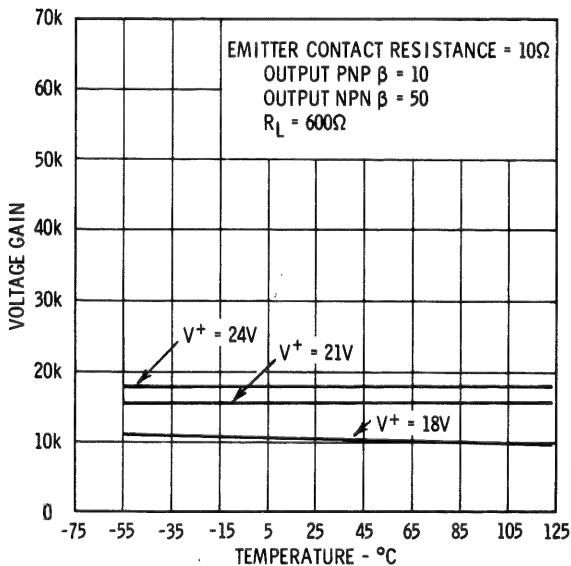
Fig. 7 Voltage Gain as a Function of Ambient Temperature.

from −55°C to 125°C for supply voltages of 18, 21, and 24V. The usual production variation of emitter contact resistance and current gain is such that Figure 3 can be considered typical. The other figures are included to show the relative significance of the uncontrollable parameters on the open-loop voltage gain of the device. From the plot set of Figure 3, the voltage gain variation is seen to be approximately ±1.5 dB with temperature and +1.5, −3dB with supply voltage (referred to 25°C and +21V, respectively).

PERFORMANCE

The large open-loop voltage gain of the μA716 makes the closed-loop gain a function of the feedback network alone. This network is designed to give nominal voltage gains of 10, 20, 100, and 200, depending upon which of three taps are decoupled to ground. The sum of R_{14} and R_{15} is made equal to the sum of R_3 and the parallel combination of R_1 and R_2 in order to minimize the offset voltage produced by the base currents of Q_1 and Q_4. Since the DC transfer of the network is unity, the quiescent output voltage will sit at approximately half the supply voltage.

It is impossible to obtain gains exactly equal to the four desired values because the number of connections is limited to three (so that the circuit can be assembled in an 8-pin package). Computed gains using the values for $R_{14} - R_{18}$ given in Figure 1 are actually 9.73, 20, 102.1, and 200. These values, however, are within the normal production variations encountered with resistor ratios. The critical resistors have been made extra-wide in the integrated circuit (Figure 8) to minimize the production spread in ratio to less than ±1 dB.
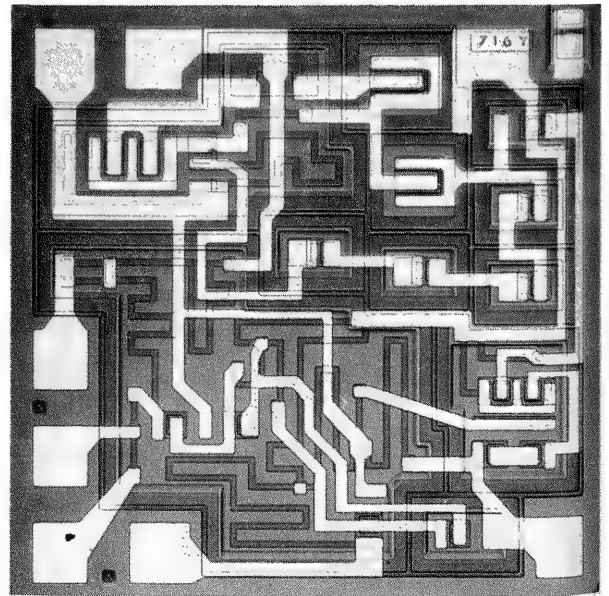
Fig. 8 Photomicrograph of the μA716.

Calculated closed-loop gain stability using the data of Figure 3 is about ±0.25 dB for temperature or supply voltage variations. Measured voltage gain stability agrees quite well with the predicted value, as shown in Figures 9 and 10. Figure 9 illustrates the voltage gain variation with temperature while Figure 10 is a function of supply voltage. Variations in closed-loop response for the lowest gain options are generally an order of magnitude better than for the gains of 200 and 100.
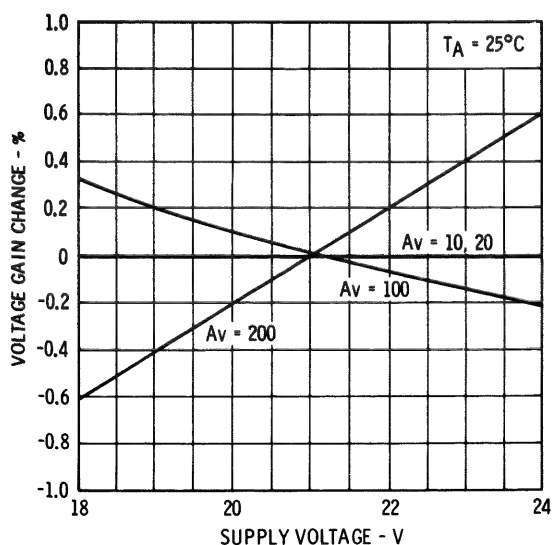
The open-loop frequency response of the μA716 is characterized by a three pole roll-off implying instability for large return differences. Indeed, for the general purpose amplifier, a minimum closed-loop gain of 56 dB is all that may be obtained without compensation. In order to stabilize the amplifier for the available gain options, therefore, some external frequency compensation is required. This is provided by a small capacitor connected from the compensation terminal (collector of Q_2) to the output. An additional R-C network is necessary for the low gain options (see Figure 11). The effect of the compensation networks of Figure 11 on the amplifier response is indicated by Figures 12 through 16. Figure 12 shows the open-loop voltage gain versus frequency characteristic, and Figures 13 through 16 illustrate the excellent closed-loop pulse response of the device. Note, from Figure 12, how the addition of a small capacitor ($3pF$) has caused the roll-off of the amplifier to approach the ideal 6 dB per octave slope. This effect has been referred to as "pole-splitting" by some authors, but is better described by the well-known Miller multiplication effect.
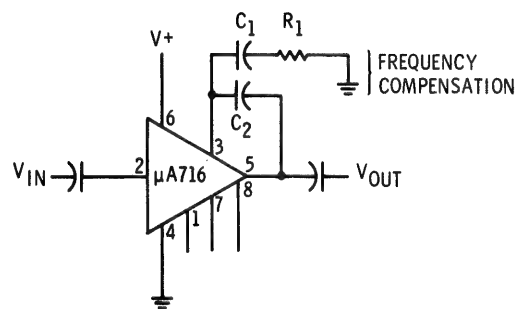
Fig. 9 Relative Voltage Gain as a Function of Ambient Temperature.

Fig. 10 Relative Voltage Gain as a Function of Supply Voltage.

Fig. 11 Connection Diagram and Component Table for Available Gain Options.

Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8
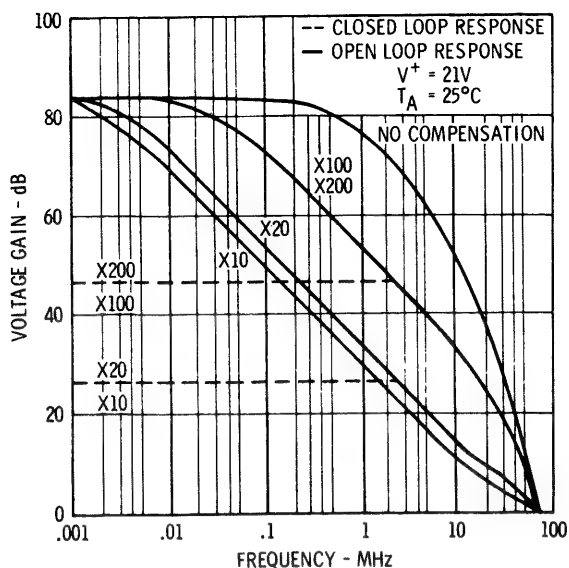
Fig. 12 Open-Loop Frequency Response of Amplifier for Suggested Closed-Loop Compensation.

An additional parameter of importance, directly related to the bandwidth of the amplifier, is the available output power as a function of frequency. Ideally, the maximum available output power of the amplifier should be obtainable over the entire bandwidth of the device. In practice, however, because of capacitance and finite current capability at any given node, full power is usually available over only a small fraction of the maximum bandwidth. With operational amplifiers, for example, this limitation is described by a slew rate figure, but in the case of an audio amplifier, slew rate is not a useful parameter; it is more useful to know the frequency dependence of the output power at a given level of distortion. In Figure 17, curves of constant harmonic distortion are provided for a 1% and 5% THD as a function of frequency, parametric in amplifier voltage gain. This shows that maximum output power may be obtained up to approximately 100 kHz.
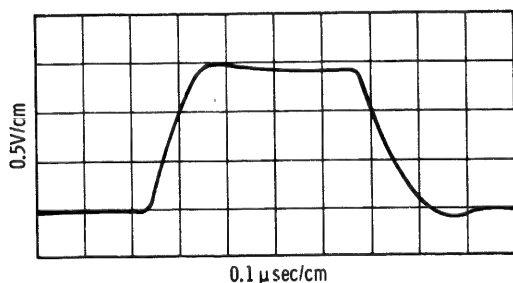
Fig. 13 Closed-Loop Response, $A_v = 10$.
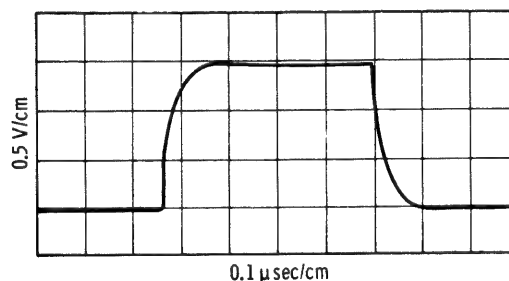
Fig. 15 Closed-Loop Response, $A_r = 20$.
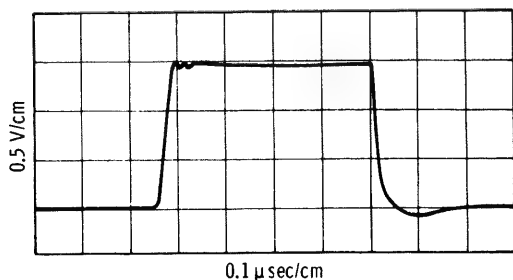
Fig. 14 Closed-Loop Response, $A_r = 100$.
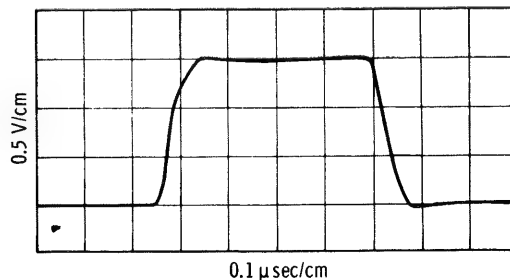
Fig. 16 Closed-Loop Response, $A_r = 200$.
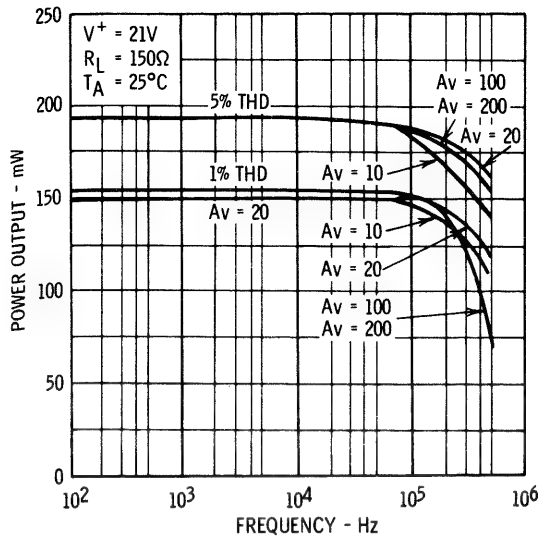
Fig. 17 Power Output as a Function of Frequency (5% and 1% THD).

As mentioned previously, the distortion of the amplifier is present because of the variation in current gain of the output devices with loading. Since very large loop gains are typical with the device, the non-linearities in the transfer function of the closed-loop amplifier are minimal. A quantitative illustration of the effect of loading on the amplifier is given in Figure 18, which shows total harmonic distortion as a function of output power, parametric in voltage gain. For harmonic distortion less than 0.05%, the measurements are essentially equipment-limited. The output resistance of the amplifier is a function of the closed-loop gain, but is less than 1Ω for all operating conditions.
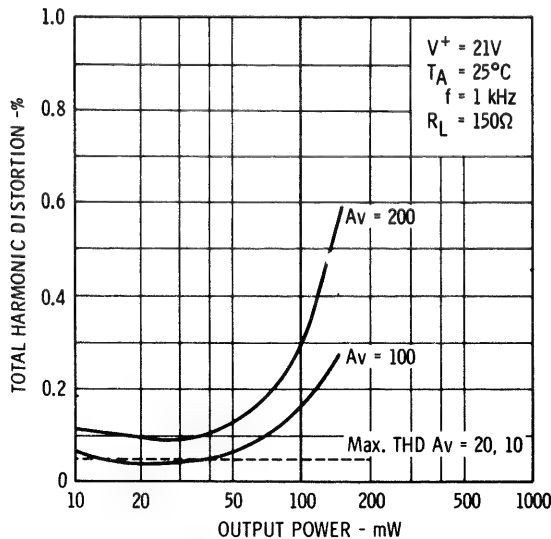
Fig. 18 Total Harmonic Distortion as a Function of Output Power.

Since the output stage is operated Class AB, the power dissipation in the amplifier does not rise directly with output power. Figure 19 shows that the device dissipation increases only 60 mW as the output power goes from 10 to 150 mW. The upper curve in Figure 19 represents the total power drawn from the power supply, and the difference between the two curves is the power delivered to the load.
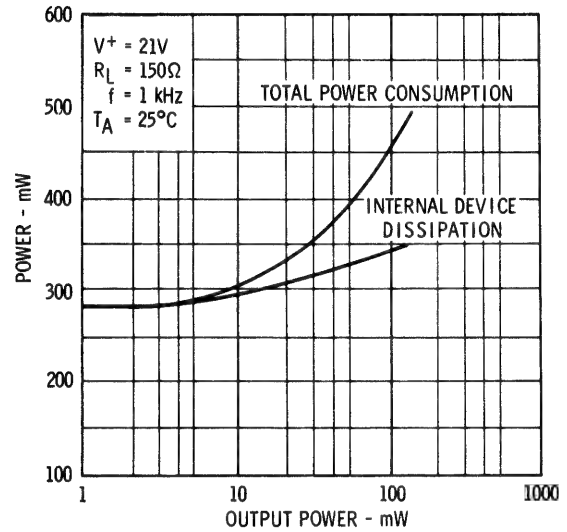
Fig. 19 Total Power Consumption and Internal Device Dissipation as a Function of Output Power.

OUTPUT IMPEDANCE MATCHING

It is sometimes required for a general-purpose amplifier to provide impedance matching to its load. A common example is the channel amplifier in a telephone transmission system, which must have a closely controlled output impedance of 600Ω. A transformer is almost universally used at the output, both for impedance matching and for conductive isolation between the amplifier and the transmission line. This aids in preventing destruction of the amplifier by large transients that may be induced in the line by lightning or man-made interference.

The output impedance of a high gain linear amplifier with negative feedback is well known and is given by the expression

$$Z_o = Z_{po}/(1 - a_o f_o) \qquad (4)$$

or

$$Z_o = Z_{po} (1 - a_o f_o) \qquad (5)$$

for current or voltage feedback, respectively; where

Z_o = output impedance of amplifier with feedback

Z_{po} = output impedance of amplifier without feedback

a_o = open-loop gain of amplifier

f_o = return ratio of feedback network

Fig. 20 Equivalent Circuit Including Output Impedance.

For systems requiring an amplifier with a relatively low or high output impedance, feedback methods are available which are easily realized in practice. Since, typically, the absolute value of the output impedance is of secondary importance (i.e., one usually requires something less than 50Ω or greater than a few $k\Omega$), other system requirements will dictate the particular amplifier/feedback configuration used.

One way of obtaining a precise output impedance is to reduce its value with voltage feedback and then add a resistor in series with the output to get the final desired value. Alternatively, the output impedance can be made very large with current feedback and the final value achieved by shunting it with a resistor. Both methods, however, have the very serious disadvantage of wasting half the output power. Within the constraints set by the available power supply voltage and power dissipation limits, it may not be possible to obtain the desired power output. However, by combining both voltage and current feedback, impedance matching can be achieved with no power loss at all.

It is obvious from Figure 20 that when the output impedance equals the load impedance, the voltage across the load is one-half the amplifier unloaded output voltage. Therefore, if a feedback arrangement is devised that causes the amplifier gain to be reduced by a factor of two when the load is applied, the desired impedance matching will have been obtained.

Figure 21 shows how this is accomplished. The basic voltage feedback amplifier is altered by the addition of a small resistor (R_c) which produces a feedback voltage proportional to the load current.
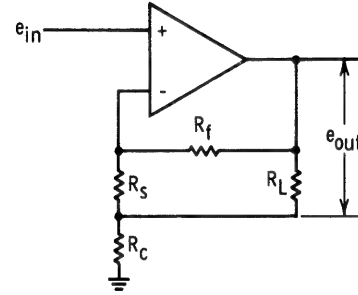
Fig. 21 Circuit for Matching Output Impedance to Load Impedance.

The fact that the load is floating is not objectionable in practice, since an output transformer will ordinarily be used. Assuming that $R_c << R_s$, the amplifier unloaded voltage gain, from basic operational amplifier theory, is given by

$$A_{vo} = \frac{1}{\left(\dfrac{R_s}{R_s + R_f}\right)} \qquad (6)$$

When the load (R_L) is connected, the gain becomes

$$A_{VL} = \frac{1}{\left(\dfrac{R_s}{R_s + R_f}\right) + \left(\dfrac{R_c}{R_c + R_L}\right)}$$

$$= \frac{1}{\dfrac{1}{A_{vo}} + \left(\dfrac{R_c}{R_c + R_L}\right)} \qquad (7)$$

If R_c is chosen such that

$$\frac{R_c + R_L}{R_c} = A_{vo}, \qquad (8)$$

the unloaded gain will be reduced by half and the desired impedance matching will be accomplished.

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An expression for output impedance can be obtained by considering the basic relationships between loaded and unloaded gain:

$$A_{VL} = \frac{1}{2} A_{vo} \text{ when } R_L = R_{out} \qquad (9)$$

therefore, from Eq. (7),

$$R_{out} = R_c \, (A_{vo} - 1) \qquad (10)$$

The unloaded gain, A_{vo}, depends upon the ratio of two diffused resistors and thus can be held within a few percent. The current feedback resistor, however, must be added external to the integrated circuit because of the large absolute value tolerances encountered in the production of monolithic resistors. Note that this method of obtaining precision output impedance does not affect the output power capability of the amplifier except for the negligible power lost in R_c.

CHANNEL AMPLIFIER

The transmission of voice frequencies between subscribers to a telephone system is generally accomplished by suppressed-carrier, AM modulation. The components of the modulating waveform are limited to the band of frequencies extending from approximately 100 Hz to 3.2 kHz. Upon demodulation at the receiving end of the system, the voice frequencies are amplified, processed, and sent on the subscriber by a channel amplifier. Electrical specifications for the channel amplifier require low distortion, flat frequency response over the channel bandwidth, 600Ω input and output impedances (to match the transmission line and filters), and an output capability of +13 dBm.

In addition, considerable savings can be achieved if DC is eliminated from the output coupling transformer.

The circuit of Figure 22 shows how the μA716 may be used to satisfy the output impedance, gain, and other requirements of the typical telephone systems channel amplifier. It uses the multiple-feedback scheme described above to obtain the required 600Ω output impedance; 600Ω input impedance is determined by resistor R_1, which can be a potentiometer if gain control is desired. Capacitors C_1 and C_2 provide input and output coupling, and C_3 is for frequency compensation. Decoupling capacitors C_4 and C_5 set the gain to 40 dB but, if desired, a single 100μF capacitor can be used in place of the two 10μF units shown.

The required performance characteristics of a typical channel amplifier are listed in Table I, along with the measured performance of the circuit of Figure 22.
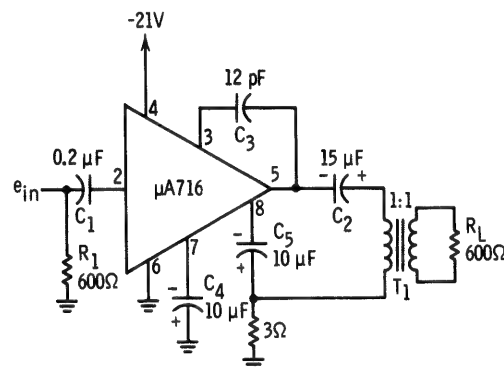
Fig. 22 Channel Amplifier Circuit.

TABLE I.

CHANNEL AMPLIFIER SPECIFICATIONS

(V⁻ = 20V, R_L = 600Ω, 0°C < T_A < 70°C, 100 Hz < f < 10 kHz)

		REQUIRED	MEASURED
Bandwidth		100 Hz − 4 kHz	50 Hz − >100 kHz
Voltage Gain		40 dB	40 dB
Gain Stability		±0.3 dB	±0.05 dB
Total Harmonic Distortion	$P_o = +7$ dBm	0.5%	0.15%
Input Resistance		600Ω ±10%	600Ω ±10%
Output Resistance		600Ω ±10%	600Ω ±10%
Output Noise Power	$R_S = 600$Ω		
	$B_n = 4$ kHz		
	$A_r = 40$ dB	−64 dBm	−75 dBm
Output Voltage Breakpoint		+13 dBm	+17 dBm
Power Supply		−21V ±1V	18-24V
Total Power Consumption	$P_o = 0$	−	280 mW
	$P_o = 20$ mW	<500 mW	300 mW
Output Coupling		AC	AC

The RF/IF amplifiers and mixers in most receiving systems generally employ few components in addition to the tuned circuits. Since tuned circuits cannot be economically integrated with existing technology, use of the remaining components in integrated form is worthwhile only if a substantial improvement in performance or stability can be obtained or if simplified design procedures can be used.

These improvements are provided by the emitter-coupled amplifier shown in Figure 1. Designed for use with transformers and/or tuned circuits, the μA703 eliminates the biasing resistors, bypass capacitors, and coupling capacitors required in conventional amplifiers; operation is essentially unilateral, and the circuit has a symmetrical output current limiting characteristic. This provides increased available power gain, simplified tuning, and superior limiting performance which greatly reduces the detuning, phase shift, and blocking that occur when conventional amplifiers saturate. The device may also be used as a harmonic mixer and is especially attractive when used as an FM limiter.

The biasing arrangement takes advantage of the closely-matched characteristics of integrated circuit transistors, while the DC return path for biasing the input and output is provided by interstage transformer coupling. A single voltage supply is all that is required for operation.

The simplicity of the amplifier is demonstrated by the fact that it is constructed on a 20-mil square silicon die (Figure 2)—a size which is small by comparison to many discrete transistors.
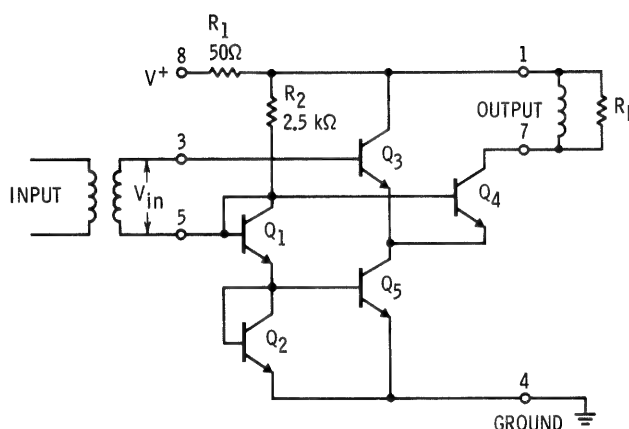
Fig. 1 Schematic Diagram of the μA 703.
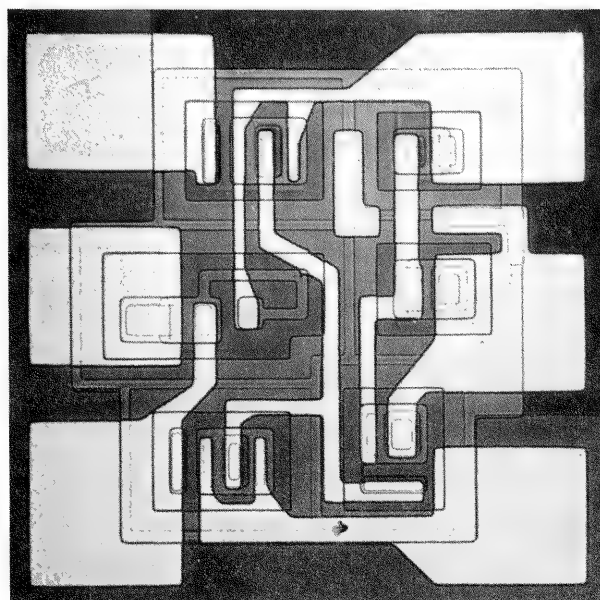
Fig. 2 Photomicrograph of the μA 703.

CIRCUIT DESCRIPTION

The analysis of the μA703 is simplified if the circuit is initially divided into a differential pair (Q_3 and Q_4) and its associated bias circuitry. Relationships may then be derived between the transfer function of the pair and its terminal currents and voltages. The DC biasing of the amplifier has already been described in Chapter 2.

To review briefly, the current through the biasing diode-connected transistor (Q_2) is approximately equal to V^+/R_2 and is relatively independent of transistor characteristics. Diode Q_1 is included to keep the current source transistor (Q_5) out of saturation. The collector current of Q_5 is equal to the diode current because the transistors are identical and their bases and emitters are connected together. When the differential pair is driven hard, the current is alternately switched between Q_3 and Q_4. Excellent limiting performance can be achieved by selecting the load resistance seen at the collector of Q_4 such that

$$R_L \leq \frac{2(V^+ - 2V_{BE})}{I_{C2}} \qquad (1)$$

This ensures that Q_4 cannot be driven into saturation.

For convenience in designing with the μA703 in high-frequency IF and RF circuits, it is best characterized as an active two-port network, with short-circuit admittance parameters used to describe its behavior. Figure 3 shows the equivalent circuit for the amplifier, where the following y-parameters have been used:

input admittance - y_{11}
reverse transadmittance - y_{12}
forward transadmittance - y_{21}
output admittance - y_{22}.
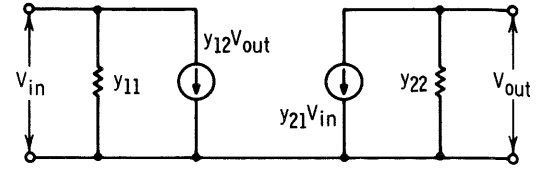
Fig. 3 y — Parameter Equivalent Circuit.

For frequencies low enough that reactive effects can be ignored, the forward transadmittance can be found with the aid of Eq. (22) of Chapter 2, which states that the difference in base-emitter voltage of two identical transistors as a function of their collector currents is

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_2}{I_1}\right) \qquad (2)$$

From Eq. (2), the relationship between the input voltage to the μA703 and the collector currents in the differential pair is given by

$$V_{in} = \frac{kT}{q} \ln\left(\frac{I_{C3}}{I_{C4}}\right) \qquad (3)$$

Since the sum of the collector currents of Q_3 and Q_4 is equal to the current source current (I_{c5}), Eq. (3) may be expressed as

$$V_{in} = \frac{kT}{q} \ln\left(\frac{I_{C5} - I_{C4}}{I_{C4}}\right) \qquad (4)$$

from which

$$I_{C4} = \frac{I_{C5}}{1 + \exp\left(\dfrac{qV_{in}}{kT}\right)} \qquad (5)$$

Eq. (5) defines the transfer characteristic of the amplifier, and is plotted in Figure 4 for a typical device.
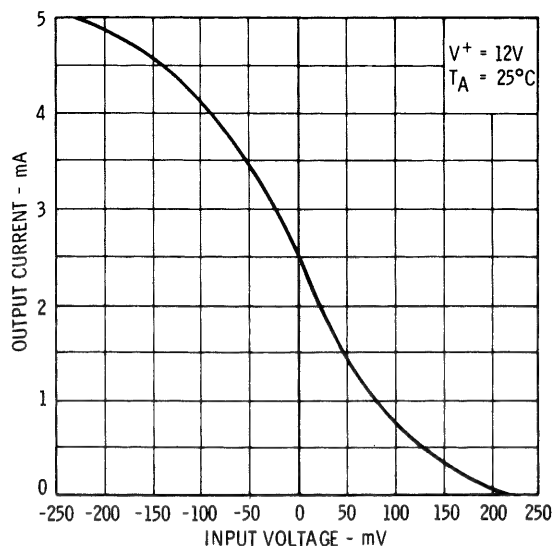
Fig. 4 Transfer Characteristic.

The forward transadmittance of the μA703 may be obtained from Eq. (5) according to the standard two-port parameter definition

$$y_{21} = \frac{\partial \bar{I}_{C4}}{\partial V_{in}}$$

$$= -\frac{qI_{C5}}{kT} \frac{exp\left(\frac{qV_{in}}{kT}\right)}{\left[1 + exp\frac{(qV_{in})}{kT}\right]^2}$$

$$= -\frac{q}{kT} \frac{I_{C5}}{2} \left[\frac{1}{1 + cosh\left(\frac{qV_{in}}{kT}\right)}\right] \qquad (6)$$

Figure 5 shows the forward transadmittance as a function of input voltage calculated from Eq. (6). Note that y_{21} is maximum when the collector currents of Q_3 and Q_4 are equal to each other and equal to one-half the source current. A large resistance between the two input terminals can cause V_{in} to be different than zero because of the DC voltage drop across this resistance produced by the base current of Q_3. This results in a shift of the operating point on the y_{21} curve to somewhere below maximum. Therefore, low DC source impedance or transformer coupling should be used with the μA703.
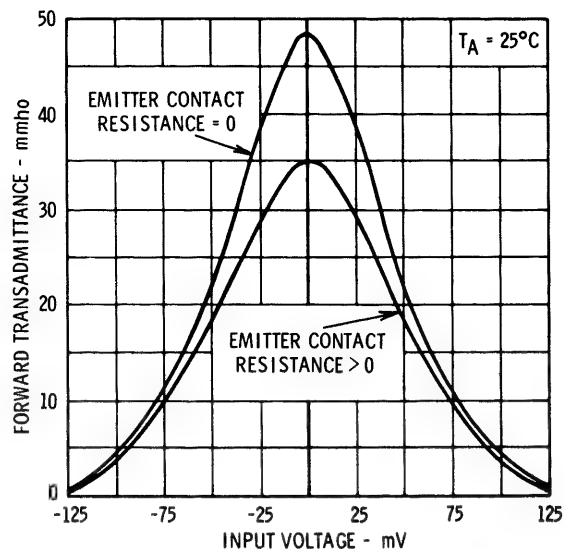
Fig. 5 Forward Transadmittance as a Function of Input Voltage.

The effect of emitter contact resistance in Q_3 and Q_4 has not been included in the analysis. By simple superposition, it can be shown that it merely decreases the maximum transadmittance available. The relative position of the maximum with respect to V_{in} is not altered. In addition, some desensitivity to input voltage will be realized because of emitter degeneration. This is also shown in Figure 5.

The input impedance is also a function of input voltage, increasing with large signals. This is because one transistor in the differential pair is being driven toward cutoff, which results in a large emitter resistance. Figure 6 shows how both input resistance and capacitance vary with signal level.
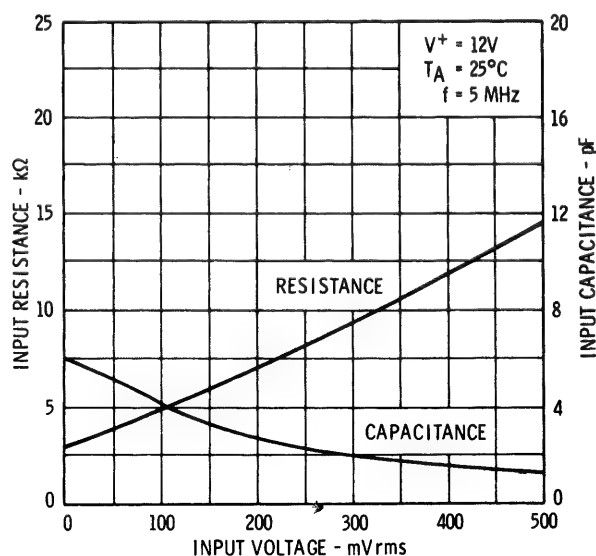
Fig. 6 Input Resistance and Capacitance as a Function of Input Voltage.

TABLE I

TYPICAL ELECTRICAL CHARACTERISTICS OF THE μA703

PARAMETER	CONDITIONS		UNITS
	$(T_A = 25°C, V^+ = 12V$		
	unless otherwise specified)		
Power Consumption	$e_{in} = 0$	110	mW
Quiescent Output Current	$e_{in} = 0$	2.5	mA
Peak-to-Peak Output Current	$e_{in} = 400$ mV rms, f = 1 kHz	5.0	mApp
Output Saturation Voltage		1.4	V
Forward Transadmittance	$e_{in} = 10$ mV rms, f = 1 kHz	35	mmho
Reverse Transadmittance	$f \leq 5$ MHz	.001	mmho
Input Conductance	$e_{in} < 10$ mV rms, $f \leq 5$ MHz	0.30	mmho
Input Capacitance	$e_{in} < 10$ mV rms, $f \leq 5$ MHz	7.0	pF
Output Capacitance	$f \leq 5$ MHz	2.0	pF
Output Conductance	$f \leq 5$ MHz	0.02	mmho
Noise Figure	$f = 30$ MHz, $R_S = 500\Omega$	6.5	dB
	$f = 100$ MHz, $R_S = 500\Omega$	8.0	dB

Over-all performance of the amplifier is summarized in Table I.

The preceding analysis and figures were based on an operating temperature of 25°C and a frequency low enough that reactive terms could be neglected. If the effect of temperature is included, the output current will vary according to the matching and tracking of the transistors, and the change in resistor values. Figure 7 shows the transfer function for two temperature extremes; the stability of the quiescent operating point is given in Figure 8, and that of the forward transadmittance
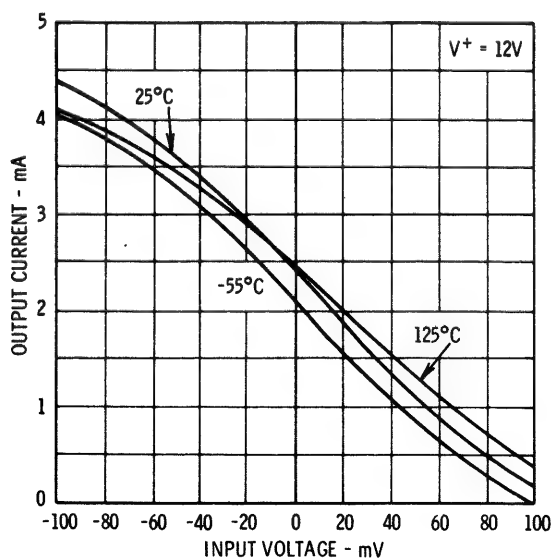
Fig. 7 Transfer Characteristic as a Function of Temperature.
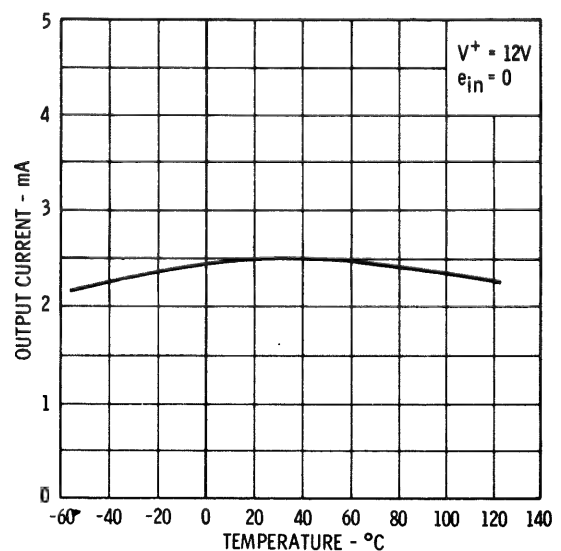
Fig. 8 Output Current as a Function of Ambient Temperature.

by Figure 9. The power consumption changes little with temperature, as illustrated in Figure 10.

Additionally, quiescent operating conditions as a function of supply voltage are given in Figures 11 and 12.
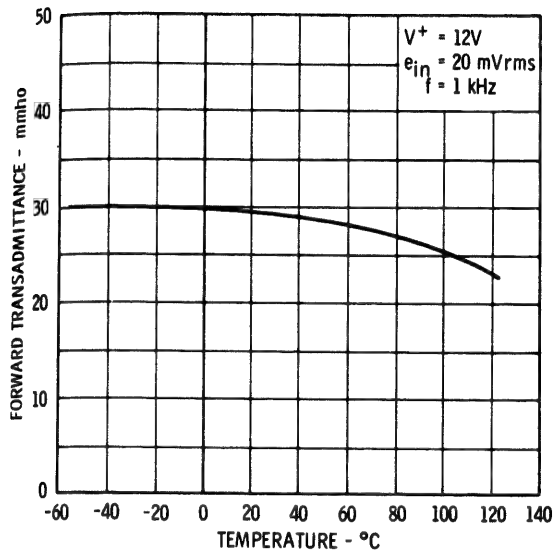
Fig. 9 Forward Transadmittance as a Function of Ambient Temperature.
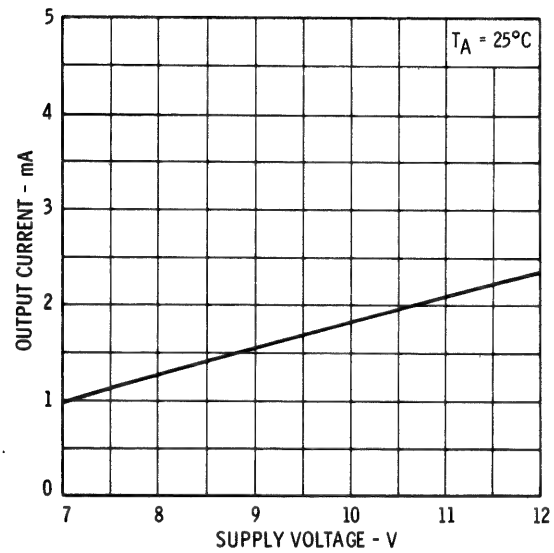
Fig. 11 Output Current as a Function of Supply Voltage.
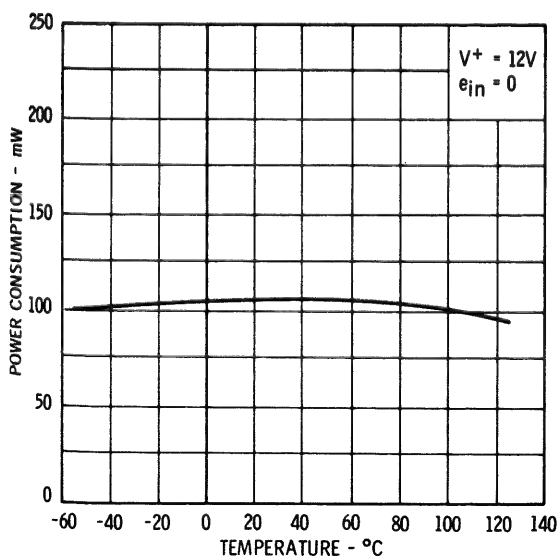
Fig. 10 Power Consumption as a Function of Ambient Temperature.
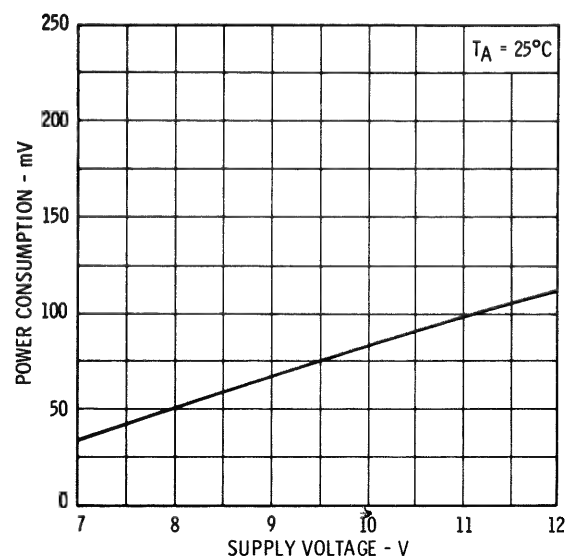
Fig. 12 Power Consumption as a Function of Supply Voltage.

Curves showing the frequency dependence of the two-port parameters of the μA703 are given in Figures 13 through 15. As can be seen, there is little change from the low-frequency values for frequencies less than 5-10 *MHz*. The frequency variation of the input, output, and transfer admittance justify the equivalent circuit of Figure 3 and are typical of most two-ports.
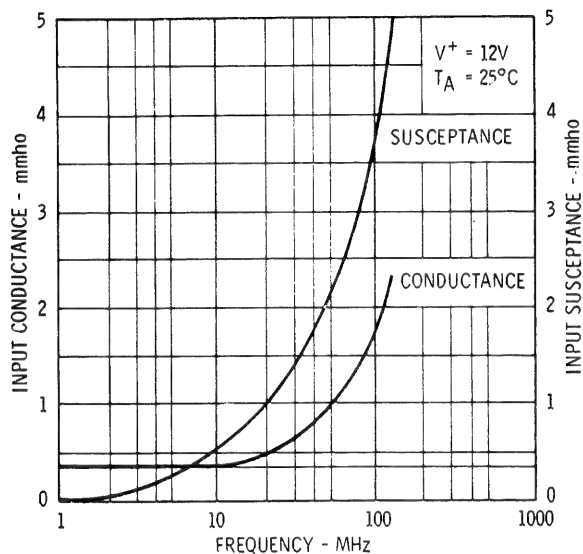
Fig. 13 Input Admittance as a Function of Frequency.
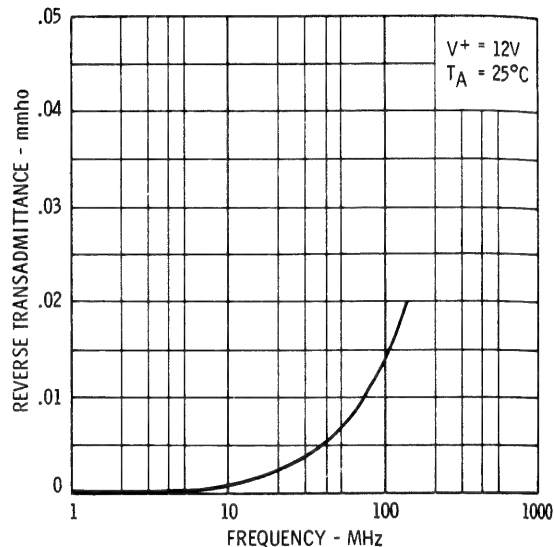
Fig. 15 Maximum Reverse Transadmittance as a Function of Frequency.
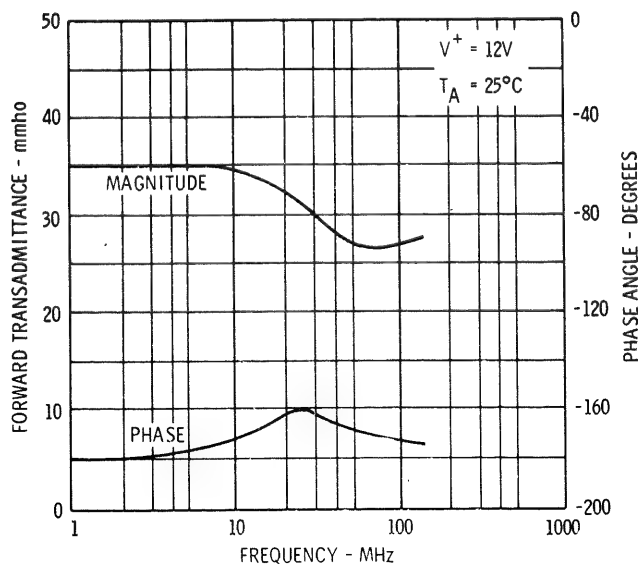
Fig. 14 Forward Transadmittance as a Function of Frequency.
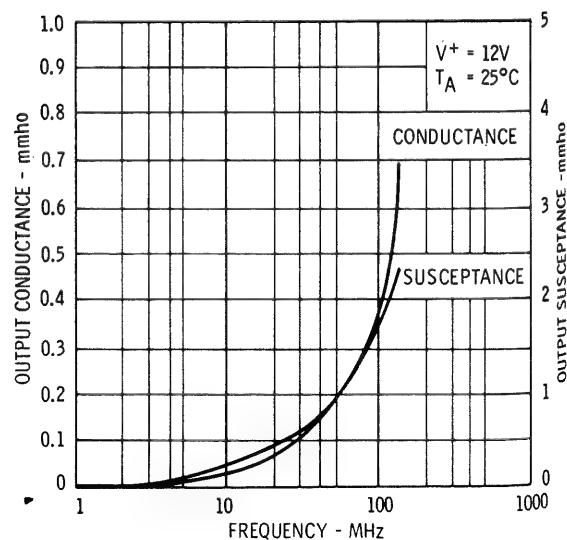
Fig. 16 Output Admittance as a Function of Frequency.

Unneutralized small-signal amplifiers have a feedback path which can cause the real part of the input admittance of the device to become negative for certain combinations of frequency and load impedance. If this situation occurs, and the source admittance is equal to or less than the negative real part of the input admittance, self-sustaining oscillations are possible. For the typical amplifier, the designer has one of two choices: feedback that is equal in magnitude and opposite in phase to that inherent in his device can be applied around the circuit, or the interstage coupling networks can be loaded sufficiently to make the input admittance always greater than zero. These solutions have major drawbacks—neutralization is at best a marginal solution since it is very frequency-sensitive and must be different for each situation. Loading the interstages is less frequency-sensitive, but the resultant mismatch loss is not always tolerable. The most satisfactory solution would be to use a device that possesses negligible intrinsic feedback—if an amplifier of that description does indeed exist. This ideal is closely approached by the μA703, which has internal feedback an order of magnitude less than most high-frequency transistors. For example, a reverse transadmittance of less than 0.001 $mmho$ at 10 MHz is not unusual.

The effect of input and output loading on the stability of the amplifier can best be seen from the expression for power gain of the device. The equivalent circuit of a typical RF amplifier, including source and load admittances, is shown in Figure 17. The expression for the input power (P_i) is

$$P_i = |V_1|^2 \, Re \, (Y_{in})$$

$$= |V_1|^2 \, Re \left(Y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \right) \qquad (7)$$

and the output power is:

$$P_o = |V_2|^2 \, Re \, (Y_L) \qquad (8)$$

From Figure 17,

$$|V_2| = \frac{|y_{21}| \, |V_1|}{|y_{22} + Y_L|} \qquad (9)$$

so

$$P_0 = \frac{|y_{21}|^2 \, Re(Y_L)}{|y_{22} + Y_L|^2} \, |V_1|^2 \qquad (10)$$

and the power gain becomes

$$\frac{P_o}{P_i} = \frac{|y_{21}|^2 \, Re(Y_L)}{|y_{22} + Y_L|^2 \, Re \left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \right)} \qquad (11)$$

It can be seen from Eq. (11) that the amplifier will be stable if

$$Re \left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \right) > 0. \qquad (12)$$

Eq. (12) can be manipulated to yield

$$2g_{11} \, (g_{22} + g_L) - Re \, (y_{12}y_{21}) - |y_{12}y_{21}| > 0. \qquad (13)$$

where the "g" terms represent the real parts of the admittance parameters.

If the power gain is reckoned from the terminals XX', Eq. (13) becomes

$$2(g_{11} + g_s) \, (g_{22} + g_L) - Re \, (y_{12}y_{21}) - |y_{12}y_{21}| > 0. \qquad (14)$$
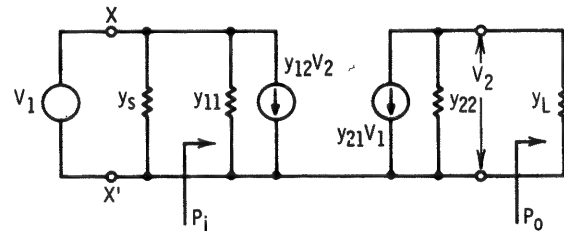
Fig. 17 Tuned Amplifier Equivalent Circuit.

Inspection of the above equation reveals that for unconditional stability at all frequencies, for any combination of source and load conductance, y_{12}, the reverse transadmittance, must equal zero. Since in practice y_{12} is finite, the source and load conductances must be manipulated to satisfy the stability criterion.

If it is assumed in Eq. (13) that the real part of y_{12} is nearly zero, an expression can be obtained that will lead to a useful figure of merit for a two-port.

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If $Re\,(y_{12}y_{21})$ approaches zero, Eq. (13) becomes

$$2g_{11}\,(g_{22}+g_L)-|y_{12}y_{21}| \geq 0. \qquad (15)$$

which for conjugate matching becomes

$$4g_{11}g_{22} \geq |y_{12}y_{21}|. \qquad (16)$$

For conditional stability,

$$4g_{11}g_{22} = |y_{12}y_{21}|. \qquad (17)$$

The maximum gain that can be obtained from the two-port when the device is neutralized and conjugately matched is, from Eq. (11)

$$\frac{P_o}{P_i} = \frac{|y_{21}|^2}{4g_{11}g_{22}} \qquad (18)$$

Using Eq. (17), the maximum stable gain (a figure of merit for high-frequency transistors and amplifiers) is

$$GMS = \left|\frac{y_{21}}{y_{12}}\right| \qquad (19)$$

Obviously, the smaller y_{12} is, the greater will be the available stable gain. For very small values of y_{12}, the gain will be determined essentially by the input and output parameters of the device. For typical high frequency transistors at 10 MHz, the GMS is 20 dB, while a GMS of 40 dB can be obtained with the μA703 at this frequency. Thus, fewer stages are required to achieve a given total gain.

A simplified design procedure for a 30 MHz amplifier that will serve to illustrate the practical aspects of the preceding discussion can now be presented. The first problem that must be considered is: "How much gain can be realized at a given frequency?" To evaluate this problem, consider Eq. 19 and the device parameters listed in Table II (taken from the curves of Figures 13-16). At 30 MHz, the forward transadmittance, y_{21}, is equal to 32 $mmhos$ and the reverse transadmittance, y_{12}, is 0.004 $mmhos$. The maximum stable gain, GMS, is therefore 39 dB.

TABLE II

TYPICAL DEVICE PARAMETERS AT 30 MHz

PARAMETER	VALUE	UNITS
Input Resistance	1.70	kΩ
Input Capacitance	9.00	pF
Output Conductance	0.08	mmho
Output Capacitance	2.50	pF
Forward Transadmittance	32 $\underline{/140°}$	mmho
Reverse Transadmittance	0.004	mmho

To obtain this gain, two conditions must be satisfied by the circuit. First, the source and load admittances have to be conjugately matched to the device; otherwise maximum transfer of power from source to load cannot be obtained. Second, the layout of the components must be such that feedback from output to input and from amplifier to external components is minimized.

The turns ratio of the input and output transformers are selected to provide a conjugate match to the device parameters listed in Table II. The actual circuit details are shown in Figure 18 and the performance is listed in Table III. Excellent agreement is seen to exist between measured and calculated power gain. Interaction between interstage coupling networks is minimal.

TABLE III

30 MHz AMPLIFIER PERFORMANCE

PARAMETER	VALUE	UNITS
Power Gain	35	dB
Bandwidth	1	MHz
Noise Figure	6	dB
Power Gain (calculated)	37.4	dB
Maximum Stable Gain	39	dB
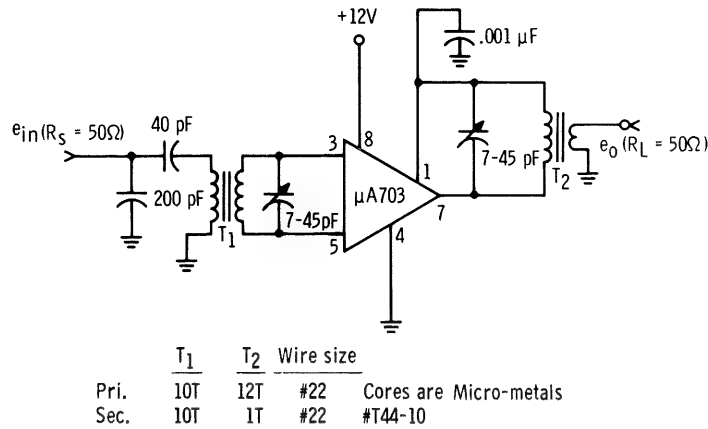
Fig. 18 30 MHz RF Amplifier.

Note that the amplifier does not utilize the limiting characteristic of the emitter-coupled pair and will saturate for large output swings. The input impedance does not drop, however, as the amplifier is driven into saturation.

LIMITING RF AMPLIFIER

The preceding discussion of the small signal amplifier can be extended to limiting amplifiers without exception. The only additional requirement that must be fulfilled is that given by Eq. (1), which ensures that the output transistor will not be saturated.

An amplifier which has a symmetrical output-voltage limiting characteristic can be obtained from the circuit of Figure 18 by a minor modification in the output transformer. The effective turns ratio is adjusted so that the 50Ω load, in parallel with the output resistance of the amplifier, causes the inequality of Eq. (1) to be satisfied.

For a 12-V power supply and a 5 mA maximum collector current, the effective load should be less than 4.5 $k\Omega$. Figure 19 shows the modified amplifier, designed for a 4.5 $k\Omega$ load and an output swing of 22 V_{pp}, with the measured performance characteristics.

Further examples of circuits using the μA703 are given in the Applications chapter.
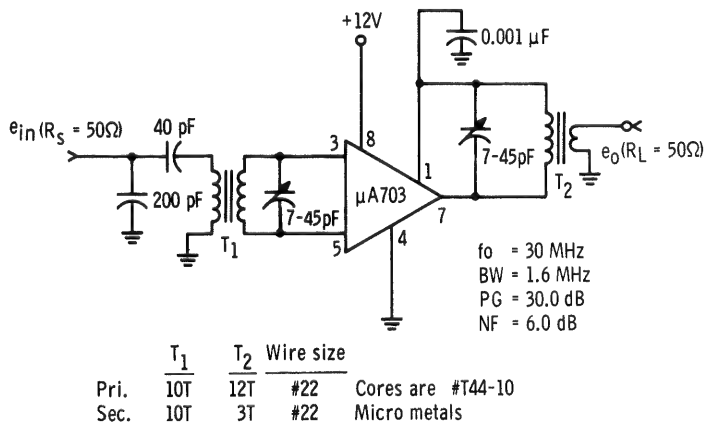
Fig. 19 Limiting RF Amplifier.

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The μA717 and μA718 integrated circuits have been designed primarily for TV sound systems and general FM applications. The first section of both the μA717 and μA718 is a high-gain, high-frequency amplifier which can be used as a 4.5 MHz amplifier, limiter and FM detector in a TV receiver. The detection scheme used departs from the usual detector circuits (ratio, discriminator, and locked oscillator) and employs a simple quadrature switching type. This permits the use of lower cost external circuitry, and at the same time considerably simplifies the alignment problems.

The second section is an additional amplifier, providing sufficient gain and power output to drive an external 0.5W to 2W audio output stage. The μA717 is designed to be operated with a +12V supply and can supply 7 mA rms current at low source impedance to a transistor audio output stage, while the μA718 is designed to be operated with a +18V supply and can supply over 5V rms to a vacuum tube. A photomicrograph of the 47.5-mil square chip is shown in Figure 1.

CIRCUIT DESCRIPTION

When used in an FM receiving system, the μA717 and μA718 can be considered a set of building blocks, as shown in Figure 2. The RF section consists of two amplifiers (which function as current mode limiters for high input level signals) that feed into an "OR" gate and a quadrature circuit tuned to the input signal frequency (4.5 MHz for TV sound systems). The quadrature tank components (R_1, L_1, and C_1) are external to the microcircuit. The recovered audio signal is developed across an external de-emphasis network (R_2, C_2). It is then fed into a volume control and back into the audio section of the microcircuit, amplified, and DC-coupled out again to drive the audio output stage.
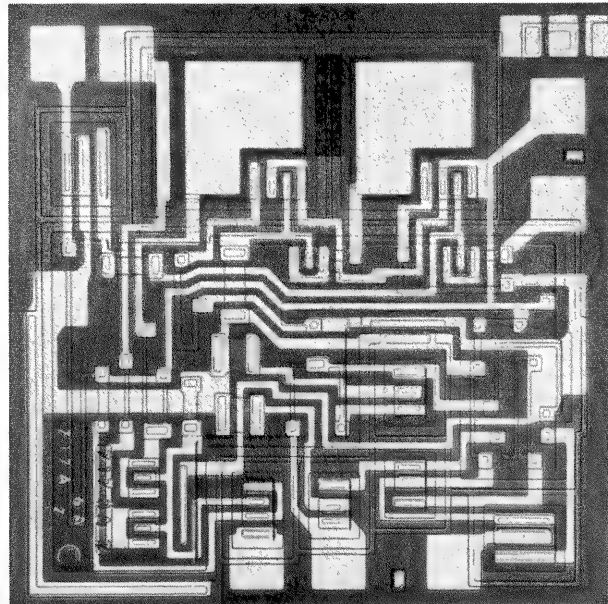
Fig. 1 Photomicrograph of the μA717.
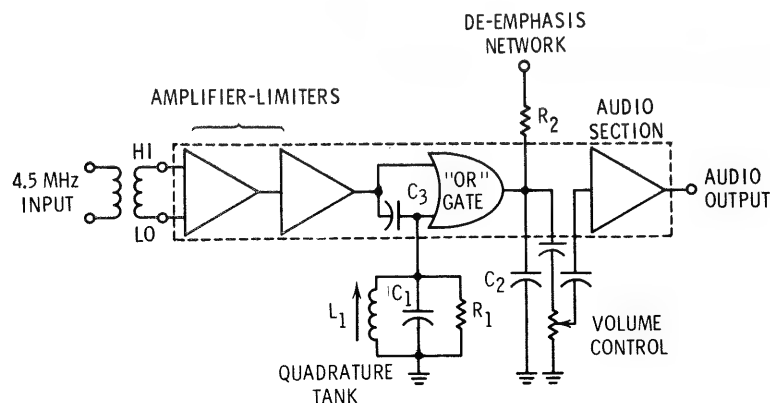
Fig. 2 Basic Building Blocks of the μA717 and μA718.

RF SECTION

Figure 3 shows the schematic for the RF section of the μA717 and μA718. The only difference between the two devices is the value of R_2 in the voltage divider that sets up the collector currents in the active transistors. Since the μA718 operates at a higher supply voltage, the value of R_2 has been decreased to lower the operating collector currents in the differential stages, thereby maintaining the total power dissipation at a reasonable value. Power gain at the operating frequency is not appreciably different for the two microcircuits.

The input signal is coupled into Q_1 through a transformer winding, choke or RC network having a series resistance less than 2 $k\Omega$. The input coupling network must provide a low DC resistance between the "Hi" and "Lo" terminals to keep from upsetting the bias on Q_1. Q_1 and Q_2 form an emitter-coupled pair with gain and limiting characteristics similar to the μA703. The bias network R_2 and R_3 is common to all the RF sections. The

signal developed across R_6 is coupled into an identical amplifier-limiter (Q_4 and Q_5) by C_1, and the output signal is taken from R_{10}.

The final stage is unique in that it can be used either as a straight amplifier or as a quadrature detector ("OR" gate). For amplifier applications, the "Quad" terminal can either be left open-circuit or connected to ground. In both cases, the DC voltage on the base of Q_7 will be zero, and therefore, Q_7 may be ignored since it is cut off. The final section then becomes similar to the first two sections, i.e., an emitter-coupled amplifier-limiter (Q_6 and Q_8), but with the input signal coupled in via C_2 and a resistor R_{12}. The output RF signal may be taken from the RF output terminal and, depending on the application, could feed a ratio detector or discriminator or any other desired circuit. However, it is felt that the use of a ratio detector or discriminator is not justified for either economic or performance considerations because of the advantages gained by the use of the quadrature detector outlined in the following section.
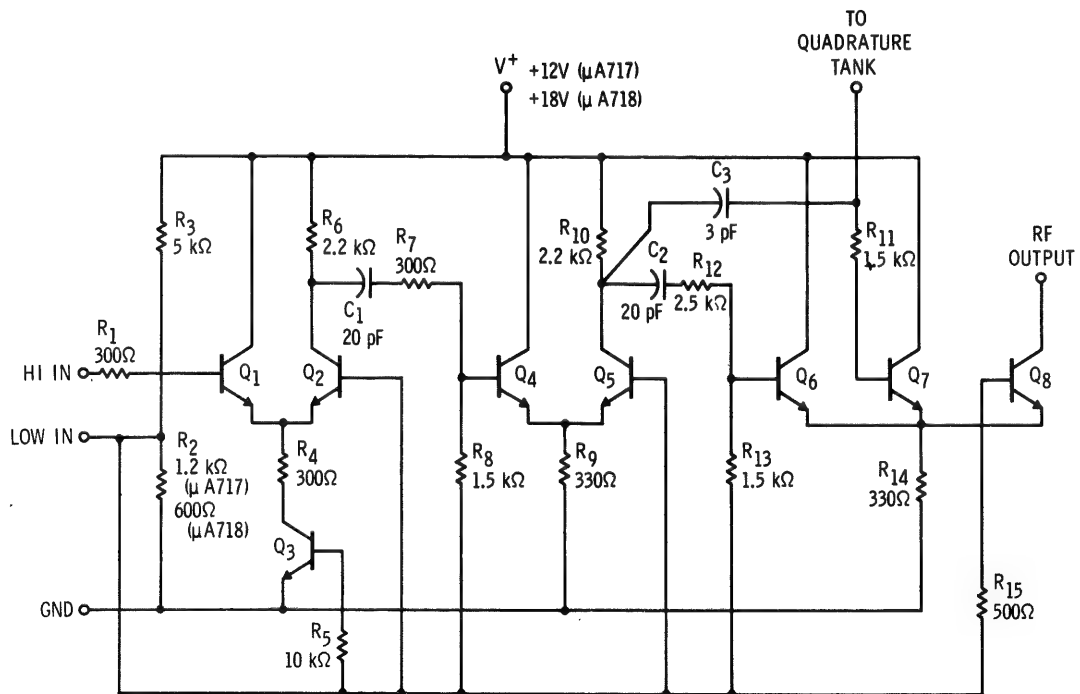
Fig. 3 Schematic of the RF Section.

The voltage gain of the complete RF section with a $1k\Omega$ resistive termination is shown in Figure 4. The RF gain has been designed for a maximum around 4.5 MHz, and the value of coupling capacitors C_1 and C_2 chosen accordingly. As can be seen, the gain falls off at 12 dB per octave at low frequencies and a little more steeply at frequencies above 20 MHz. The useful frequency range is between 100 kHz and 50 MHz.

Current mode limiting — in which Q_4 and Q_5, together with Q_6 and Q_8, do not saturate — is possible above about 2 MHz for the μA717 and at all frequencies for the μA718. Current mode limiting gives symmetrical limiting without imparting violent phase distortion to the FM signal. This improves the AM rejection and capture ratio, and reduces distortion in the demodulated audio signal.

Very high values of power gain (on the order of 70 dB) can be realized at 4.5 MHz with input and output matching. The reverse transfer admittance (feedback capacitance, etc.) is extremely small and both microcircuits can be used to obtain gains approaching M.A.G. (70 dB at 4.5 MHz) with no special precautions if the "Lo" input terminal is bypassed by a ceramic capacitor of 0.01 μF or more. Conventional transformers may be used in consumer-type cans.
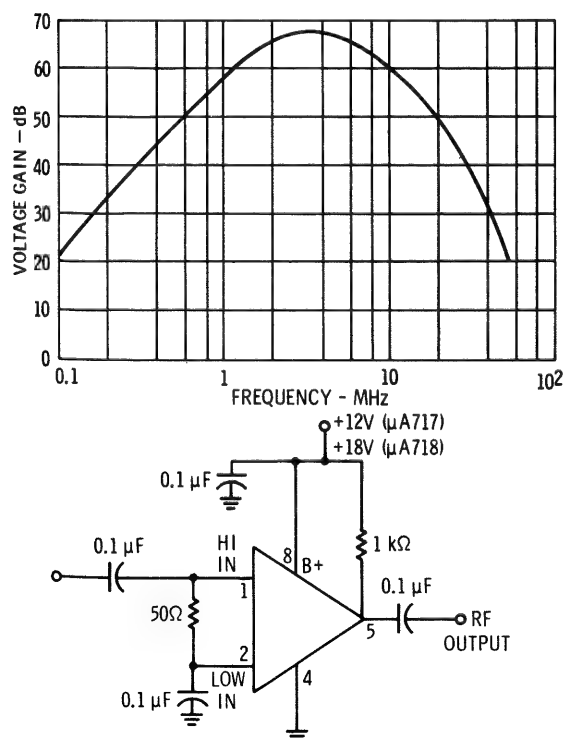
Fig. 4 Voltage Gain of the RF Section.

THE QUADRATURE DETECTOR

For many years, quadrature detectors have been used with vacuum tubes for TV sound detectors. This has been possible due to the fact that multi-grid tubes offer more control electrodes with good isolation between each electrode. The major advantage of the quadrature detector has been in cost/performance considerations, and especially in the simplicity of the quadrature coil design. Discriminators, ratio detectors, etc., require fairly complicated two-pole transformers and necessitate somewhat difficult tuning procedures when compared to a simple quadrature detector.

One of the well-known advantages of monolithic linear microcircuits is the very low cost of individual matched transistors and resistors. This has led to a complete reexamination of the FM detector circuitry based on a different cost criteria than would be used with a discrete component system. One solution to the FM detector can be found in the "OR" gate, which is very popular in current-mode logic circuitry (Figure 5). The logic functions are shown in Table I. Consider the case when one of the input signals (INPUT 2) is displaced with respect to the other input signal in phase by 90°. The conduction period for a "Lo" output will be one-quarter of the total duty cycle.
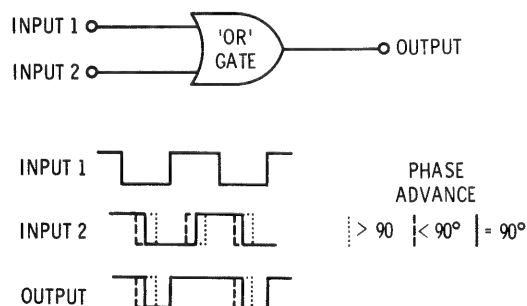
Fig. 5 "OR" Gate.

TABLE I

OUTPUT VOLTAGE FOR VARIOUS COMBINATIONS OF INPUT VOLTAGES

INPUT 1	INPUT 2	OUTPUT
HI	LO	HI
LO	HI	HI
HI	HI	HI
LO	LO	LO

If the phase of INPUT 2 signal is varied around 90°, the "Lo" output period will vary in the same manner. The output signal can be integrated to remove the AC component, resulting in a DC output proportional to the phase difference between the two input signals. This is shown in Figure 6, where the phase difference between the two input signals is plotted against the DC component of the output signal. In theory, perfect linearity can be achieved; and, as will be shown, extremely good linearity can be achieved in practice as well.
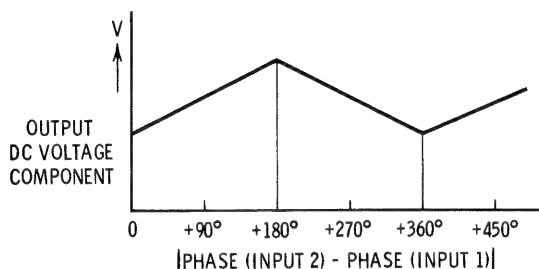
Fig. 6 "OR" Gate Input-Output Characteristics.

The practical "OR" gate configuration chosen for the μA717 and μA718 is an emitter-coupled trio with the two input signals applied to the bases of transistors Q_6 and Q_7, and the resultant output signal taken from the collector of Q_8. In this way, it is most convenient to convert the "OR" gate into a straight emitter-coupled amplifier as previously described, without having to add external components.

The complete quadrature detector is shown in Figure 7. The 90° phase shift for one input is achieved primarily by C_3 and the R_p of the quadrature coil. The other input signal is fed into the base of Q_6 via C_2 and R_{12}. Resistor R_{12} isolates the common input drive point from Q_6. To obtain the

audio component, the output signal is integrated by a $4.7 k\Omega$ resistor and a $0.01\mu F$ capacitor. (De-emphasis is achieved at the same time with suitable component values).

The phase-frequency relationship of a tuned circuit near resonance is not linear. However, a suitable compromise between the "Q" factor of the tuned circuit, the recovered audio output signal, and the audio distortion gives more than acceptable results. "Q" factors in the ranges of 30 to 60 are required for TV sound systems ($\pm 25 kHz$ deviation). For critical FM applications at $10.7 MHz$, lower "Q" factors should be used to obtain linearities of better than 0.8% for $\pm 75 kHz$ deviations.

Another way to obtain very good linearity is to use a double-pole quadrature coil. The input and output phase-frequency linearity of a double-pole filter is optimized by choosing $kQ_{pri} = 0.7$, where k is the coupling factor. The major advantage of two-pole filters is that they provide much higher detector sensitivities for a given linearity than a simple quadrature coil. This is shown in Figure 8. This improvement of the simple quadrature detector results in linearities as good as the best ratio detectors and discriminators, and should prove to be popular in high-quality FM tuners.
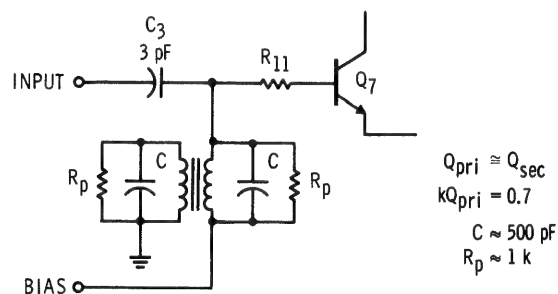
Fig. 8 Double-Pole Quadrature Detector.
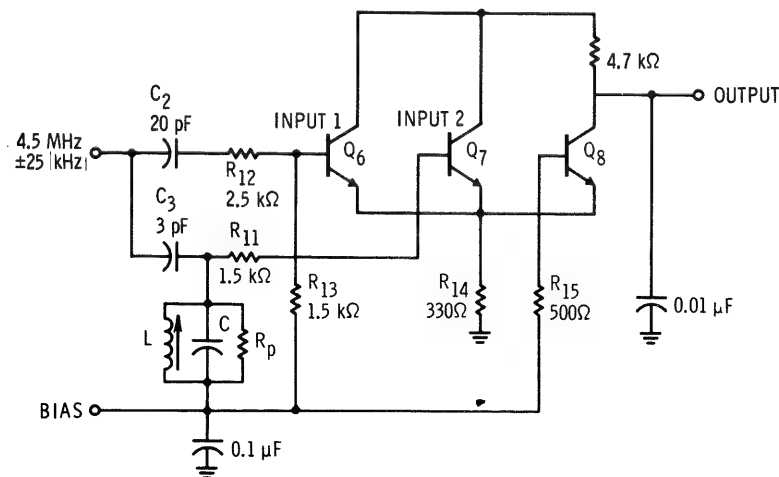
Fig. 7 The Quadrature Detector.

The input admittance at the base of a transistor in an emitter-coupled configuration varies both in conductance and susceptance values, depending on the applied input signal level. As shown in Figure 9, the input conductance and susceptance decrease with increasing signal. The tuning capacitor (C) and the R_p of the quadrature tank circuit should therefore be chosen such that input variations of transistor Q_7 with the normal range of input signal values do not appreciably change the "Q" or resonant frequency of the tank circuit. A tuning capacitance of about 500 pF appears optimum for both 4.5 MHz and 10.7 MHz operation.
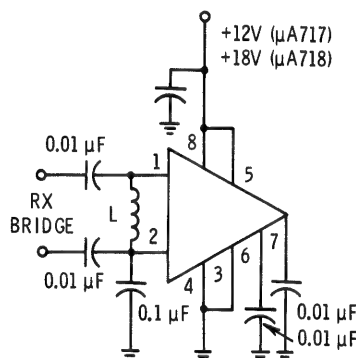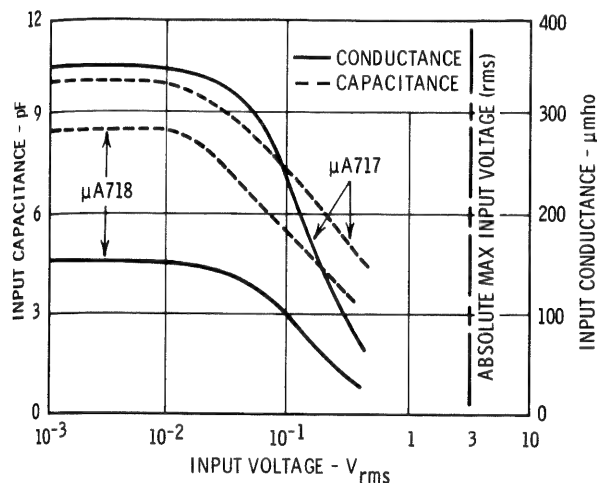
Fig. 9 Input Capacitance and Conductance Variation with Signal Level.

AUDIO SECTIONS

The audio drive requirements for tubes and transistors differ considerably and are responsible for the two devices, μA717 and μA718, designed around different supply voltages. The μA717 has been designed to drive transistor output stages in both color and black-and-white TV receivers and will be described first.

μA717 AUDIO SECTION

There are many supply voltages off which the transistor audio power output stages are operated.

However, they can be classified into two principal ranges — high voltage (150 V) and low voltage (12-36 V). The audio section of the μA717 is designed to drive both ranges. Figure 10 shows the schematic of the audio section of the μA717. The audio amplifier uses the balanced biasing circuit described in Chapter 2 to give a stable output voltage at the collector of Q_{10} of about 4V. The two V_{BE} drops of Q_{11} and Q_{12} give a resultant DC output voltage of 2.7 V at the "Audio" output terminal. Due to close matching of components, this output voltage can be held fairly accurately in production.
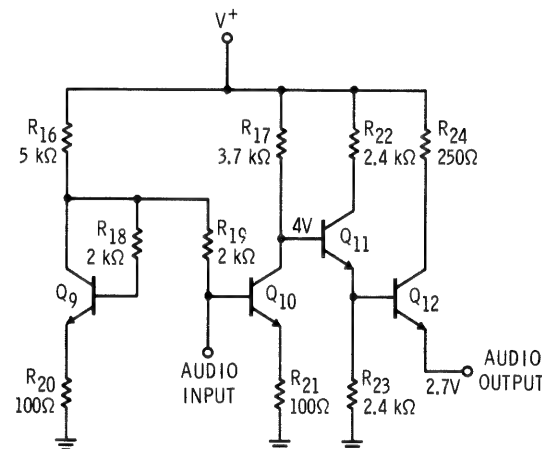
Fig. 10 Audio Section of the μA717.

Q_{12} can drive directly into the external power output transistor. As such, the positive and negative excursions of the output drive should be similar (i.e., ±3 V approximately), otherwise it is possible that the mean DC bias of the power output transistor could change under overdrive conditions and at the limit even destroy the output transistor. To avoid peak positive output voltages greater than 6 V from the microcircuit, Q_{11}, together with R_{22} and R_{23} have been included. The emitter-follower Q_{12} can supply peak currents of 20 mA, being limited by its own saturation voltage and output short-circuit protection of R_{24}.

Figure 11 shows the recommended schemes for driving high and low voltage audio output stages with the μA717. The high voltage scheme permits the most economical operation, and can supply 2W of power to the loudspeaker. The low voltage scheme employs a DC feedback circuit to re-define the output DC voltage from the microcircuit, allowing more of the supply voltage to be used to obtain audio output power with less voltage across the emitter resistor of the audio output transistor.

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a) High Voltage Audio
Output Stage

b) Low Voltage Audio
Output Stage
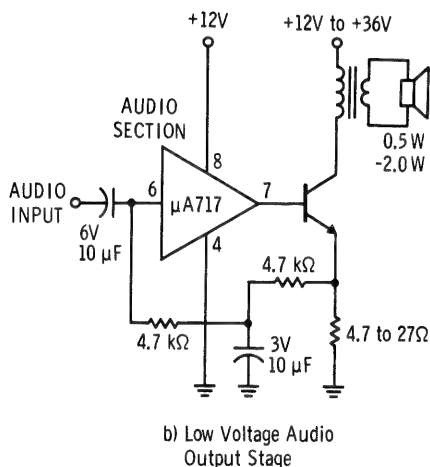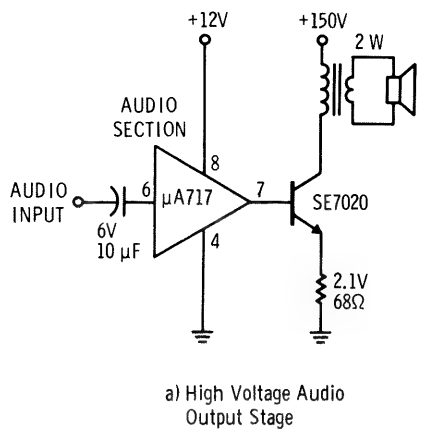
Fig. 11 Typical Audio Configuration for the μA717.

AUDIO SECTION OF THE μA718

The audio section of the μA718 (see Figure 12) is obtained through a simple metal mask option on the basic μA717 circuit, and is designed to drive the tube audio output stage in a hybrid TV receiver. As most tubes require a drive of at least 15 V_{pp}, the circuit employs an 18V supply. Since R_{17} is equal to one-half of R'_{16}, and the rest of the circuit is symmetrical, the DC bias of the "Audio" output is approximately equal to one-half the supply voltage. A little over 16 V_{pp} audio swing can be obtained to drive a tube. A typical tube output circuit is shown in Figure 13.

The audio section of the μA718 may also be used as an additional IF amplifier in an FM tuner. It has very well-defined input and output impedance and gain. Due to the pin configuration, and to avoid instability problems resulting from the very high gain, the audio section used as an IF amplifier should follow the RF section. This application gives the μA718 the highest over-all RF gain of any linear integrated circuit obtainable today.
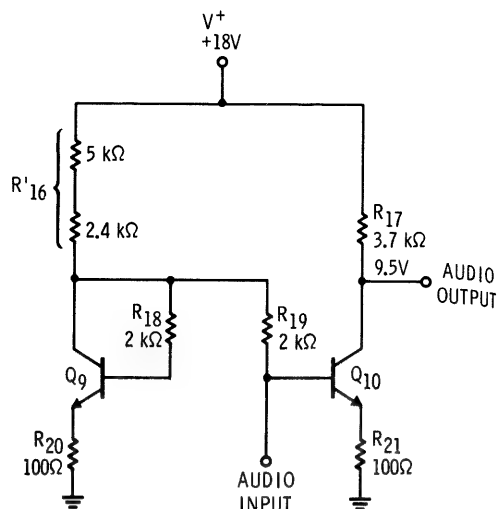
Fig. 12 Audio Section of the μA718.
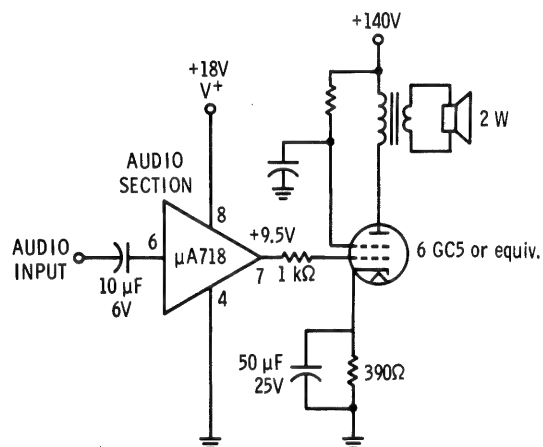
Fig. 13 The μA718 Driving a Tube Output Stage.

CONCLUSION

The μA717 and μA718 offer the consumer equipment designer new possibilities to reduce the cost and complexity of many current designs without any sacrifice in performance. The flexibility of circuit design reflected in the μA717 and μA718 allows them to be used in most applications employing FM signal processing. The supply voltage design centers for either device can be between 9 and 18 V through the addition of an external bias chain consisting of two resistors, one from the V^+ to the "Lo" input terminals and the other from the "Lo" input to the GND terminals.

Typical consumer applications for the devices are given in the Applications chapter.

EFFECTS OF RADIATION ON LINEAR MICROCIRCUITS

CHAPTER 12

INTRODUCTION

Since many linear microcircuits are being used in space and defense applications, it was deemed advisable to determine the radiation resistance of the linear microcircuits produced by Fairchild. To date, the program has been concerned with determining the permanent damage caused by fast neutrons. Units were tested prior to irradiation, then exposed to fast neutrons of energies greater than 0.01 MeV, and retested. The reactor used in the program was a light-water pool-type TRIGA Mark F reactor. Dosimetry was in sulfur-pellet form. No attempt was made to anneal damage.

This chapter details the radiation effects on individual components in the microcircuit and attempts to show how these effects can be correlated to over-all circuit performance. Circuits tested were two operational amplifiers, the μA702A and μA709, and two comparators, the μA710 and μA711.

COMPONENT EVALUATION

A major part of the testing program was to evaluate the effects of radiation on the individual components of an integrated circuit. In the case of linear integrated circuits, these included transistors, diode-connected transistors, zener diodes, and resistors. To evaluate individual components, a special metal mask was put on and individual components bonded out to the pins on a standard TO-99 package. Data was recorded on individual components before and after radiation. The most important components are the NPN transistors, which consist of three basic types: (1) a high-current gain, high breakdown type used in the μA709, (2) a medium breakdown type used in the μA702A, and (3) a medium-current gain, low breakdown gold-doped transistor used in the μA710 and μA711.

*Planar is a patented Fairchild process.

Radiation Effects on Transistors.

Current Gain Degradation The most significant change in transistor parameters is, of course, the current-gain degradation. The transistors used in linear microcircuits generally feature a high-current gain achieved by minimizing the base-width of the transistor, which also results in an increase in f_T. They are made by the standard Planar* epitaxial process, with slightly different diffusion schedules to achieve high breakdown and high current-gain.

Table I shows the current gain — before and after radiation — of the transistors used in the μA709, measured at 10 μA collector current. The current gain at 10 μA is important in the operation of the μA709 because the input stages are operated at collector currents of only 20 μA. Table II shows the current gain of the μA709 transistors at 100 μA. As can be seen by a comparison of Tables I and II, both pre- and post-radiation current gains are higher at 100 μA than at 10 μA. The lower current gain at 10 μA is due to the fact that the emitter efficiency is lower at small currents and is also reduced by irradiation. This can be shown by plotting the change in common-base current-gain versus collector current at various radiation levels. Fig. 1 is such a plot for the μA709 transistors. More discussion of the current-gain degradation is given in the section on the circuit performance of μA709.

Table III shows the current gain before and after radiation of the medium current gain low-breakdown transistor used in the μA702A. Data is given for the most critical application, $I_C = 100$ μA. At this current level, the degradation of the μA702A is somewhat greater than that of the μA709, as can be seen by a comparison of Table II and Table III. This transistor shows the same degradation of emitter efficiency at low current levels as the μA709

TABLE I

CURRENT-GAIN OF μA709 NPN TRANSISTORS MEASURED WITH $V_{CE} = 5V$ AND $I_C = 10\ \mu A$.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1-1	118	105			
1-2	164	140			
2-1	102	100			
2-2	67	65			
3-1	30		25		
3-2	69		50		
5-1	58			20	
5-2	82			20	
6-1	169			25	
6-2	112			23	
7-1	135				3.3
7-2	88				3.5
8-1	44				2.3
8-2	55				2.3

TABLE II

CURRENT-GAIN OF μA709 TRANSISTORS MEASURED WITH $V_{CE} = 5V$ AND $I_C = 100\ \mu A$.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1-1	198	185			
1-2	248	218			
2-1	200	200			
2-2	190	188			
3-1	81		63		
3-2	118		90		
5-1	150			39	
5-2	193			42	
6-1	280			50	
6-2	210			45	
7-1	265				7.2
7-2	215				6.8
8-1	108				5.2
8-2	130				5.2

TABLE III

CURRENT-GAIN OF μA702A TRANSISTORS MEASURED WITH $V_{CE} = 5V$ AND $I_C = 100\ \mu A$.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1-1	72	70			
1-2	109	120*			
2-1	120	118			
2-2	145	133			
3-1	70		57		
3-2	102		75		
4-1	177		112		
4-2	162		105		
5-1	188			27	
5-2	213			27	
6-1	136			21	
6-2	147			22	
7-1	158				3.8
7-2	162				2.8
8-1	77				4.8
8-2	125				3.8

*Increased attributed to test error
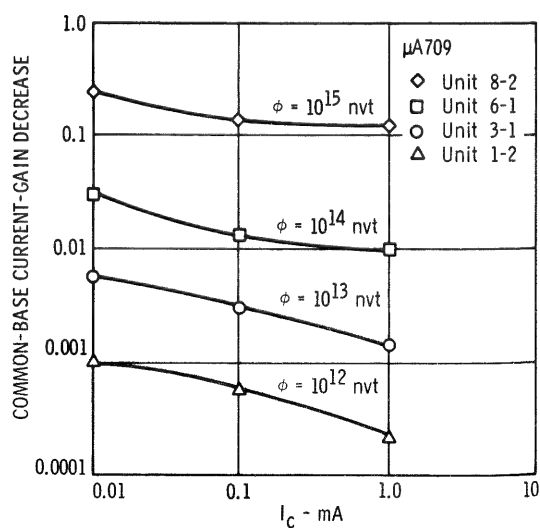
Fig. 1 Common-Base Current-Gain Degradation versus I_C at Various Levels of Radiation for the μA709 Transistors.

transistor. Figure 2 is the plot of alpha degradation versus I_C. Note the similarity to Figure 1. This again shows that the emitter efficiency is degrading with radiation.

As previously mentioned, two of the circuits tested were integrated comparators. These units are gold-doped to increase switching speed, and incorporate medium-current gain low-breakdown transistors. The common-emitter current gain for the transistors is given in Table IV for $V_{CE} = 5V$ and $I_C = 1$ mA. Because of the low gain of these devices at low currents, they are usually not used below 1 mA. For purposes of comparison, the gain of the μA709 devices is given at $I_C = 1$ mA in Table V. Comparing the results for gold-doped transistors with those for the μA709 transistors at 1 mA, there does not appear to be any appreciable benefit from the gold-doping as concerns radiation resistance. The μA709 devices all have higher current gains after radiation. The only drawback of the μA709 device is that it saturates sooner, due to higher collector resistivity. The transistors used in the μA711 will not be discussed here because the processing is identical to that of the μA710.

Leakage Current Effects Since radiation tends to decrease the lifetime on both sides of a p-n junction, the bulk leakage currents tend to increase. However, since surface leakage may predominate at low temperatures, low-temperature leakage currents may increase or decrease.
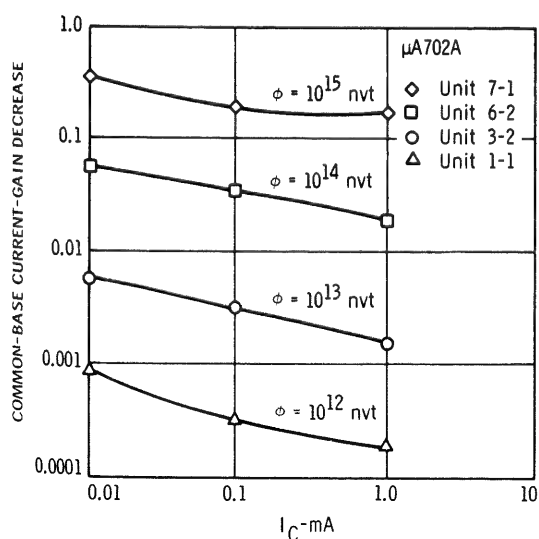
Fig. 2 Common-Base Current-Gain Degradation versus I_C at Various Levels of Radiation for the μA702A Transistors.

CURRENT-GAIN OF μA710 TRANSISTORS MEASURED WITH $V_{CE} = 5V$ AND $I_c = 1$ mA.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
9-2	61	57			
10-1	72	73*			
10-2	62	61			
11-1	100		80		
11-2	87		70		
12-2	53		45		
13-1	71			29	
13-2	85			30	
14-1	60			21	
14-2	55			20	
15-1	74				4.1
15-2	75				4.2
16-1	81				4.3
16-2	86				4.4

*Increase attributed to test error

TABLE V

CURRENT-GAIN OF μA709 TRANSISTORS MEASURED WITH $V_{CE} = 5V$ AND $I_c = 1$ mA.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1-1	300	280			
1-2	340	315			
2-1	312	310			
2-2	342	340			
3-1	155		128		
3-2	172		140		
5-1	286			70	
5-2	313			71	
6-1	404			79	
6-2	343			85	
7-1	400				Sat
7-2	370				7.0
8-1	217				6.1
8-2	240				6.6

Table VI shows the room temperature I_{CBO} of μA709 transistors before and after radiation. Notice that all leakages went down. This is probably due to changes in surface leakage. Table VII shows the I_{CBO} for the same units at 125°C before and after radiation and indicates more clearly the increase in I_{CBO} due to lifetime damage. Since these increases are rather small even at high temperatures, they will not affect the operation of most linear circuits.

TABLE VI

VARIATION OF ROOM TEMPERATURE I_{CBO} (nA) WITH RADIATION FOR μA709 TRANSISTORS MEASURED WITH $V_{CB} = 5V$.

DEVICE NO.	RADIATION LEVEL			
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt
4-1	0.10	0.016		
9-1	0.14	0.008		
11-1	0.10	0.02		
14-1	0.10	0.002		
19-1	0.10	0.002		
2-1	0.10		0.06	
3-1	0.16		0.01	
5-1	0.10		0.05	
15-1	0.10		0.017	
18-1	0.11		0.01	
6-1	0.15			0.075
7-1	0.2			0.05
10-1	0.12			0.04
16-1	1.2			0.9
17-1	0.15			0.07

Voltage Breakdown Because radiation increases the resistivity, the breakdown voltage tends to increase on most transistors. However, some devices which are very close to punch-through may become punch-through devices and actually show a decrease in breakdown voltage, although this did not occur in the units tested. Table VIII gives the breakdown voltages for the μA709 devices after radiation. As can be seen, all are well above 40 V. Breakdown voltages were also measured on the medium-beta low-breakdown gold-doped transistors. These were all well above the minimum 10 V required for satisfactory operation. The LV_{CEO} after radiation is given in Table IX.

TABLE VII

VARIATION OF 125°C I_{CBO} (nA) WITH RADIATION FOR μA709 TRANSISTORS MEASURED WITH $V_{CB} = 5V$.

DEVICE NO.	RADIATION LEVEL			
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt
4-1	3.0	5.5		
9-1	4.2	2.2		
11-1	12.0	3.4		
14-1	3.5	2.1		
19-1	4.0	2.2		
2-1	4.0		18.0	
3-1	4.0		6.0	
5-1	12.0		14.0	
15-1	3.4		8.0	
18-1	3.5		5.5	
6-1	4.4			30.0
7-1	16.0			21.0
10-1	3.0			21.0
16-1	11.0			48.0
17-1	11.0			40.0

TABLE VIII

LV_{CEO} OF μA709 TRANSISTORS (V) AFTER RADIATION MEASURED AT 1 mA.

DEVICE NO.	RADIATION LEVEL			
	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1-1	52			
1-2	50			
2-1	88			
2-2	53			
3-1		68		
3-2		69		
5-1			86	
5-2			88	
6-1			68	
6-2			70	
7-1				95
7-2				86
8-1				52
8-2				52

TABLE IX

LV_{CEO} OF µA710 TRANSISTORS *(V)* AFTER RADIATION MEASURED AT *1 mA*

DEVICE NO.	RADIATION LEVEL			
	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
10-1	15.8			
10-2	15.2			
11-1		16.0		
11-2		15.6		
13-1			16.9	
13-2			16.8	
14-1			17.2	
14-2			17.2	
15-1				25.5
15-2				26.0
16-1				35.5
16-2				25.0

TABLE X

CURRENT GAIN OF LATERAL PNP VERSUS RADIATION MEASURED WITH $V_{CE} = 5V$ AND $I_c = 100$ µA.

DEVICE NO.	RADIATION LEVEL			
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt
1	8-1	6.4		
2	7.0	6.3		
3	5.8		2.0	
4	3.1		1.5	
6	9.1			0.2

TABLE XI

CURRENT GAIN OF VERTICAL PNP VERSUS RADIATION MEASURED WITH $V_{CE} = 5V$ AND $I_c = 1$ mA

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
10	6.5	6.0			
12	25		14.3		
14	25			1.7	
15	26				.08
16	32				.13

PNP Transistors   In the µA709 operational amplifier, there are two types of PNP transistors, a lateral and a vertical type. The lateral PNP has been described in Chapter 2. As made in the µA709, it is of necessity a wide-base device due to masking tolerances and side-diffusion. This wide base gives it a low base-transport factor. In addition, due to the diffusion profiles, the emitter efficiency is low, and results in a very low gain unit. With proper circuit design, however, the lateral PNP can still be a useful, level-shifting device. As there was no discernible gain at 10^{15} *nvt*, data is given only to 10^{14} *nvt*. Table X gives the pre- and post-radiation current gain of the lateral PNP at 100 µA, the only current at which this device is used. As can be seen, the device is quite heavily damaged by radiation. Fortunately, the circuit can tolerate gains less than unity. More discussion of this point will be given later. Breakdown voltage of this device is quite high due to the impurity profiles. All devices had LV_{CEO}'s greater than 80 *V* after radiation.

The vertical PNP, otherwise known as the substrate PNP, has higher current gain than the lateral PNP due to a smaller base width. This device is used as an output emitter-follower transistor. This device also proved to be quite sensitive to radiation. Table XI gives the pre- and post-radiation current gains at $I_c = 1$ *mA*. As can be seen, the typical device with a gain of 25 has a gain slightly less than two at 10^{14} *nvt*. This is also instructive in considering the parasitic current gain of the substrate, which, for a radiated device, would be very low—one of the few good effects of radiation.

Summary of Radiation Effects on Transistors   In the preceding sections, it has been shown that the predominant effect of radiation is to reduce the current-gain of the microcircuit transistors. This effect is more pronounced in the case of the two types of PNP transistors tested than in the case of the NPN transistors. Other transistor parameters degenerated very little and are not considered to affect circuit operation.

Diode-Connected Transistors   In the design of linear integrated circuits, another commonly used component is the diode-connected transistor (DCT). The DCT is generally used as a biasing device and sometimes as a voltage clamp. The DCT, rather than a collector-base diode, is employed because of its low leakage to the substrate. The most important characteristic of the DCT is its adherence to the ideal transistor equation, which may be expressed as:

$$I_d = I_S \exp{(qV_d/kT)}, \tag{1}$$

where I_d = diode current
V_d = diode voltage.

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This is important because many bias currents in integrated circuits are calculated using this equation. Deviations from the ideal diode equation are due to, among others, contact resistance, base resistance, or collector resistance. The most important is collector resistance, particularly for higher resistivity devices such as the μA709. Table XII gives the diode voltage of a μA710 DCT before and after radiation at $I_d = 1$ mA. Notice the large change at 10^{15} nvt.

TABLE XII

DIODE VOLTAGE *(V)* OF μA710 DCT VERSUS RADIATION MEASURED AT *1 mA.*

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
9-2	0.721	0.721			
10-2	0.716	0.713			
11-2	0.706		0.708		
12-2	0.719		0.720		
13-2	0.698			0.710	
14-2	0.717			0.724	
15-2	0.711				0.773
16-2	0.712				0.765

Table XIII gives the diode voltage of a μA709 DCT before and after radiation. The significant difference is that, at 10^{15} nvt, the μA709 diode voltage could not be read because the collector saturated at approximately 40 μA. There is considerable scatter in the μA709 data, making a quantitative statement difficult even at 10^{15} nvt. However, the μA710 does show a definite upward trend, attributed to base current drop across the base resistance. Both types, the μA710 and the μA709 DCT's, should be usable up to 10^{14} nvt.

TABLE XIII

DIODE VOLTAGE *(V)* OF μA709 DCT VERSUS RADIATION MEASURED AT *1 mA.*

DEVICE NO.	RADIATION LEVEL			
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt
2-1	0.720	0.719		
2-2	0.683	0.673		
3-1	0.699		0.696	
3-2	0.699		0.699	
5-1	0.685			0.697
5-2	0.692			0.699

Zener Diodes Zener diodes are used as level-shifting devices in the μA710 and μA711. To determine if any changes took place, the zener voltage was measured at 100 μA. No significant changes occurred at 10^{15} nvt radiation.

Resistors Diffused resistors were tested from the μA702A, μA709, and μA710. All resistors were measured at 0.1 volt to avoid parasitic diode effects. The resistors change very little even at 10^{15} nvt, owing to a low sheet resistivity of approximately 100 Ω/sq. Table XIV gives the pre- and post-radiation data for resistors radiated to a level of 10^{15} nvt. The first three numbers indicate the type of circuit in which the resistor is used. The change is fairly uniform from one device to the next and in no case is greater than 4%. The maximum ratio change is less than 1% for units on the same chip. Since linear microcircuits are designed to depend on ratios and not absolute values, and since radiation changes are small compared to initial component tolerances, resistance change with radiation is considered insignificant.

TABLE XIV

RESISTANCE VERSUS RADIATION OF DIFFUSED RESISTORS MEASURED AT *0.1V* AND RADIATED TO *10^{15} NVT.*

DEVICE NO.	BEFORE ($k\Omega$)	AFTER ($k\Omega$)	% CHANGE
702-151	2.067	2.117	+2.4
702-152	1.957	2.000	+2.1
702-161	2.351	2.402	+2.1
702-162	2.226	2.283	+2.5
709-151	26.40	27.10	+2.6
709-152	26.10	26.70	+2.2
709-161	35.31	36.50	+3.3
709-162	34.61	35.68	+3.0
710- 71	1.020	1.044	+2.3
710- 72	0.950	0.977	+2.8
710- 81	0.730	0.749	+2.5
710- 82	0.720	0.733	+1.8

MICROCIRCUIT PERFORMANCE

In the previous section, a discussion was given of the sensitivity to radiation of the various microcircuit components. In this section, the circuit performance of the linear microcircuits will be discussed. The parameters under consideration include gain, offset, input bias current, and supply current.

Voltage Gain

The differential voltage gain of a differential amplifier is given by:

$$A_V = \frac{I_C R_L}{kT/q},\qquad (2)$$

where A_V = differential voltage gain
  I_C = collector current in one side of the differential pair
  R_L = the collector load resistance

Notice that this equation does not include the effect of finite input impedance or the input impedance of the next stage. The effect of finite input impedance is to lower the effective input voltage; the effect of the input impedance of the next stage is to shunt the collector resistor. Both of these terms are dependent on the common-emitter current-gain. Thus, although the basic voltage gain is independent of radiation, assuming I_C and R_L are constant, the actual voltage gain is current gain-dependent and therefore radiation-dependent. In like manner, the small-signal voltage gain of a grounded-emitter stage can be shown to be $qI_C R_L/kT$. This equation is also independent of current gain, but the same limitations apply.

Tables XV (a) through (d) show the voltage gain versus radiation of the μA702A, μA709, μA710, and μA711, with all data taken at room temperature. Table XV(a) suggests that with selection, a minimum gain of 900 could be guaranteed for the

μA702A at 10^{14} nvt. The technical reason for the gain reduction is probably the loading effect of the second stages, Q_4 and Q_5, on the input stage load resistors (See the schematic given in Figure 3 of Chapter 5).

Table XV(b) gives the gain versus radiation of the μA709 operational amplifier to 3×10^{13} nvt. The guaranteed minimum gain for the μA709 is 25,000. None of the units had a gain that fell this low after radiation. Thus, at 3×10^{13} nvt, all units met the specification for a premium device. There are a number of things which could cause gain reduction, primarily the loading on the input collector resistors by the second stage $(Q_3\text{-}Q_6)$. It is not expected that the later stages will affect the voltage gain because of the feedback network formed by R_{15} and R_7. One radiation effect which may increase the gain is an increase in the diode voltage of the DCT, Q_{10}. This would increase the input stage bias current and the gain of the input stage. However, referring to Table XIII, the voltage change is very small at 10^{14} nvt, and so the effect should be negligible.

Table XV(c) gives the voltage gain versus radiation of the μA710 comparator. This device had good performance up to 10^{14} nvt, where the worst gain was 800. The reduction in gain is attributed primarily to the loading of Q_3 and Q_4 upon R_1 and R_2 (See schematic of Figure 4 of Chapter 7). Notice that the current gain given in Table IV is approximately 25. This gives an input impedance to Q_3 and Q_4 of about $500\,\Omega$, causing a 50% gain degradation, which is roughly what is seen at 10^{14} nvt.

The causes of degradation of the μA711 gain (Table XV(d)) are basically the same as those for the μA710. An important factor to note is that an output signal appeared at the output of all of the μA702A, μA710, and μA711 devices that were radiated to 10^{15} nvt; even at this high level, there were no catastrophic failures.

TABLE XV(a)

VOLTAGE GAIN VERSUS RADIATION OF μA702A DEVICES MEASURED AT $V^+ = 12V$ AND $V^- = -6V$

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	2000	1700			
2	1400	1100			
3	1700	1500			
4	1500	1300			
6	1700		1350		
7	2200		1600		
8	1700		1400		
9	1700		1300		
11	1800			1000	
12	2000			1000	
13	1200			500	
14	1900			950	
16	1300				100
17	1400				25
18	1900				150
19	2000				25

TABLE XV(b)

VOLTAGE GAIN VERSUS RADIATION OF μA709 DEVICES MEASURED AT $V^+ = +15V$ AND $V^- = -15V$

DEVICE NO.	RADIATION LEVEL			
	0	3×10^{12} nvt	10^{13} nvt	3×10^{13} nvt
1	45,000	45,000		
5	43,000	43,000		
7	43,000	43,000		
9	45,000	45,000		
4	44,000		43,000	
6	40,000		34,000	
8	43,000		43,000	
10	40,000		40,000	
13	44,000			30,000
14	44,000			40,000
15	45,000			40,000
19	45,000			43,000

TABLE XV(c)

VOLTAGE GAIN OF μA710 DEVICES VERSUS RADIATION MEASURED AT $V^+ = +12V$, $V^- = -6V$

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	1400	1200		
2	2000	1800		
3	1600	1500		
9	1800		1200	
11	1400		800	
12	1500		850	
17	1600			60
18	1800			65
19	1800			30

TABLE XV(d)

VOLTAGE GAIN OF μA711 DEVICES VERSUS RADIATION MEASURED AT $V^+ = +12V$, $V^- = -6V$

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	1400	1200		
2	1800	1500		
3	1800	1700		
4	1700	1500		
9	1700		800	
10	1800		800	
11	1800		900	
12	1800		1000	
19	2000			60
20	1400			40
21	1800			20
22	1700			60

Input Bias Current

The performance parameters most sensitive to radiation appear to be the input bias current and its correlate, the input resistance. A short calculation will show that the change in input bias current is a function of the common base current-gain degradation. The input bias current, I_B, can be expressed as a function of the DC current gain, β, as:

$$I_B = I_C/\beta. \tag{3}$$

The change in input bias current $I_{B\phi} - I_{BO}$ can be expressed as

$$I_{B\phi} - I_{BO} = I_C/\beta_\phi - I_C/\beta_O. \tag{4}$$

Adding and subtracting

$$I_{B\phi} - I_{BO} = I_C(1 - 1/\beta_O - 1 + 1/\beta_\phi). \tag{5}$$

Assuming fairly high betas

$$\begin{aligned} I_{B\phi} - I_{BO} &= I_C(\alpha_1 - \alpha_2) \\ &= I_C\Delta_\alpha, \end{aligned} \tag{6}$$

where Δ_α = the alpha degradation. Tables XVI (a) through (d) give input bias current versus radiation for microcircuits μA702A, μA709, μA710, and μA711 (recorded at room temperature).

The input stage of the μA702A is biased at approximately 200 μA; hence, an input bias current of 2 μA corresponds to a current gain of 100. From Table I, it is seen that the 100 μA gain at 10^{14} nvt is in the region of 40 to 50; therefore 4 to 5 μA is expected as the input bias current at this radiation level. This is approximately the value obtained on three out of four units. The other unit was a low gain device before radiation and, as such, degraded more after radiation.

The input bias current versus radiation for the μA709 is given in Table XV(b). The input stage is biased at 20 μA, so that an input bias current of 0.1 μA corresponds to a current gain of 200. Extrapolating the data of Table I, a gain of 50 to 75 should be expected at 3×10^{13} nvt at 20 μA collector current. This corresponds to an input bias current of 0.25 to 0.4 μA, within the region of the actual measured currents.

Table XVI(c) shows the input bias current versus radiation for the μA710 comparator. The input stage is biased at 1 mA; an input bias current of 10 μA therefore corresponds to a current gain of 100. Referring to Table IV, gain after radiation ranges from 20 to 30, corresponding to input bias currents of 30 to 50 μA. The units tested, however, ran from 65 to 80 μA. This is attributed to the fact that all the units tested had lower gains than the component transistors tested. The results of the μA711 are virtually identical to the μA710. In Table XVI(d), notice the lower currents at 10^{14} nvt due to higher initial current gains.

TABLE XVI(a)

INPUT BIAS CURRENT (μA) FOR THE μA702A DEVICES VERSUS RADIATION MEASURED AT $V^+ = +12V$ AND $V^- = -6V$.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	3.4	3.7			
2	2.2	2.4			
3	3.1	3.2			
4	3.0	3.4			
6	5.4		6.3		
7	2.9		4.1		
8	3.8		4.8		
9	2.8		3.8		
11	1.7			5.8	
12	1.7			5.5	
13	8.8			16.0	
14	2.0			6.0	
16	9.0				44.0
17	4.5				19.5
18	1.8				22.5
19	2.3				19.5

TABLE XVI(b)

INPUT BIAS CURRENT *(μA)* FOR THE *μ*A709 DEVICES VERSUS RADIATION MEASURED AT $V+ = +15V$ AND $V- = -15V$.

DEVICE NO.	RADIATION LEVEL			
	0	3×10^{12} nvt	10^{13} nvt	3×10^{13} nvt
1	0.12	0.14		
2	0.16	0.19		
3	0.15	0.18		
5	0.09	0.12		
4	0.15		0.27	
6	0.12		0.22	
8	0.07		0.13	
10	0.20		0.30	
13	0.13			0.30
14	0.13			0.32
15	0.21			0.40
16	0.11			0.29

TABLE XVI(c)

INPUT BIAS CURRENT *(μA)* FOR THE *μ*A710 DEVICES VERSUS RADIATION MEASURED AT $V^+ = +12V$ AND $V^- = -6V$.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	29.0	31.2		
2	13.0	19.2		
3	11.0	14.5		
4	9.0	9.1		
9	23.0		66.7	
11	33.0		79.8	
12	29.0		79.6	
17	8.2			225
18	49.0			415
19	19.0			233
20	42.0			361

TABLE XVI(d)

INPUT BIAS CURRENT *(μA)* FOR THE *μ*A711 DEVICES VERSUS RADIATION MEASURED AT $V^+ = +12V$ AND $V^- = -6V$.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	16.5	19.1		
2	14.3	17.8		
3	12.5	14.6		
4	9.6	11.0		
9	12.7		27.8	
10	10.9		25.0	
11	11.0		27.2	
12	7.0		16.7	
19	9.1			74.0
20	21.4			87.3
21	24.9			100.0
22	14.9			84.6

Voltage Offset

The voltage offset of a differential pair, ΔV_{BE}, is found from Eq. (20) of Chapter 2 as:

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right) + \frac{kT}{q} \ln\left(\frac{I_{S2}}{I_{S1}}\right), \qquad (7)$$

where I_{S1} and I_{S2} are the reverse saturation currents of the differential pair. Since a differential pair usually operates with identical collector currents, the voltage offset is mostly due to the mismatch in I_{S1} and I_{S2}. Although radiation tends to increase these, they should track together and the ratio should remain unchanged. Tables XVII(a) through (d) show the voltage offset change versus radiation on the μA702A, μA709, μA710, and μA711 (at room temperature). Only one μA702A changed more than 1 mV up to 10^{14} nvt. All μA711's and μA710's changed less than 1 mV. All μA709's changed less than 0.2 mV, but they were tested only to 3×10^{13} nvt. Since other parameters show much worse degradation, voltage offset change is considered insignificant.

Current Offset

As the current offset, I_{os}, is a function of the current gain mismatch of the input pair, it would be expected that I_{os} would increase with radiation. While this is usually the case, a great number of exceptions were seen. The reason that the current offset does not show a great increase is that, after

TABLE XVII(a)

VOLTAGE OFFSET *(mV)* VERSUS RADIATION FOR μA702A DEVICES.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	+0.8	+0.7			
2	+2.8	+2.5			
3	+0.9	+0.9			
4	−0.8	−0.8			
5	−2.4	−2.0			
6	+0.1		+0.3		
7	+2.0		+1.9		
8	+2.6		+2.7		
9	−1.0		−1.0		
10	−0.6		−0.8		
11	−0.9			−1.4	
12	+0.9			+0.5	
13	−1.8			−3.4	
14	+0.6			+0.4	
15	−0.6			−1.2	
16	+2.0				−6.2
17	−0.4				−6.5
18	−2.9				−6.2
19	−0.2				−4.6
20	−1.8				−7.2

TABLE XVII(c)

VOLTAGE OFFSET *(mV)* VERSUS RADIATION FOR μA710 DEVICES.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	+6.2	+6.2		
2	+6.0	+6.0		
3	+3.6	+3.6		
4	−6.4	−6.3		
9	+5.7		+6.0	
11	+1.4		+1.3	
12	+5.9		+6.1	
17	+1.1			−1.3
18	+2.5			+4.6
19	+2.0			−1.5
20	−0.1			−7.6

TABLE XVII(b)

VOLTAGE OFFSET *(mV)* VERSUS RADIATION FOR μA709 DEVICES.

DEVICE NO.	RADIATION LEVEL			
	0	3×10^{12} nvt	10^{13} nvt	3×10^{13} nvt
5	−0.3	−0.3		
7	+2.1	+2.2		
9	−0.6	−0.5		
2	−3.0	−3.0		
6	−0.2		−0.2	
8	−0.3		−0.2	
4	−0.4		−0.4	
11	−0.8		−0.8	
15	−1.0			−1.0
19	+1.8			+1.8
13	−1.5			−1.4
14	−0.6			−0.6

TABLE XVII(d)

VOLTAGE OFFSET *(mV)* VERSUS RADIATION FOR μA711 DEVICES.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	+1.2	+1.2		
2	+0.4	+0.4		
3	−0.2	−0.15		
4	−4.1	−4.1		
9	+0.6		+1.0	
10	−1.4		−1.0	
11	+0.5		+0.8	
12	+0.6		+1.2	
19	−0.2			+6.4
20	+0.8			+8.6
21	+2.2			Sat
22	−1.4			+0.2

radiation, high gain units have a greater percentage change than low gain units. This tends to equalize the base current and minimize the offset current. Tables XVIII(a) through (d) give the offset current versus radiation for the units tested—again at room temperature.

TABLE XVIII(a)

INPUT OFFSET CURRENT (μA) VERSUS RADIATION FOR THE μA702A DEVICES.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	0	+ .25			
2	+ .05	+ .35			
3	− .45	+ .35			
4	− .85	+ .25			
5	+ .65	+ .25			
6	−1.80		− .50		
7	+ .10		+ .15		
8	+1.80		+ .75		
9	−1.05		− .05		
11	+ .35			− .10	
12	− .05			+ .20	
13	−1.75			−1.00	
14	+ .45			+ .55	
16	+5.10				− .40
17	− .50				− .45
18	+ .30				−1.00
19	− .40				− .50

TABLE XVIII(b)

INPUT OFFSET CURRENT (nA) VERSUS RADIATION FOR THE μA709 DEVICES.

DEVICE NO.	RADIATION LEVEL			
	0	3×10^{12} nvt	10^{13} nvt	3×10^{13} nvt
1	+80	+70		
5	0	0		
7	+90	+90		
9	+70	0		
6	−40		−40	
8	+20		+20	
4	−20		−20	
11	−10		+10	
15	0			0
19	+20			+ 40
13	−20			− 40
14	−90			−110

TABLE XVIII(c)

INPUT OFFSET CURRENT (μA) VERSUS RADIATION FOR THE μA710 DEVICES.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	+1.0	−1.5		
2	+1.0	−2.0		
3	0	− .5		
4	−3.0	+3.0		
9	+4.0		+6.5	
11	+2.0		+2.5	
12	+3.0		+6.5	
17	0			+2.5
18	+13.5			−19.5
19	+1.0			+4.0
20	−2.5			+11.6

TABLE XVIII(d)

INPUT OFFSET CURRENT (μA) VERSUS RADIATION FOR THE μA711 DEVICES.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	−1.0	−1.0		
2	−0.5	+1.0		
3	−1.5	−1.5		
4	−0.5	−1.0		
9	0		0	
10	0		0	
11	−0.5		0	
12	−1.0		−1.0	
19	+1.0			+5.0
20	0			+11.0
21	+1.0			Sat
22	−2.0			−1.5

Power Dissipation

Since the supply current drain is a function of a number of resistors, it is expected that the power dissipation should decrease with increasing radiation. This is indeed the case, but the decreases are somewhat larger than expected, except in the case of the μA709. This is attributed to a change in the output voltage at which power dissipation was measured—before radiation.

Tables XIX(a) through (d) give the power dissipation versus radiation of the units tested.

TABLE XIX(a)
POSITIVE SUPPLY CURRENT (mA) VERSUS RADIATION OF THE μA702A DEVICES MEASURED AT $V^+ = +12V$ AND $V^- = -6V$.

DEVICE NO.	RADIATION LEVEL				
	0	10^{12} nvt	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	7.1	6.9			
2	8.4	6.8			
3	6.8	6.5			
4	7.6	6.7			
6	7.5		7.0		
7	8.5		6.7		
8	7.0		6.4		
9	7.2		6.1		
11	7.0			6.6	
12	7.2			6.7	
13	8.0			6.8	
14	7.8			6.8	
16	7.4				5.1
17	7.6				5.1
18	7.3				4.8
19	6.9				5.0

TABLE XIX(b)
POSITIVE SUPPLY CURRENT (μA) VERSUS RADIATION OF THE μA709 DEVICES MEASURED AT $V^+ = +15V$ AND $V^- = -15V$.

DEVICE NO.	RADIATION LEVEL			
	0	3×10^{12} nvt	10^{13} nvt	3×10^{13} nvt
1	3.45	3.53		
5	3.73	3.28		
7	4.25	4.31		
9	3.40	3.45		
6	3.41		3.48	
8	2.72		2.71	
4	4.16		4.28	
11	3.20		3.28	
15	3.64			3.83
19	4.05			4.18
13	3.45			3.51
14	3.07			3.08

TABLE XIX(c)
POWER DISSIPATION (mW) VERSUS RADIATION OF THE μA710 DEVICES MEASURED AT $V^+ = +12V$ AND $V^- = -6V$.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	94.2	94.5		
2	81.6	81.6		
3	83.4	85.1		
4	85.1	86.0		
9	109.0		107.5	
11	96.4		93.5	
12	99.0		96.5	
17	204.0			169.7
18	100.0			72.1
19	64.4			45.7
20	96.0			70.2

TABLE XIX(d)
POWER DISSIPATION (mW) VERSUS RADIATION OF THE μA711 DEVICES MEASURED AT $V^+ = +12V$ AND $V^- = -6V$.

DEVICE NO.	RADIATION LEVEL			
	0	10^{13} nvt	10^{14} nvt	10^{15} nvt
1	137	132		
2	143	129		
3	159	153		
4	109	100		
9	127		117	
10	133		133	
11	130		116	
12	120		105	
19	130			100
20	146			109
21	147			106
22	147			109

SUMMARY AND CONCLUSIONS

It has been shown that the predominant effect of radiation on microcircuit components is the degradation of current-gain. Both base-transport factor and emitter efficiency are reduced. Resistors change less than 4 percent at 10^{15} *nvt*. Other changes are insignificant.

With circuit parameters, the largest change is seen in the input bias current. The amount of change in voltage gain is a function of current gain dependence and feedback. Voltage offsets and current offsets change little at levels at which other parameters are largely degraded. Power dissipation is generally reduced. Most units were within specification at 10^{14} *nvt*, indicating that microcircuits compare favorably to discrete components in regard to fast neutron radiation.

APPLICATIONS

This chapter presents some of the possible circuit applications using the linear integrated circuits described in the preceding sections. In general, the "C", or industrial grade, versions of the devices specified may be substituted in the circuits unless specifically stated otherwise. Due regard must be taken, however, of certain relaxations in specifications and the reduced operating temperature range. Also, in most of the operational amplifier circuits, either μA702A or μA709 may be used, with suitable alterations being made in the circuit for parameter differences such as gain, common mode range, supply voltage, etc.

For ease of location, the circuits are loosely grouped into the following categories:

> DC Amplifiers
> AC Amplifiers
> Precision Supplies
> Nonlinear Circuits
> Special Functions
> Comparators
> Consumer Circuits
> Core Memory Sense Amplifiers

SECTION A   DC AMPLIFIERS

RESISTANCE BRIDGE AMPLIFIER

Probably one of the largest potential uses for the μA702A is as a signal conditioner for a telemetry system. One such application is shown in Figure 1. Here, the differential output of a thermistor bridge is amplified by 10. A single-ended output is obtained such that the amplifier output is zero when the bridge is balanced. The high common mode and supply rejection of the amplifier give a null independent of supply voltage. In the circuit shown, the null drift of the bridge due to the amplifier will be less than $1mV$ over the temperature range of $-55°C$ to $+125°C$.
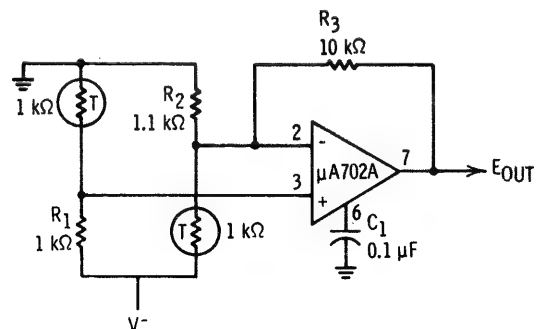
Fig. 1 Amplifier for Thermistor Bridge.

SOLAR CELL AMPLIFIER

Figure 2 gives the schematic for a circuit developed as a servo-amplifier in a system where light falling on two solar cells is detected and amplified to drive a servo-positioning motor. The polarity of the output depends upon the relative strength of illumination between the two cells. The common-mode operating point is at approximately half the negative supply voltage, and the sensitivity is $50mV/\mu A$. The amplifier responds to the short-circuit current of the sensors as the voltage across them is kept less than a few mV.
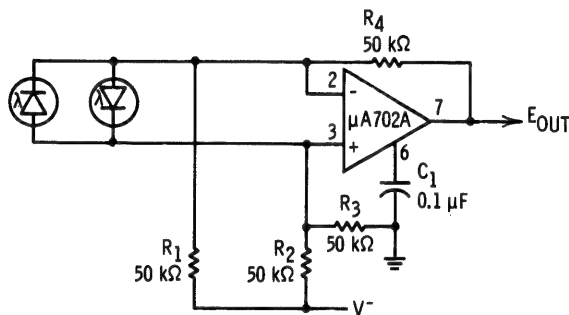
Fig. 2 Preamplifier for Servo System Using Solar Cell Sensors.

INTEGRATOR

The $\mu A702A$ can also be used as an integrator or low-pass amplifier as shown in Figure 3. The 3-dB point in the frequency response will occur for $R_3 = 1/(2 \pi f C_1)$. The capacitor from the non-inverting input to ground (C_3) is required in addition to the frequency compensation to eliminate the effect of the input capacitance on that terminal.
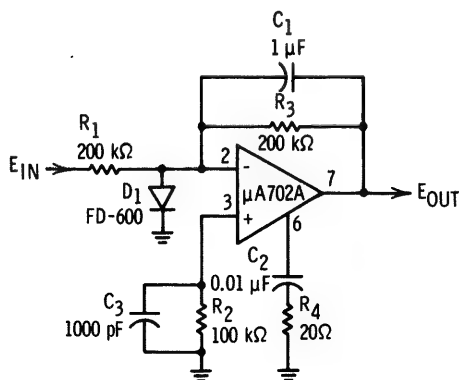
Fig. 3 Integrator or Low-Pass Amplifier.

VOLTAGE FOLLOWER

In one particular application, the limited common-mode range of the $\mu A702A$ does restrict its use when large voltage swings are required. This happens when it is used as a unity gain, non-inverting amplifier. The difficulty may be avoided to a certain extent with the circuit in Figure 4. The common-mode range is actually "bootstrapped" by connecting the output to pin 1. With this circuit, the amplifier may be operated as a voltage follower with output swings of $\pm 3V$.
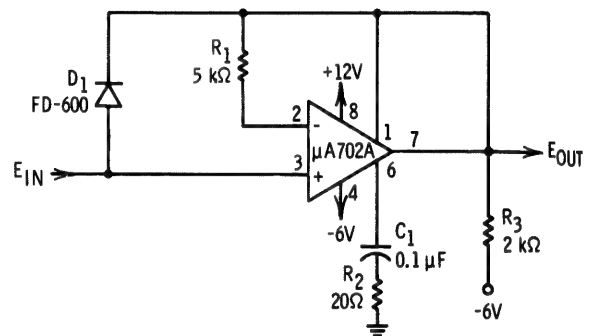
Fig. 4 Voltage Follower.

HIGH-INPUT IMPEDANCE AMPLIFIER

A modified Darlington connection can be used to obtain higher input impedance and lower offset currents than are possible with the $\mu A702A$ alone. This is shown in Figure 5. A high-gain, matched transistor pair is used to increase the input impedance. Resistors R_1 and R_2 reduce offset voltage and noise, and make the gain and open-loop frequency response almost unaffected by the addition of an
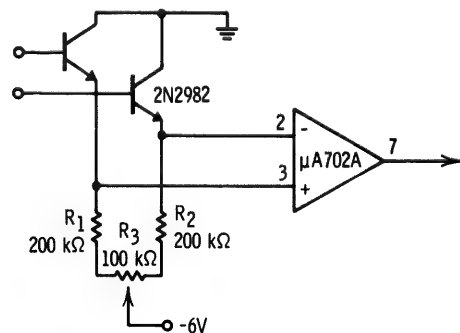
Fig. 5 Circuit for Using Emitter-Follower Inputs on the $\mu A702A$ with a Connection Which Eliminates Possible Latch-Up Condition — Provisions are Also Made for Balancing Offset on the Input.

input stage. A convenient offset null is provided with R_3, although it may be eliminated if not required. It is interesting to note that this method of zeroing offset also minimizes temperature drift. An additional feature of this circuit is that the collector-base diodes of the added transistor also serve as clamping diodes, which prevent driving the amplifier into a latch-up condition by exceeding the common-mode voltage range.

MEDIUM-POWER AMPLIFIER

The μA716 can be used in DC as well as AC applications as a medium power output stage. Figure 6 shows how it can be used with a μA702A to form an operational amplifier having the low input offset and drift of the μA702A, together with the low distortion and high output current capability of the μA716. The open-loop voltage gain of the composite amplifier is 36,000, the closed-loop gain is 200, and the typical input offset voltage is 1.5 mV. The amplifier can deliver 15 V_{pp} to a 150Ω load with less than 0.5% distortion from DC to 10 kHz.
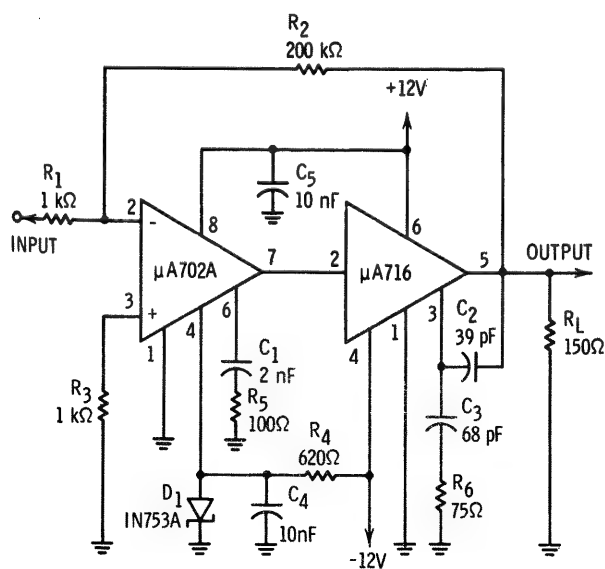
Frequency compensation is provided by $C_1 - R_5$ for the μA702A, and by $C_2 - C_3 - R_6$ for the μA716.

LOW DRIFT AMPLIFIER

The primary application of the μA726 is as an input stage for DC differential amplifiers. The circuit of Figure 7 shows how the μA726 can be used as a preamplifier for a μA709 operational amplifier. The first μA726, A_1, is the differential input stage and has a gain of about 70; collector current is set at 10 μA by the constant current source Q_1. The second μA726, A_2, is connected as a pair of emitter-followers to keep the temperature-dependent offset current of the μA709 from unbalancing the collector currents of A_1 and producing an input offset voltage drift. The temperature coefficient of resistors R_4 and R_5 should match to 10 $ppm/°C$. The composite amplifier typically has an over-all gain of approximately 3,000,000, and initial offset voltage of 1 mV, an offset current of 10 nA, a voltage offset drift of 0.2 $\mu V/°C$, and a current offset drift of 10 $pA/°C$ from $-55°C$ to $+125°C$. Using the extreme limits for the parameters of A_1, A_2, and A_3, the worst-case drift will be less than 1.5 $\mu V/°C$. Frequency compensation for the amplifier is provided by C_1, R_6, C_2, R_{10}, and C_3. For applications with closed-loop gain greater than unity, capacitor C_1 should be reduced and resistor R_6 increased accordingly; C_1 should be a low leakage capacitor. For gains of 100 or greater, C_1 and R_6 are not needed.

Fig. 6 Medium Power Amplifier.

For applications in which a somewhat higher input offset current drift can be tolerated, the μA726 designated A_2 and resistors R_7, R_8, and R_9 can be eliminated, and the output of amplifier A_1 fed directly into A_3. Resistor R_1 should be decreased to 75$k\Omega$ and resistors R_4 and R_5 decreased to 24.3$k\Omega$. The $C_1 - R_6$ compensation network should be changed to 10 μF and 300Ω for unity-gain. The resulting amplifier typically has an over-all gain of 3,000,000, an input voltage offset of 1.0 mV, an input current offset of 50 nA, a voltage offset drift of 1 $\mu V/°C$ and a current offset drift of 30 $\mu A/°C$. The maximum expected offset voltage drift with this circuit is about 2 $\mu V/°C$.
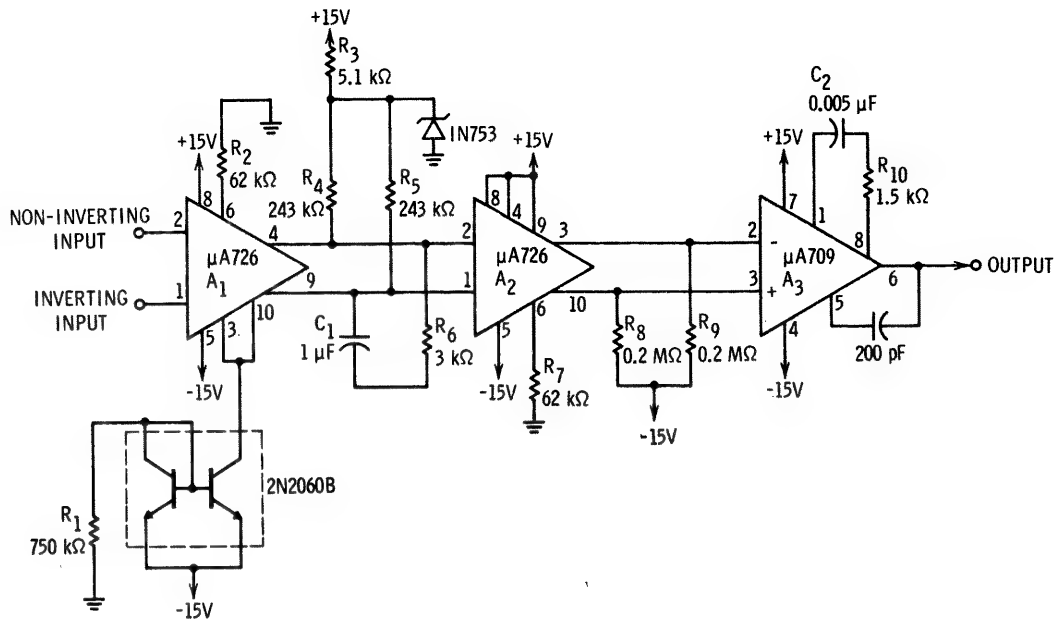
Fig. 7 High-Gain, Low-Drift DC Amplifier.

SECTION B   AC AMPLIFIERS

PIEZO-ELECTRIC TRANSDUCER AMPLIFIER

Figure 1 shows a circuit with high input impedance suitable for amplifying the output from a piezo-electric transducer. Positive feedback (bootstrapping) is used to remove the shunting effect of the input bias resistor (R_3) on the input impedance. The voltage gain of the circuit is 3, and the input impedance is in excess of $5M\Omega$. The lower cutoff frequency of the amplifier, as shown, is $1Hz$.
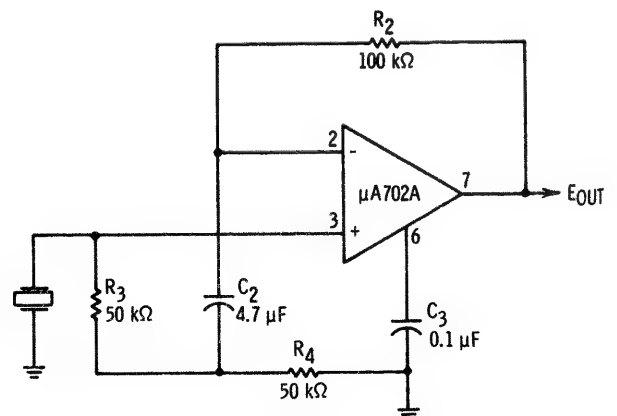
Fig. 1 High Input Impedance Amplifier for Piezo-Electric Transducer.

TAPE HEAD AMPLIFIER

A low-noise preamplifier for use with low-level audio or instrumentation tape heads is shown in Figure 2. A matched pair of low-noise transistors is used as a differential input stage to provide good common-mode rejection and high input impedance, after which the μA702A provides amplification. Over-all feedback is not employed, but a reasonably constant gain of 100 is provided. With the circuit configuration used, the common-mode range is considerably in excess of that of the μA702A alone, particularly in the positive direction.
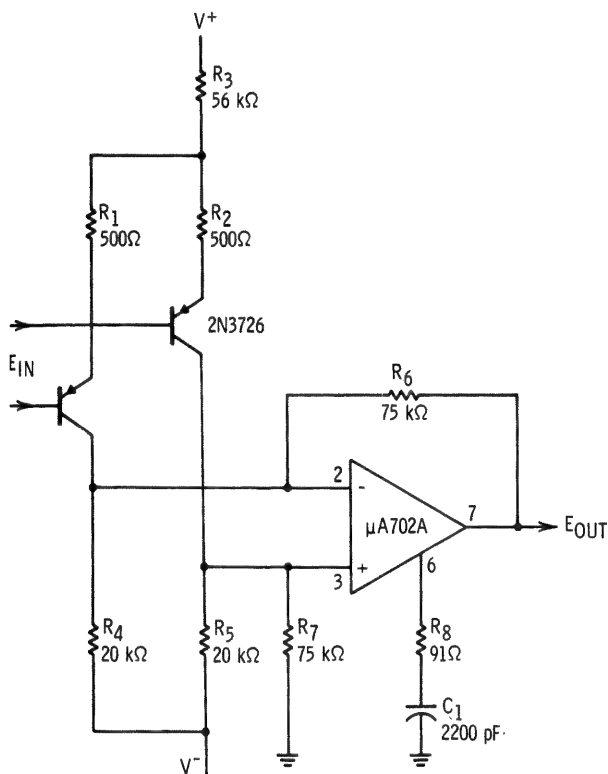
Fig. 2 Low-Noise, High Input Impedance Amplifier for Use with Low-Level Tape Head. Circuit Features Differential Input for Noise Rejection.

DELAY EQUALIZER*

Facsimile, high-speed telegraphy, and data transmission are extremely vulnerable to delay distortion. For the compensation of this distortion in carrier systems and associated equipment, types of corrective networks are required that may be

readily designed and individually adjusted to meet the conditions of a particular application. Generally designated as all-pass circuits, such networks have an amplitude characteristic that is essentially independent of frequency throughout the useful frequency range. A typical equalizer consists of a number of all-pass sections in tandem, each of which inserts a controlled amount of delay at selected frequencies.

A delay equalizer section using the μA702A is shown in Figure 3. Its operation can be understood by writing the transfer function for the general configuration shown in Figure 4:

$$\frac{V_{out}}{V_{in}} = \frac{(Z_1 + Z_4)\, Z_3 - (Z_2 + Z_3)\, Z_4}{(Z_1 + Z_4)\,(Z_2 + Z_3) - Z_4\,(Z_2 + Z_3)} \quad (1)$$

For $Z_1 = Z_4$, $Z_2 = jX$ and $Z_3 = R$, Eq. (1) becomes

$$\frac{V_{out}}{V_{in}} = \frac{R - jX}{R + jX} \quad (2)$$

which is the desired characteristic of an all-pass network.
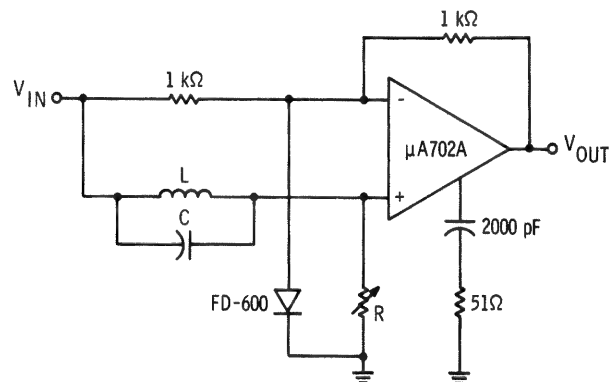
Fig. 3 Delay Equalizer Section Using the μA702A.
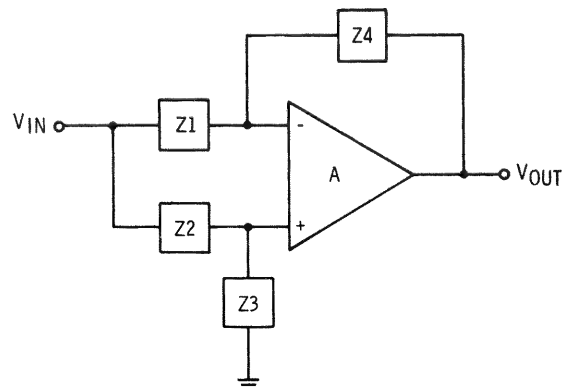
Fig. 4 General Configuration of a Delay Equalizer Section.

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The advantages of the circuit become evident by comparing it with the conventional delay equalizer shown in Figure 5. The conventional circuit requires an audio transformer and a large tantalum capacitor to operate properly at low frequencies. However, the differential input of the μA702A eliminates the need for a transformer (or a more complicated bridged section) while the low offset of the amplifier allows a large number of amplifiers to be directly coupled. In addition, the high open-loop gain gives a large amount of negative feedback and permits the desired transfer function to be approached more closely. These advantages are particularly significant when one considers that many applications require eight or more sections in tandem.
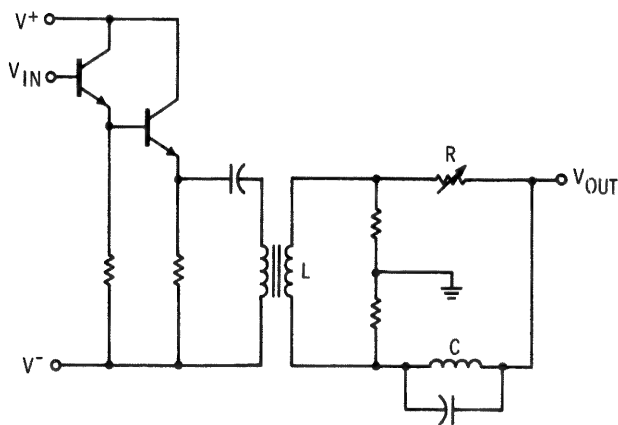
Fig. 5 Conventional Delay Equalizer Section.

SERVO CURRENT DRIVER

A fairly typical example of an application in which an operational amplifier would not normally be considered — but in which a μA702A can be used quite effectively — is shown in Figure 6. This is a push-pull, Class-B, servo current driver.

The output current of opposite sides is sensed across R_8 and R_{13}. One μA702A (A_1) functions as a unity-gain, non-inverting amplifier that makes the voltage across R_8 equal to the input voltage for positive input signals. For negative input signals, A_2 functions as a unity-gain, inverting amplifier that forces the voltage across R_{13} to be equal to the input voltage. Thus, phase inversion for the push-pull amplifier is obtained. The quiescent output current of the amplifier is determined by R_4 and R_9, and, with the values shown, will be approximately 20 mA on each side. The circuit provides a $\pm 2A$ output current for a $\pm 2V$ input signal. The input resistance is $4k\Omega$.

It is immediately obvious that the excellent DC characteristics of the μA702A permit biasing of the output stage at very low quiescent currents
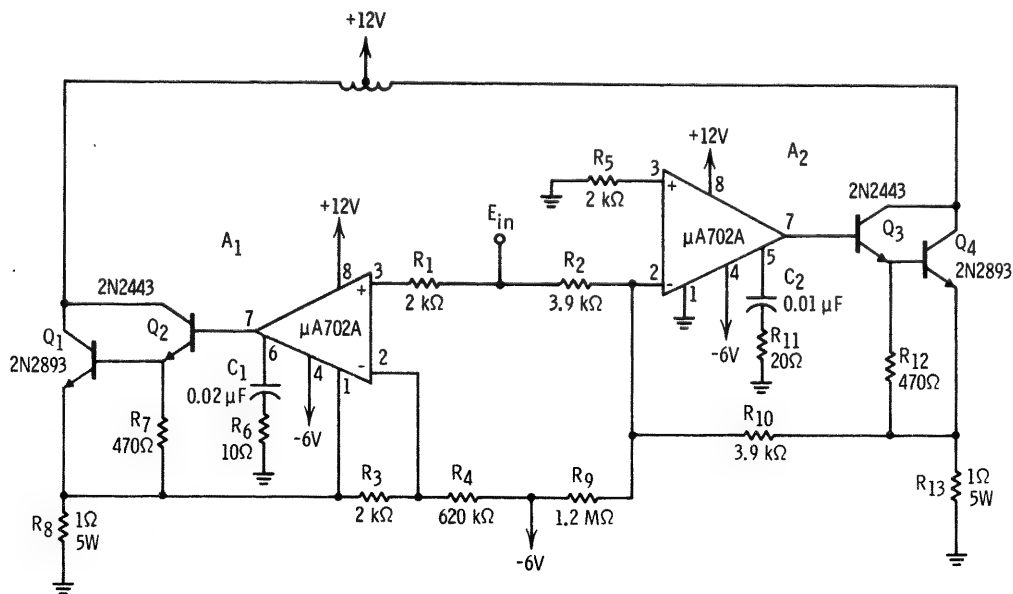
Fig. 6 Class-B Servo Current Driver.

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without running the risk of thermal runaway or of encountering a dead zone — even for operation over the full temperature range. It is also apparent that the low offset and high gain provide reasonable accuracy without an excessive waste of supply voltage across the current-sensing resistors. Since the output transistors are included within the feedback loop, their characteristics have a negligible effect on over-all performance.

One unusual aspect of this circuit is that the ground terminal of A_1 (pin 1) is connected to the current-sensing resistor, R_8. This provides bootstrapping on the common mode range of the amplifier so that it can be operated above its usual common mode limit of $+0.5V$ without exceeding ratings.

HEADPHONE AMPLIFIER

Figure 7 shows an amplifier suitable for driving a pair of earphones for broadcast station, aircraft, and military communications receivers. It is also excellent for language laboratories, electronic teaching machines, geiger counters, telephone switchboards, and other general communications applications.
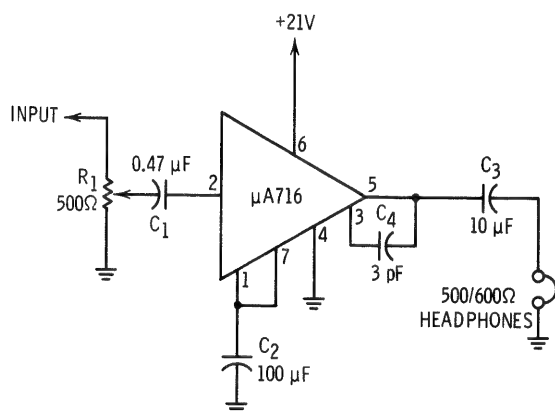
Fig. 7 X100 Headphone Amplifier.

The μA716 general-purpose amplifier can deliver 50 mW to a 500/600Ω headset with less than 0.2% distortion over the entire audio frequency band. Potentiometer R_1 is the volume control, C_1 and C_3 provide input/output coupling, and C_4 is for stabilization. Voltage gain is selected by bypassing the appropriate gain taps with C_2 (connected for 40 dB gain in the circuit shown).

ELECTROCARDIOGRAPH PREAMPLIFIER

The differential amplifiers used for electrocardiograph work must have high common mode rejection, very high differential input impedance, and low noise over a bandwidth of about 0.1 Hz to 100 Hz. Another characteristic generally required of such circuits is that they be direct-coupled; this permits input switching without having to wait several seconds for the amplifier to recover from the overload caused by switching transients in the coupling capacitors. With DC coupling, however, the electrodes may see differential DC voltages up to ± 100 mV on the skin of the patient, while the useful signal is around 1 mV. Hence, the amplifier must have a large dynamic range at the output to accommodate this DC signal, while maintaining a high common mode rejection ratio at the input.

The dual amplifier input circuit of Figure 8 has extremely high input impedances — both differential and common mode. As a result, the circuit is quite insensitive to imbalances in the source impedances that might occur if one of the electrodes is not properly connected to the patient. The outputs of amplifiers A_1 and A_2 are:

$$e_1 = V_{CM} - V_{IN}\left(\frac{R_1}{R_2} + \frac{1}{2}\right) \qquad (3)$$

$$e_2 = V_{CM} + V_{IN}\left(\frac{R_3}{R_2} + \frac{1}{2}\right), \qquad (4)$$

and hence the differential output for $R_3 = R_1$ is

$$e_2 - e_1 = V_{IN}\left(1 + 2\frac{R_1}{R_2}\right). \qquad (5)$$

The cross-coupling between the amplifiers via R_2 reduces the common mode gain to unity but amplifies the differential signal (unlike a normal pair of voltage-followers). The component values shown provide a differential gain of 50, which leaves margin in the output swing capability of the μA709's for a maximum common mode signal of $\pm8V$, a differential DC offset of ±100 mV, and the normal input signal. The third amplifier converts the differential signal to single-ended, and boosts the gain to 5000. Capacitors C_1, C_3, C_6, and C_7 limit the bandwidth to 100 Hz to reduce high-frequency noise and pickup.

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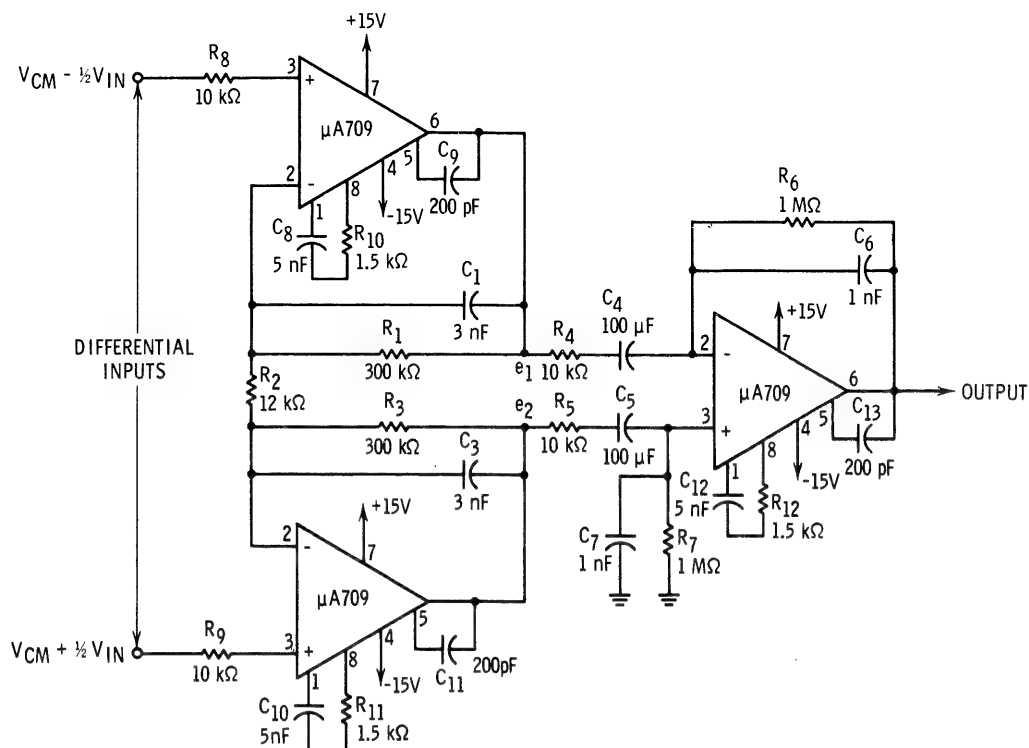
Fig. 8 Electrocardiograph Preamplifier.

HIGH-GAIN, PRECISION AC AMPLIFIER

Two μA702A's connected in cascade comprise the circuit shown in Figure 9, which has an open-loop gain of 140 dB and a closed-loop gain of 70 dB with 0.1% accuracy. To obtain an effective input impedance greater than 100 $M\Omega$, the input bias resistor for the non-inverting input, R_3, is boot-strapped via C_2 to the summing junction. The second amplifier is driven from the lag frequency compensation terminal to provide protection for its inputs; D_1 and D_2 prevent latch-up. The two frequency compensation networks, $C_3 - R_4$ and $C_4 - R_5$ are proportioned so that full output swing may be obtained from the amplifier to frequencies in excess of 100 kHz. Care should be taken with parts layout, lead dress, and power supply decoupling to ensure that oscillations are not caused by the extremely high gain and wide bandwidth of the circuit.
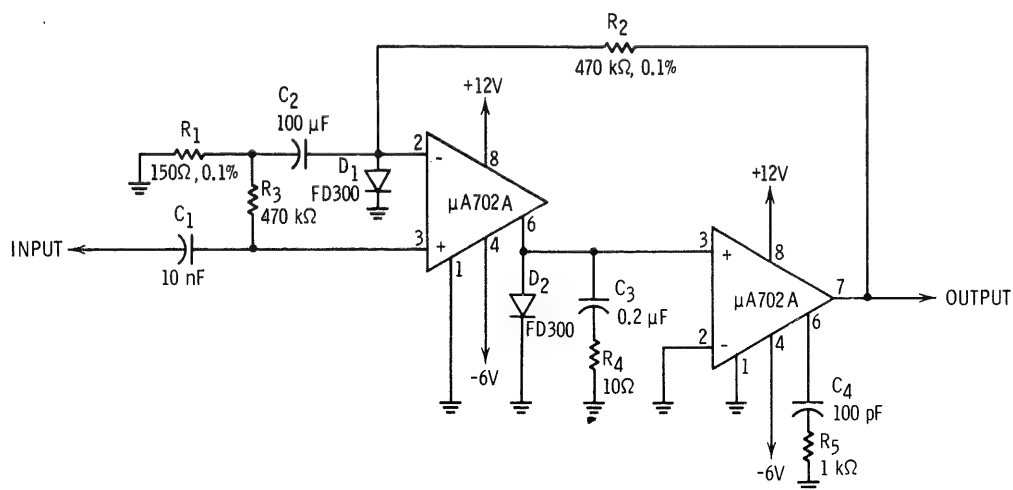
Fig. 9 Precision High-Gain AC Amplifier.

Figure 10 shows the schematic of a 100 *MHz* RF amplifier using the μA703. As with all circuits using the μA703 at frequencies above 30 *MHz*, the low input terminal (pin 5) should be decoupled to ground. This is necessary for two reasons:

1) The two diodes (or saturated transistors) between pins 5 and 4 are not a perfect short circuit and so do not completely decouple the base of the grounded base transistor of the emitter-coupled pair.

2) The high frequency current gain is falling off at 6 dB/octave at frequencies above 30 *MHz*. This results in more base current at high frequencies and consequently more RF current in the two decoupling diodes or external decoupling capacitance.

Without the additional bypass capacitance, both the power gain and the gain figure are decreased by about 8 dB.

The μA703 may be used as a current mode limiter if the total output admittance (including "g_{22}") is more than about 0.3 *mmho*. The power gain will be a little under 20 dB. Reverse AGC may be obtained by bleeding current from pin 5, thereby reducing the value of the current in the emitter-coupled pair.

The circuit for the measurement of power gain and noise figure at 200 *MHz* (Figure 11) is essentially the same as used at 100 *MHz* with, of course, changes in the values of the tuning components.

Typical Performance Figures
(12 *V* supply, $f = 100MHz$)

1. Power Gain   20-21 dB
2. Noise Figure   6 dB
3. Bandwidth   5 *MHz*
4. Gain Figure $\left|\dfrac{y_{21}}{y_{12}}\right|^2$ $= 62$ dB
5. Maximum Stable Gain $\left|\dfrac{y_{21}}{y_{12}}\right| = 31$ dB

The "*y*" parameters for the μA703 at 100*MHz* are:

$$y_{11} = 1.2 + j3 \; mmhos$$
$$y_{22} = 0.2 + j1.5 \; mmhos$$
$$y_{21} = 19 \; mmhos$$
$$y_{12} = 0.015 \; mmhos$$

Typical Performance Figures
(12 *V* supply, $f = 200MHz$)

1. Power Gain   14 dB
2. Noise Figure   7.5 dB
3. Bandwidth (−3*dB*)   10 *MHz*
4. Gain Figure   41.5 dB
5. Maximum Stable Gain 20.5 dB

The "*y*" parameters for the μA703 at 200 *MHz* are:

$$y_{11} = 2 + j6.3 \; mmhos$$
$$y_{22} = 0.7 + j3.2 \; mmhos$$
$$y_{21} = 12 \; mmhos$$
$$y_{12} = 0.12 \; mmhos$$
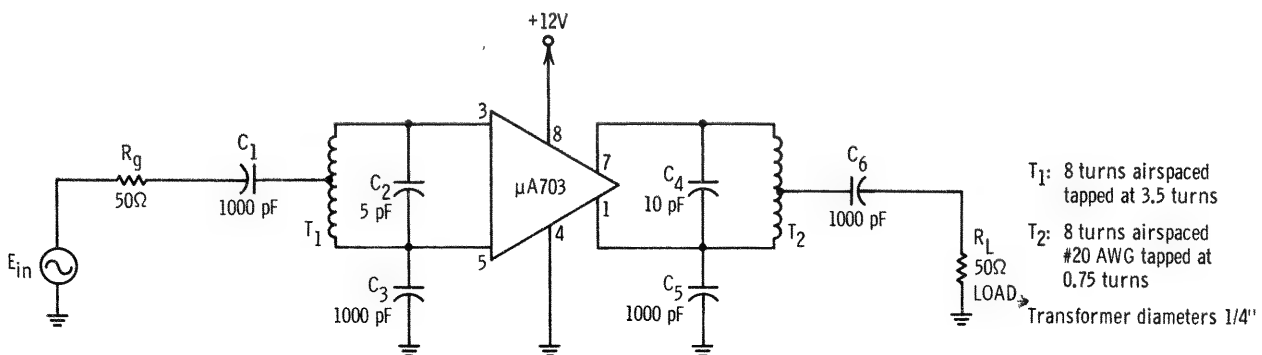
Fig. 10 100 MHz RF Amplifier.
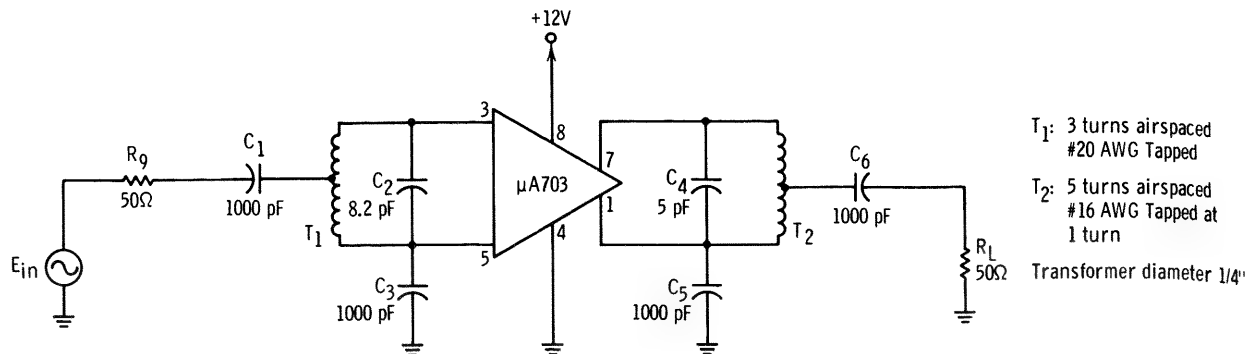
Fig. 11 200 MHz Test Jig.

SECTION C   PRECISION VOLTAGE SUPPLIES

SUPPLIES USING THE μA709

Although temperature-compensated voltage reference diodes can provide excellent temperature stability, they are only available in rather odd voltage ranges and may have a large tolerance on the actual zener voltage. In addition, the current that can be drawn from these sources without upsetting the temperature coefficient is usually limited to less than 10% of the bias current.

Operational amplifiers can be used as buffers for these references to prevent loading and to provide a convenient means of voltage adjustment. Two possible circuits are shown in Figure 1. The circuit of Figure 1(a) gives an output voltage greater than the zener reference, and that of Figure 1(b) gives an output less than the reference. The high input impedance, low offset voltage, and low thermal drift of the μA709 make possible excellent isolation without degrading the stability of the

(a)

(b)
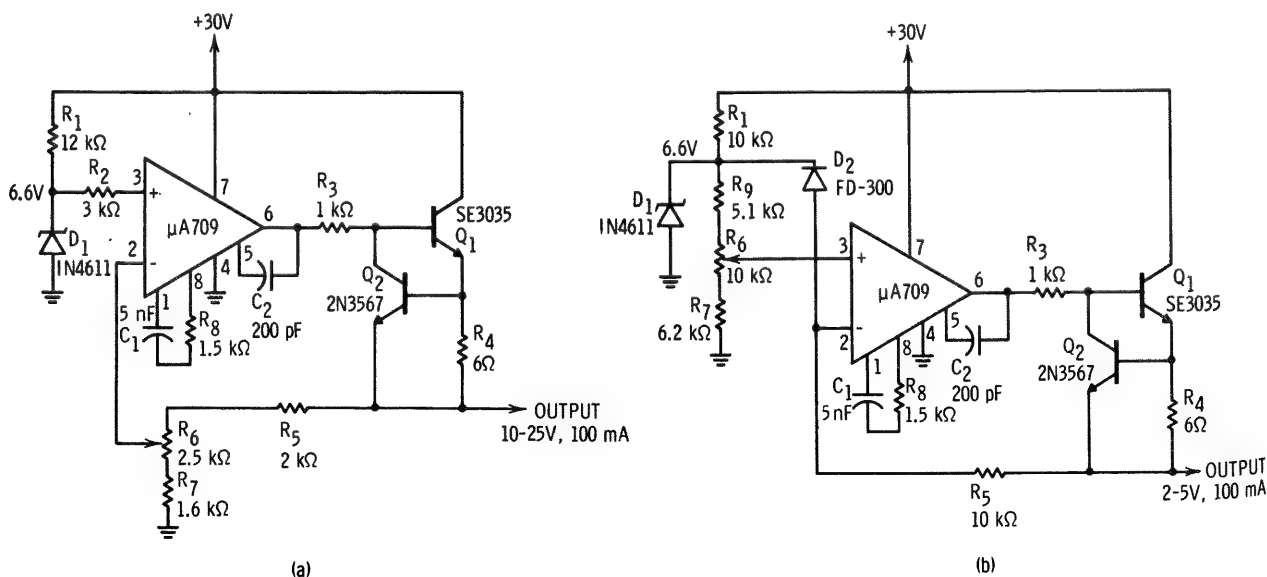
Fig. 1 Precision Voltage Supplies.

reference. An interesting feature of the μA709 in this application is that it can be operated from a single power supply, and so no negative voltage source is necessary.

An additional emitter-follower, Q_1, is used at the output to deliver a larger output current than could be supplied by the μA709 alone. Output protection is provided by Q_2, which limits the base drive to Q_1 when the output current exceeds 100 mA. The current limit can be adjusted by varying R_4. Figure 2 shows the output voltage versus output current characteristic of the circuit, and illustrates the excellent regulation obtained up to the current-limiting point. For applications requiring only moderate output capability (10 mA), the μA709 can be used alone and Q_1, Q_2, R_3, and R_4 can be eliminated from the circuit.

The circuit of Figure 1(b) is similar to that just described, except the amplifier is operated at unity-gain with its input taken from a tap across the reference diode. Minimum output voltage is limited to 2 V to keep the amplifier inputs within their operating common-mode range. Diode D_2 protects the amplifier inputs, and C_1, C_2, and R_8 provide frequency compensation (for both circuits).

Normally, the μA709 is capable of 28-V_{pp} output swings when biased with $\pm$ 15 V supplies. The 100-V DC regulator circuit shown in Figure 3 uses a single μA709 as the control element, but in a modified bootstrap configuration that accomplishes two objectives:

1) It allows greater than 60 V output adjustment range.
2) It operates within its specified power supply range.

When operated in this manner, both the regulation (better than 0.01%) and the range of nominal output voltages (up to 250V) are better than standard ground-referenced circuitry. The bootstrap effect is accomplished by the 30-V zener diode. This stabilizes the voltage across the operational amplifier at a level that is within the μA709's rating, and that tracks the output voltage within the control range of the operational amplifier over a wide range of output voltages.

Fig. 2 Regulator Output Voltage versus Load Current.
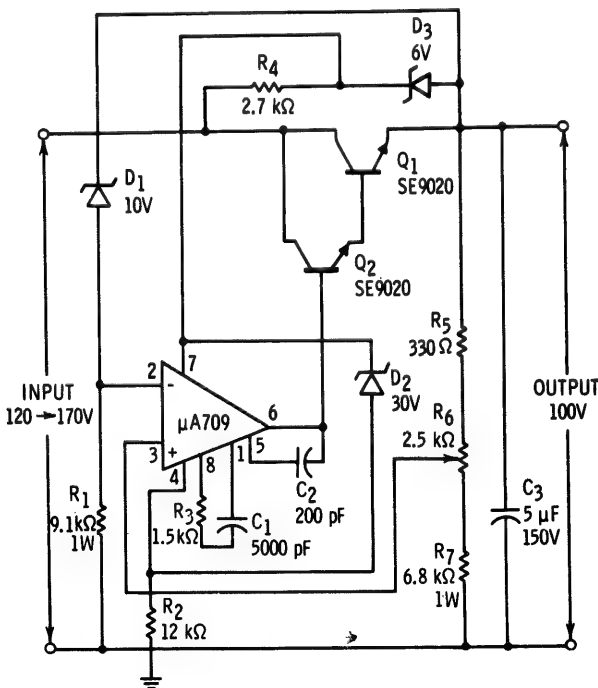
Fig. 3 High Voltage Supply.

SUPPLY USING THE μA702A

A circuit for a precision voltage source using the μA702A operational amplifier is given in Figure 4. Since the magnitude of the zener voltage is outside the normal common-mode range of the amplifier, a different method from that used with the μA709 circuits must be employed to develop the input voltage to the circuit. The input voltage is forced to be equal to the output voltage minus the reference by connecting the zener between the output and the inverting input. The voltage divider, R_3, R_4, between the output and the non-inverting input then determines the magnitude of the output voltage. As with the other circuits, Q_1 supplies large output current and Q_2 provides current limiting. The $R_6 - D_2$ network ensures starting of the regulator under any conditions. In this application, the μA702A is operated between $+18V$ and ground; it is not necessary to make connection to the common terminal of the amplifier since it will normally seek a level of $+6V$.

The basic circuit can be explained with the aid of the simplified schematic given in Figure 5. The μA710 is connected as a level detector with hysteresis, and the regulator reference voltage is fed to the non-inverting input. Therefore, the comparator will switch on when the voltage on the inverting input is slightly below the reference; and it will switch off when this voltage is slightly above the reference. When the comparator turns on, it drives Q_1 which saturates Q_2, applying the DC input voltage to the load through L_1. The output voltage is sent back to the inverting input of the comparator; hence, when the output voltage rises above the reference voltage, the comparator turns off. The output voltage now falls at a rate determined by L_1 and C_1. When it drops by an amount equal to the hysteresis, the comparator turns back on, and the output again rises. Therefore, the circuit operates in a self-oscillating mode in such a way as to maintain a constant ripple voltage across the load independent of input voltage or load.

Fig. 4 Precision Voltage Supply.

Fig. 5 Simplified Schematic of the Switching Regulator.

SWITCHING REGULATOR USING THE μA710

A circuit which demonstrates the flexibility of the μA710 is the high-power switching regulator shown in Figure 6. It is capable of delivering an output current greater than $2A$ at better than 85% efficiency. The output voltage is adjustable over a very wide range, and the load and line regulation is better than 0.5%. The operating frequency is about $10kHz$ and the output ripple is less than $10 \ mV$. Current limiting is provided to keep the dissipation in the power-switch transistor at a safe value.

The purpose of the diode in Figure 5 is to provide a return path for the inductor current after the switching transistor turns off. The size of the inductor has a considerable influence on the efficiency. If the inductor is large enough to maintain a relatively constant current through the switching cycle, it is easy to see how it is supplying the load current continuously. However, this current (which is equal to the load current) is only being supplied by the input voltage source for part of the cycle. The inductor is acting as a source, supplying current through the diode, for the remainder. Therefore, the average input current is less than the

output current. As the inductor is made smaller, the peak currents become greater, increasing the losses in the power switch transistor, the inductor, and the diode.

An interesting feature of the circuit is that if the inductor is made large enough so the current through it does not go to zero through the cycle, the operating frequency will be affected little by the load or the input voltage. Instead, it will be determined by the inductor, the output capacitor, and the amount of hysteresis on the comparator.

The complete schematic of the switching regulator is shown in Figure 6. A pre-regulator (Q_3, R_5 and D_3) is used to supply current for the temperature-compensated, voltage-reference diode, D_1, and to provide power for the μA710. The comparator is operated from supply voltages of $0V$, $+6V$, and $+18V$ instead of the usual positive-negative voltage combination. The $+6V$ is provided by zener diode, D_2. An emitter-follower transistor, Q_4, is added at the output to increase the output-current capability. Q_5 serves as the current-limiting transistor: when the peak output current exceeds about $3A$, the power switch transistor is no longer required to maintain the output

voltage. Instead, Q_5 supplies current directly to the inverting input of the comparator. The power transistor still switches, but does not have to handle anywhere near the full short-circuit current at the maximum supply voltage, as would be required with conventional current-limit schemes.

The output voltage is established with the resistive divider formed by R_7 and R_8. A potentiometer can be substituted to make this voltage continously variable, with the zener reference voltage determining the lower limit of adjustment, and the input voltage and breakdown voltage of the discrete transistors determining the upper limit. If additional ripple filtering is desired, it can be added without degrading regulation by connecting R_8 to the output of the added filter instead of to C_6, but keeping C_4 connected to C_6 to provide the self-oscillating feedback. R_8 can also be used for remote-voltage sensing in this manner.

Because of the relatively high operating frequency of the circuit, all large-value capacitors should be solid tantalum, and all low-value capacitors should be disc ceramic to provide adequate bypassing.
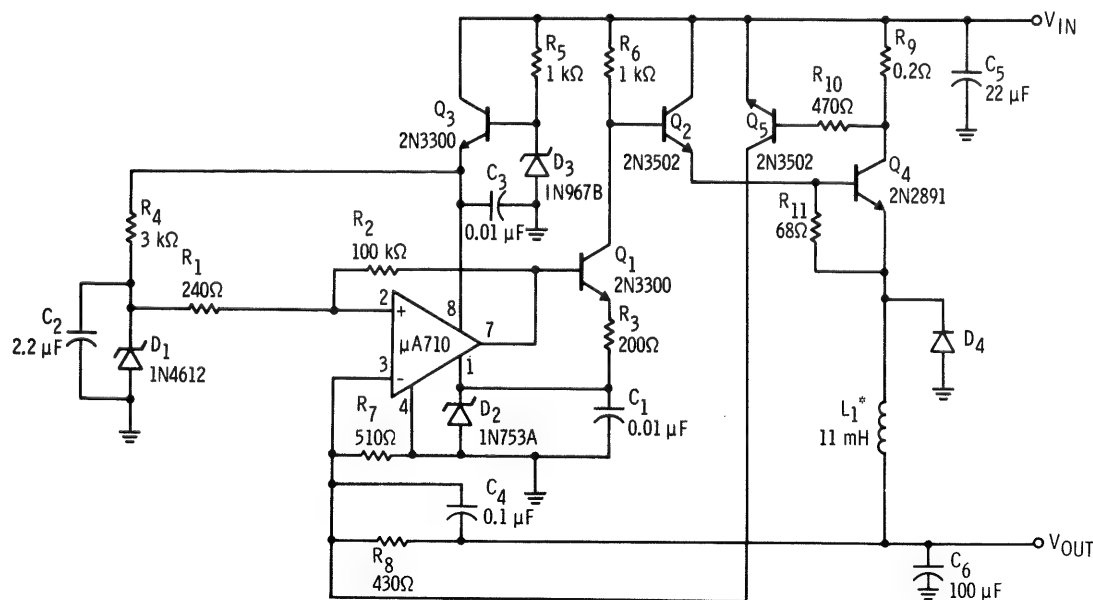
*250 turns #20 enameled copper wire wound on Molybdenum Permalloy Toroid (Arnold Engineering Co. #253168-2)

Fig. 6 High Power Switching Regulator.

SECTION D   NONLINEAR CIRCUITS

HALF-WAVE RECTIFIER

In many circuits such as rectifiers, clippers, clampers, and peak detectors where diodes are characteristically called for, the threshold voltage of the diode can be a significant problem. This is particularly true in low-level circuits. In these cases, an operational amplifier is quite useful in that it can be used to reduce the effective threshold of the diodes by several orders of magnitude.

Figure 1 gives an example of this. It functions as a half-wave rectifier or ideal diode circuit. The output is an inverted replica of negative input voltages, and is zero for positive input voltages. The threshold voltage of the silicon diodes is divided by the open-loop gain of the amplifier, so it is less than 1 mV.
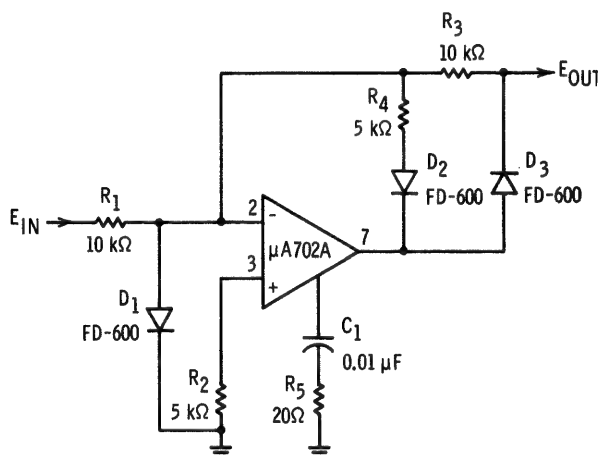
Fig. 1 Half-Wave Rectifier.

PEAK DETECTOR

One difficult problem that can be solved with the $\mu A710$ is the accurate measurement of the peak amplitude of very fast pulses. A peak detector which does this is shown in Figure 2. The input signal is applied to the non-inverting input of the $\mu A710$ The output is taken from a large capacitor connected to the inverting input. If the voltage on the input terminal is greater than that on the output, the comparator output will swing positive and rapidly charge the capacitor through D_1. When the input voltage drops below the voltage on the capacitor, the output of the $\mu A710$ swings negative

and the diode becomes reverse-biased, leaving the capacitor charged to the peak value of the input signal.
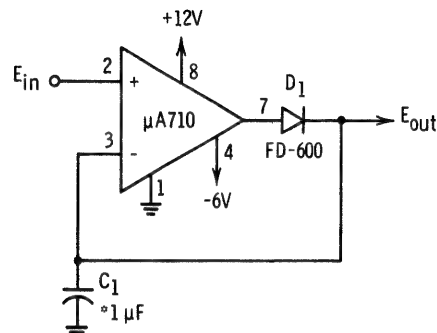
*Tantalum Slug Capacitor (Sprague Type 150D)

Fig. 2 Positive Peak Detector for Fast Pulses.

Because of the low offset and fast response time of the $\mu A710$, the circuit can measure the amplitude of pulses less than $100ns$ wide with an accuracy of 5 mV. The operating range of the circuit, which is determined by the available output swing of the comparator, is 0 to $+2.5V$. The decay time of the voltage developed across the capacitor is determined by the input bias current of the $\mu A710$ (approximately 20 ms/V). If it is desired that the peak detector follow more rapidly varying signals, a resistor can be inserted between the output and the negative supply voltage. The peak detector loads the signal source very little. The maximum current drawn from the source is approximately 25 μA, and this only occurs at the peak of the input signal.

The circuit functions as a unity-gain feedback amplifier at the peak of the input signal, with C_1 providing frequency compensation. Hence, C_1 cannot be made much smaller than the $1\mu F$ indicated, or the circuit will oscillate at the peak of the input signal, giving erratic operation. However, larger values of capacitance can be used.

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A circuit that will operate with negative-going input signals is shown in Figure 3. A μA702A is used, and the output voltage will be positive and equal to the negative peak value of the input waveform.

circuit: if it is not driven from a low impedance source, internal frequency compensation is required to prevent oscillations.
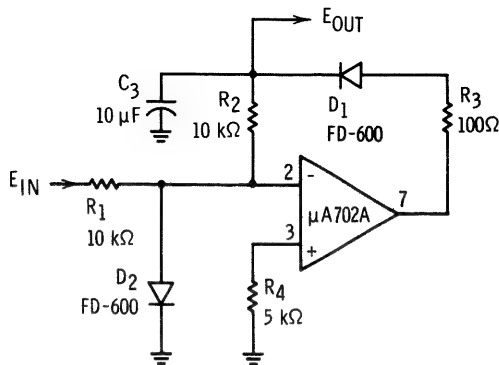
Fig. 3 Peak Detector Using μA702A.

Fig. 5 Peak-To-Peak Detector.

CLAMPER

Another diode circuit is illustrated in Figure 4. This is a precision clamper. It gives an inverted, positive-going output signal that is clamped to the DC reference voltage supplied to the amplifier (E_{ref}).
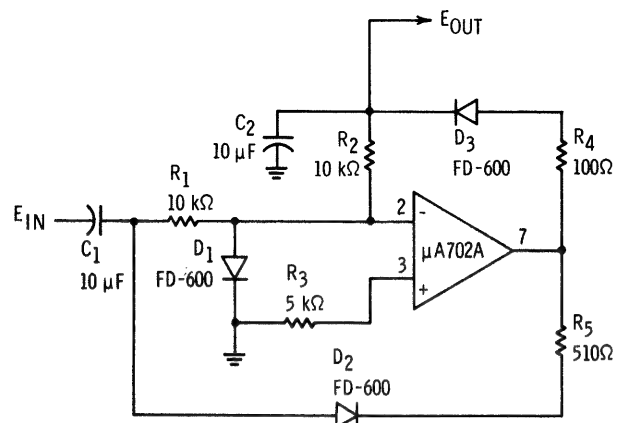
ABSOLUTE VALUE AMPLIFIER

An absolute value amplifier, or full-wave rectifier, using a pair of μA702A's is shown in Figure 6. The output is equal to the amplified positive absolute value of the input signal.

Fig. 4 Clamper.

PEAK-TO-PEAK DETECTOR

The circuit in Figure 5 is another example of the use of diodes with operational amplifiers. The output of the circuit is a positive DC voltage proportional to the peak-to-peak value of the input waveform. One precaution is necessary with this
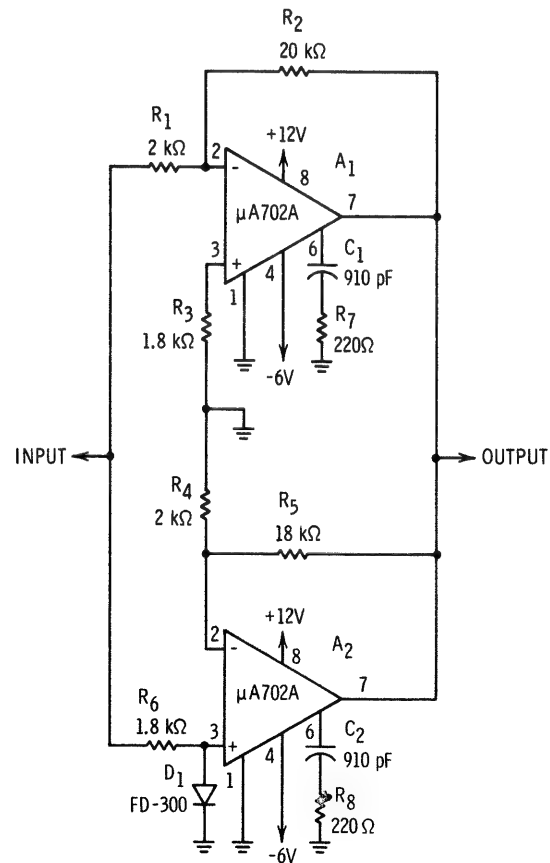
Fig. 6 Absolute Value Amplifier.

The input signal is applied to the two amplifiers connected in parallel. Amplifier A_1 provides an inverting gain of 10 and A_2 gives a non-inverting gain of 10. The output of A_2 will thus be positive for positive values of input signal, and the output of A_1 will be positive for negative inputs. Since the output stage of the μA702A is an emitter-follower, the output of the circuit of Figure 6 must follow whichever amplifier swings positive, thereby achieving the absolute value function. The $C_1 - R_7$, $C_2 - R_8$ networks provide frequency compensation for the amplifiers, and D_1 protects the input of A_2.

This connection cannot be used with the μA709, however, because its complementary output stage has equal sink and source current capabilities.

An alternate circuit which also uses two μA702A's, is shown in Figure 7. The first amplifier acts as a unity-gain, half-wave rectifier, giving negative output for positive input signals. The output, along with the original input signal, is fed into the second amplifier, which sums them together. Because of the ratios R_8/R_2 and R_8/R_5, the amplifier operates with unity gain to the original signal, and X2 for the negative half-wave output signal. The net effect is that the output is always positive-going and equal to the absolute value of the input.

LOGARITHMIC AMPLIFIER

The bipolar transistor is probably the most predictable nonlinear element known to physics; using the expression given in Eq. (22) of Chapter 2, the emitter-base voltage differential between two matched transistors operating at different collector currents is

$$\Delta V_{BE} = \frac{kT}{q} \, ln \left(\frac{I_{C1}}{I_{C2}}\right) \qquad (1)$$

In the circuit of Figure 8, a transistor (Q_1) is used as the feedback element around a μA709 operational amplifier. The negative feedback forces the collector current of Q_1 to be equal to the current into the summing node of the amplifier. Hence, we can write

$$I_{C1} = \frac{E_{IN}}{R_1} \qquad (2)$$

The collector current of Q_2 is determined by the positive supply voltage and R_6 as

$$I_{C2} = \frac{V^+}{R_6} \qquad (3)$$
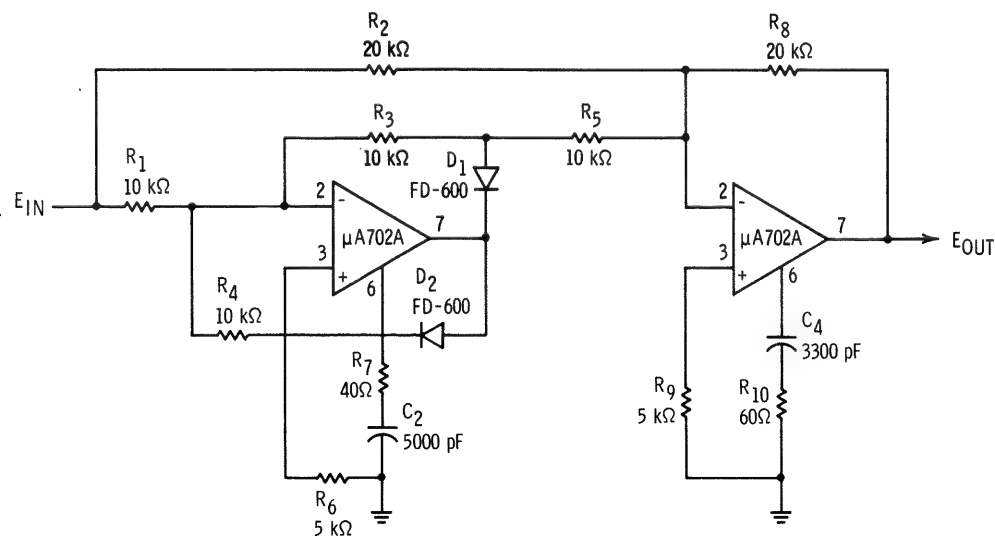
Fig. 7 Full-Wave Rectifier.
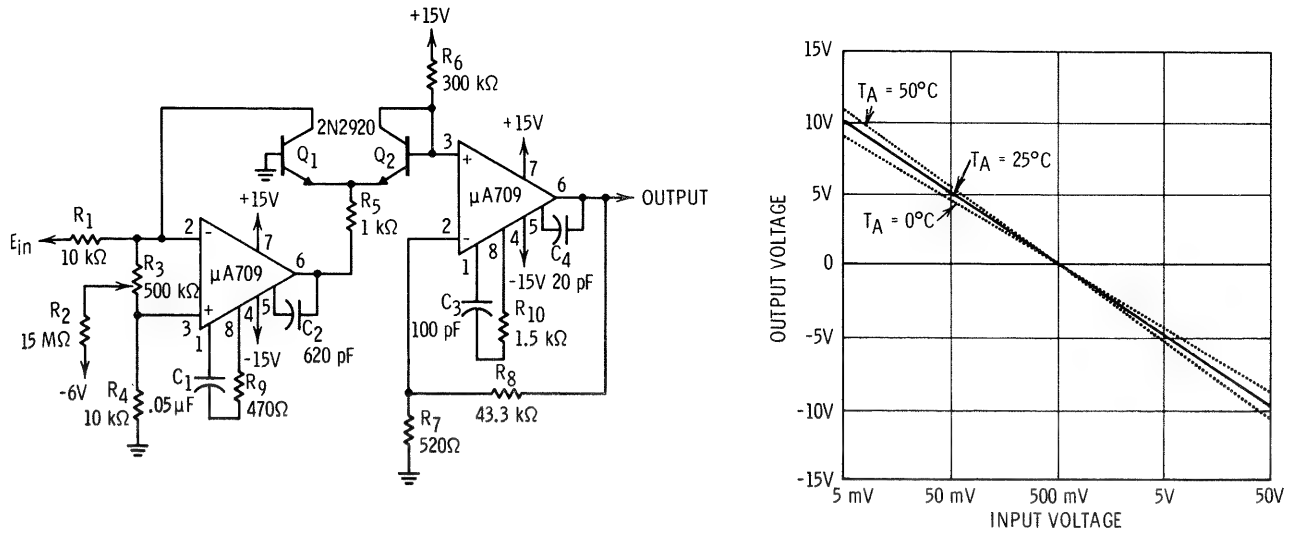
Fig. 8 Logarithmic Amplifier.

If Q_1 and Q_2 are a matched pair of transistors, Eq. (1) can be used to give

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{R_6 E_{IN}}{R_1 V^+} \right) \qquad (4)$$

Since the base of Q_1 is grounded, the negative of this voltage is presented to the input of the second amplifier. The gain of this stage is

$$A_V = \frac{R_7 + R_8}{R_7}$$

so

$$E_{OUT} = - \frac{kT(R_7 + R_8)}{qR_7} \ln \left(\frac{R_6 E_{IN}}{R_1 V^+} \right) \qquad (5)$$

which shows that the output voltage is proportional to the logarithm of the input voltage. It can be seen from Eq. (5) that the coefficient of the log term is proportional to absolute temperature, which gives it a thermal sensitivity of 0.3%/°C. The over-all transfer function of the amplifier is given for various operating temperatures in Figure 8. As shown, the amplifier has a dynamic range of 80 dB.

Additional details of the circuit in Figure 8 are that R_2 and R_3 are used to provide an offset adjustment that increases the dynamic range for small input signals. R_5 is used to limit the loop gain of the input amplifier so that it can be frequency compensated. To minimize the effect of the input bias current of the output amplifier, R_7 is chosen to be equal to the diode impedance of Q_2. The slope of the log characteristic is determined by R_8, while R_6 determines the zero crossing.

The temperature-dependent term in Eq. (6) can be eliminated by using a μA726 as the logarithmic element. This is shown in Figure 9; the first μA726, A_1, extends the lower end of the dynamic range of the amplifier, and the second μA726 holds the kT/q scale factor to $\pm 1\%$ over the $-55°C$ to $+125°C$ temperature range.

MULTIPLIER

Another interesting use for the nonlinear properties of the bipolar transistor is the multiplier shown in Figure 10. The basic multiplying element is the transistor pair, Q_1 and Q_2. Its operation can be understood from the following:

The small-signal transconductance of a transistor can be obtained by differentiation of Eq. (8) of Chapter 2:

$$\frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT} \qquad (6)$$

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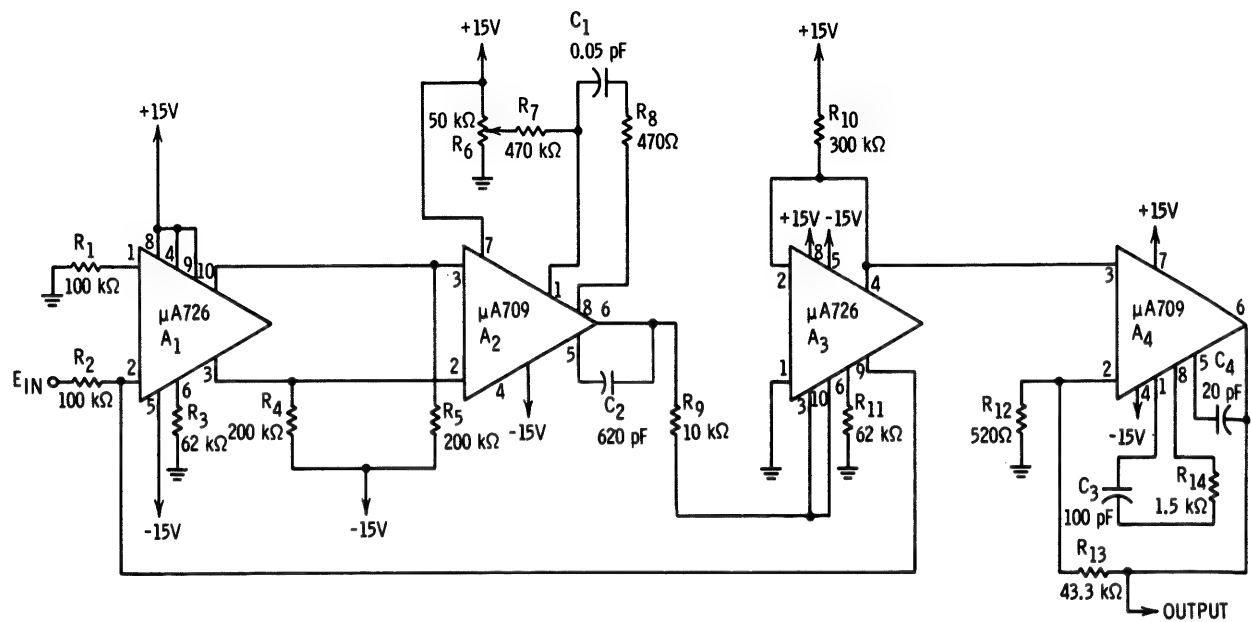
Fig. 9 Logarithmic Amplifier with Temperature Stabilization.
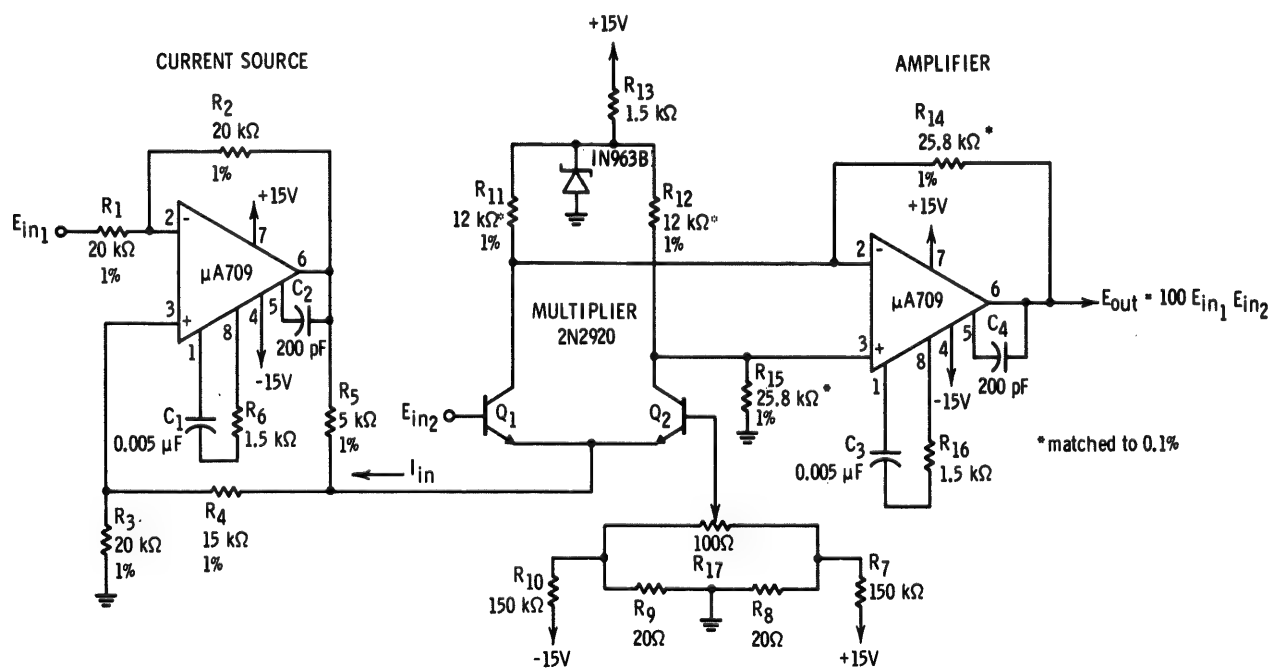
Fig. 10 Multiplier.

A matched transistor pair in a differential config-uration, as shown in Figure 10, will now be con-sidered. For zero differential input voltage, the input current supplied to the emitters will split equally between the two transistors, and the dif-ferential output current will be zero. Hence, Eq. (6) can be rewritten in terms of the differential out-put current, the input current to the emitters, and the input voltage as

$$I_{OUT} = \frac{q}{2kT} I_{IN} E_{IN2} \tag{7}$$

Hence, the differential output current is pro-portional to the product of the differential input voltage and the current supplied to the emitters of Q_1 and Q_2. Using standard operational amplifier theory, this current can be shown to be

$$I_{IN} = \frac{E_{IN1} R_2}{R_5 R_1} \tag{8}$$

A second input voltage is supplied to the dif-ferential pair. Combining Eqs. (7) and (8) and setting $R_1 = R_2$, the output current of the dif-ferential pair is

$$I_{OUT} = \frac{q}{2kTR_5} E_{IN1} E_{IN2} \tag{9}$$

The output of the pair is connected to a second μA709 that converts the differential current to a single-ended, zero-referred voltage. The output voltage of this amplifier will be $E_{OUT} = R_{14}I_{OUT}$, for $R_{14} = R_{15}$ and $R_{11} = R_{12}$. Hence

$$E_{OUT} = \frac{qR_{14}}{2kTR_5} E_{IN1} E_{IN2} \tag{10}$$

which shows that the output voltage is proportional to the product of the two input voltages.

There are several hints that are pertinent to making the circuit work correctly. One is that the resistor pairs $R_{11} - R_{12}$ and $R_{14} - R_{15}$ must be very closely matched (within 0.1%). An adjustment is provided for nulling the offset of Q_1 and Q_2. This adjustment should be made when the current-source current is at its maximum value. It should also be noted that Eq. (7) is a small-signal approx-imation, so the voltage input to the differential pair should be kept small. Restricting the input

voltage to $\pm 20 mV$ gives linearity that is acceptable for the majority of applications. It should also be pointed out that E_{IN2} can be a bipolar signal while E_{IN1} must be a positive voltage.

HARMONIC MIXER

The small-signal forward admittance of the μA703 with a time-varying input signal is given by

$$y_{21}(t) = -\frac{q}{kT} \frac{I_{C5}}{2} \left[\frac{1}{1 + cosh\dfrac{qV_{in}(t)}{kT}} \right] \tag{11}$$

where $V_{in}(t) = V_{lo} Cos \omega_{lo}t + V_s cos \omega_s t$
V_{lo} = local oscillator voltage
ω_{lo} = local oscillator frequency
V_s = signal voltage
ω_s = signal frequency

For a harmonic mixer, the amplitude of the signal must be less than the local oscillator so that trans-admittance modulation of the μA703 is accom-plished essentially by V_{lo}.

Since the *cosh* function of Eq. (11) is an even function, only components which are even mul-tiples of the local oscillator frequency will be pres-ent in the output of the μA703. The graphical solution of Eq. (11) is shown in Figure 11 for the
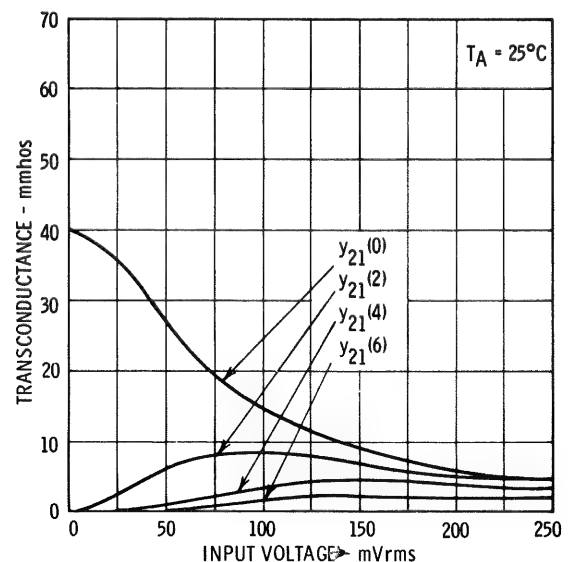
Fig. 11 Forward Transconductance of Emitter-Coupled Pair for Even-Order Harmonics.

first three harmonics. A general algebraic solution is not attempted here since it would provide little more than exercise. It can be seen from the figure that the large local oscillator drive generates components of the forward transadmittance which are even functions only. This "harmonic mixing" is more useful than a conventional mixer because of the lower frequencies and reduced filtering required. It would be much easier to design a 50 MHz oscillator than a 100 MHz oscillator for use as a local oscillator, for example. One possible configuration for the mixer is shown in Figure 12.
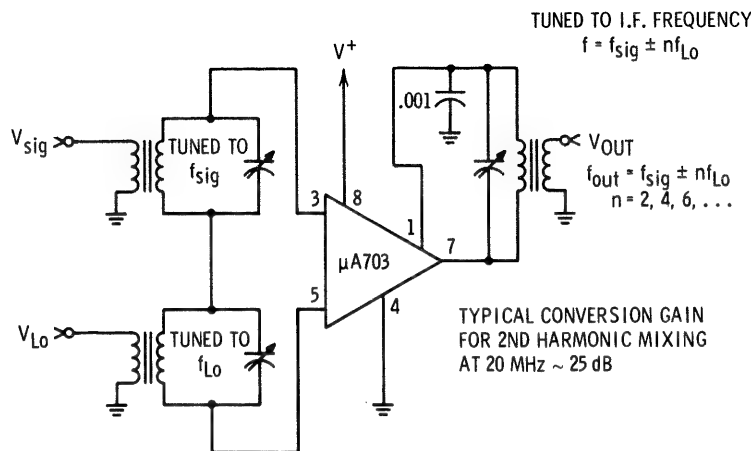
Fig. 12 μA703 Mixer Connection.

SECTION E   SPECIAL FUNCTIONS

TRANSFORMERLESS MODULATOR-DEMODULATOR*

The need for a modulator or demodulator frequently arises in the design of control or communication systems. In the past, matched diode bridges have been used in conjunction with transformers to perform this function. The approach has the disadvantage that the transformers operate over a relatively limited frequency range, usually require special designs, are bulky, and are expensive in small quantities.

The circuit described uses the μA702A as a full-wave modulator-demodulator that requires no transformers and uses only standard, readily-available parts. It will operate over a wide range of frequencies and is easily adapted to different applications.

Figure 1 is a schematic diagram of the circuit. Input switch Q_1 alternately switches the μA702A from an inverting amplifier configuration (with Q_{1A} on) to a non-inverting connection (with Q_{1B} on). The inverting and non-inverting gains are equal

for $R_1 = R_2$, $R_3 = R_4$ and

$$R_6 = \frac{(R_1 + R_3)\, R_3 R_5}{(R_1 + R_3)\,(R_3 + R_5) - R_3 R_5} \qquad (1)$$

where the voltage gain is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_5}{R_1 + R_3} \qquad (2)$$
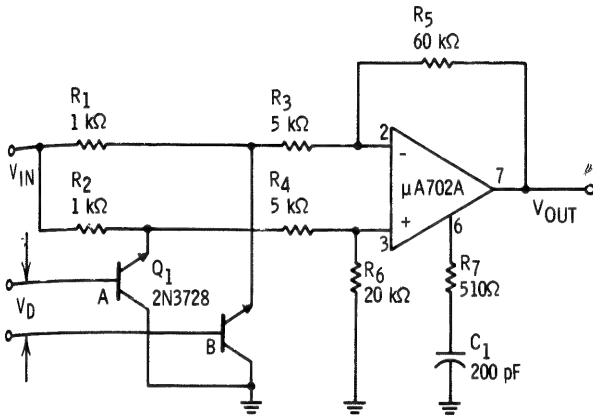
Fig. 1 Schematic of the Transformerless Modulator-Demodulator.

For modulator operation, the input voltage (V_{IN}) is a DC signal and the output is a square wave with magnitude proportional to V_{IN} and either in phase or out of phase with the drive voltage (V_D), depending on the algebraic sign of V_{IN}.

For demodulator operation, V_{IN} is an AC voltage. With a sinusoidal input, the average value of V_{OUT} varies as the cosine of the phase difference between V_D and V_{IN}. With a square-wave input, the average value of V_{OUT} is a linear function of the phase difference of V_{IN} and V_D. To minimize offset in the circuit of Figure 1, the switch transistors are operated in an inverted configuration. The push-pull drive signal can be readily obtained from an integrated circuit flip-flop. The circuit values give a gain of 10 and a 10 MHz bandwidth. Additional advantages of using the μA702A are that a substantial gain can be provided, and the output impedance is quite low and constant throughout the switching cycle, which simplifies output filtering.

PHASE DETECTOR

Figure 2 shows a circuit developed as a $400Hz$ transformerless phase detector. The first μA702A is used without feedback to produce switching pulses to the base of Q_1. The network R_1C_2 produces a phase lag of 90° with respect to the input reference signal V_{ref}. The second μA702A acts as a differential amplifier into which V_{ref} and V_{IN} are fed. Its output voltage will, in general, swing about zero potential. The output (V_{OUT}) is the integral of the voltage present at the amplifier output during the period of each cycle for which Q_1 is switched on.
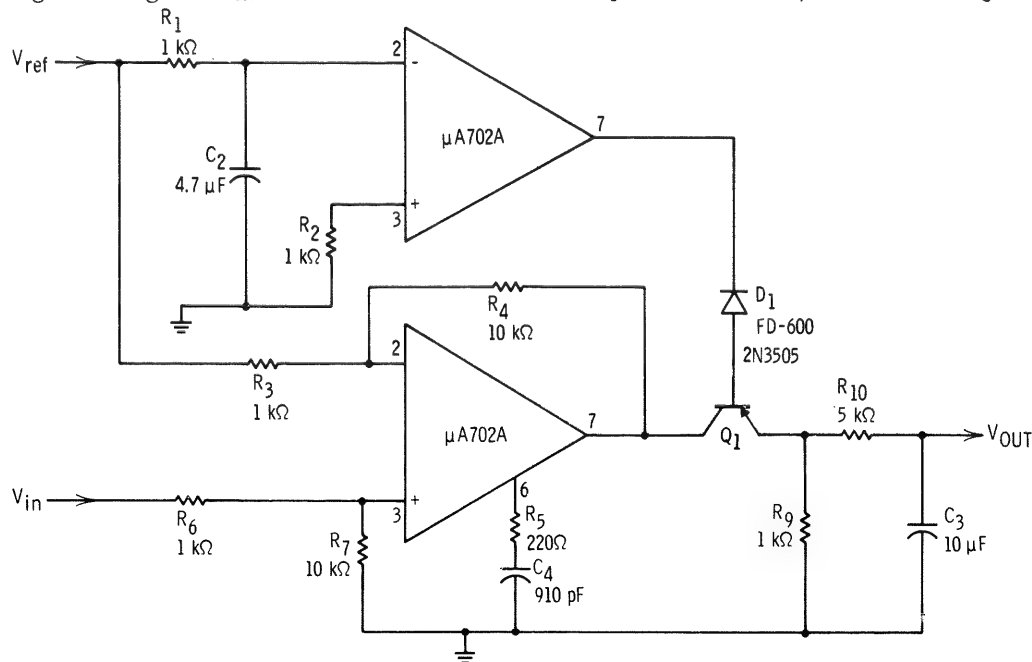
Fig. 2 400 Hz Phase Detector.

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Even when V_{IN} and V_{ref} are in phase, they will not necessarily be of the same amplitude. The difference in amplitude will result in a sine wave output at the amplifier output. Since, however, the switching pulse has been displaced in phase by $-90°$, the output integrates to zero, having swung symmetrically about zero during the "on" period. If V_{IN} is not in phase with V_{ref}, the amplifier output will not be symmetrical about zero for the "on" period, and there will be a resultant output, V_{OUT}, which will be negative if V_{IN} leads V_{ref} and positive if it lags.

When the amplifier output is negative, Q_1 acts as an emitter-follower with R_9 as the emitter load. Where it is positive, the emitter and collector are reversed in role such that R_9 becomes the collector load. There is, however, adequate base current drive to saturate the switch in this configuration, though there is some loss in output voltage symmetry. D_1 is used to block the positive-going output from the first $\mu A702A$ and to protect Q_1 from excessive reverse voltage. In order to provide approximately 90° phase shift, $X_{C2} < R_1/10$, and to provide approximate integration of the output waveform, $C_3 R_{10} > 10t$, where $t = 1/f$ and $R_L > R_{10}$.

Although the output is relatively independent of the ratio in amplitude between V_{ref} and V_{IN}, optimum results will be obtained if these amplitudes are matched to within 10%. In any case, care must be taken to avoid exceeding the common mode operating range of both amplifiers by limiting the input to a maximum of $1V_{pp}$. Greater sensitivity may be obtained by increasing the gain of the differential amplifier but it is important to avoid nonlinear operation caused by a combination of input error signals, or the discrimination will be upset.

MAKING A NYQUIST PLOT UNDER CLOSED-LOOP CONDITIONS*

In any closed-loop feedback system, it is desirable to measure the open-loop response. There are certain classes of closed-loop systems, however, which cannot be operated under open-loop conditions; therefore, the response must be measured while the loop is closed.

A Nyquist plot can be made by using the technique shown in Figure 3. A disturbance, V_0 is added to the feedback path such that $V_0 + V_2 = V_1$, where V_2 is the amplifier output voltage and V_1 is the input voltage. Normalizing with respect to V_1

$$\frac{V_0}{V_1} + \frac{V_2}{V_1} = 1, \qquad (3)$$

reveals that the second term is the open-loop gain of the system and the first term is the return difference. Since these two quantities are vectors, they may be used to plot the open-loop gain and phase of the system.
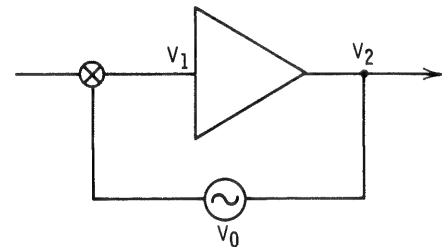
Fig. 3 Diagram Showing Insertion of Disturbance into Closed-Servo Loop.

The main disadvantage of this procedure is the difficulty in inserting V_0 into the feedback loop. By using a pair of $\mu A702A$ operational amplifiers as shown in Figure 4, the measurement can be readily
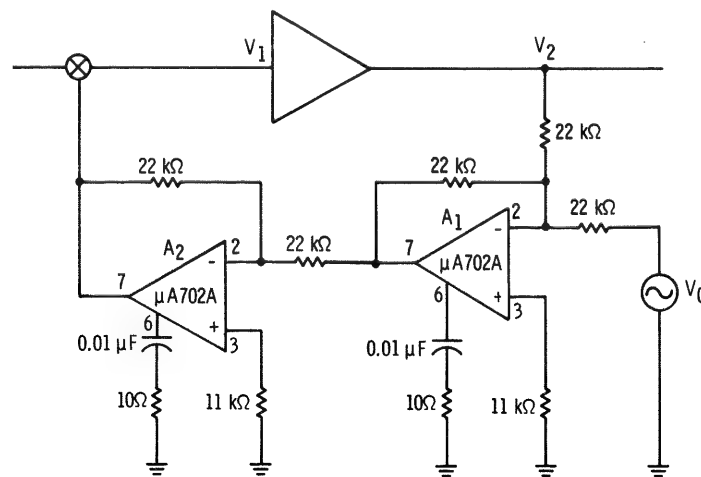
Fig. 4 Circuit for Introducing Disturbance from Single-Ended Source.

made while still having one side of V_O grounded. Amplifier A_1 operates as a unity-gain summing amplifier, and A_2 functions as an inverter. The circuit is compact and reliable, and permits utilization of a measurement technique heretofore difficult to implement.

P.P.I. SWEEP GENERATOR*

Two μA702A operational amplifiers may be used to generate the waveforms required for a radial plan position indicator display. High linearity, uniform bilateral integration, rapid reset time, and an output that directly powers a deflection driver are some of the advantages obtained. In addition, the entire circuit is easily encapsulated in a small package instead of the several circuit boards required using conventional components.

The amplifiers in Figure 5 are connected as two independent integrators, diode-clamped to zero until a range gate pulse arrives and allows the sweep waveform to begin. The input to each integrator is derived from the antenna or servo position as the sine and cosine output of a synchro resolver. The value of the sine or cosine of the input determines the rate at which the integrators reach the

end of the range gate; the polarity of the input determines whether the integrators sweep positive or negative, thus giving four quadrant integration.

The amplifier outputs appear on the display as a series of radial sweeps. The time constants shown in Figure 5 give several thousand radial sweeps for an antenna circular rate of about 40 *rpm*. The display is unblanked only during the sweep times.

MULTIVIBRATORS

It is possible to use the μA710 as a one-shot multivibrator with the circuit shown in Figure 6. It has the particular advantage that the trigger point can be determined within $\pm 10mV$ over a $\pm 5V$ range. The trigger level of the one-shot is equal to the externally set threshold voltage (V_{ref}). The duration of the output pulse is given by

$$t = (R_2 + R_3) \ C_1 \ ln \left[\frac{\Delta V_0 R_2}{V_{ref} (R_2 + R_3)} \right] \qquad (4)$$

where ΔV_0 is the total output swing.
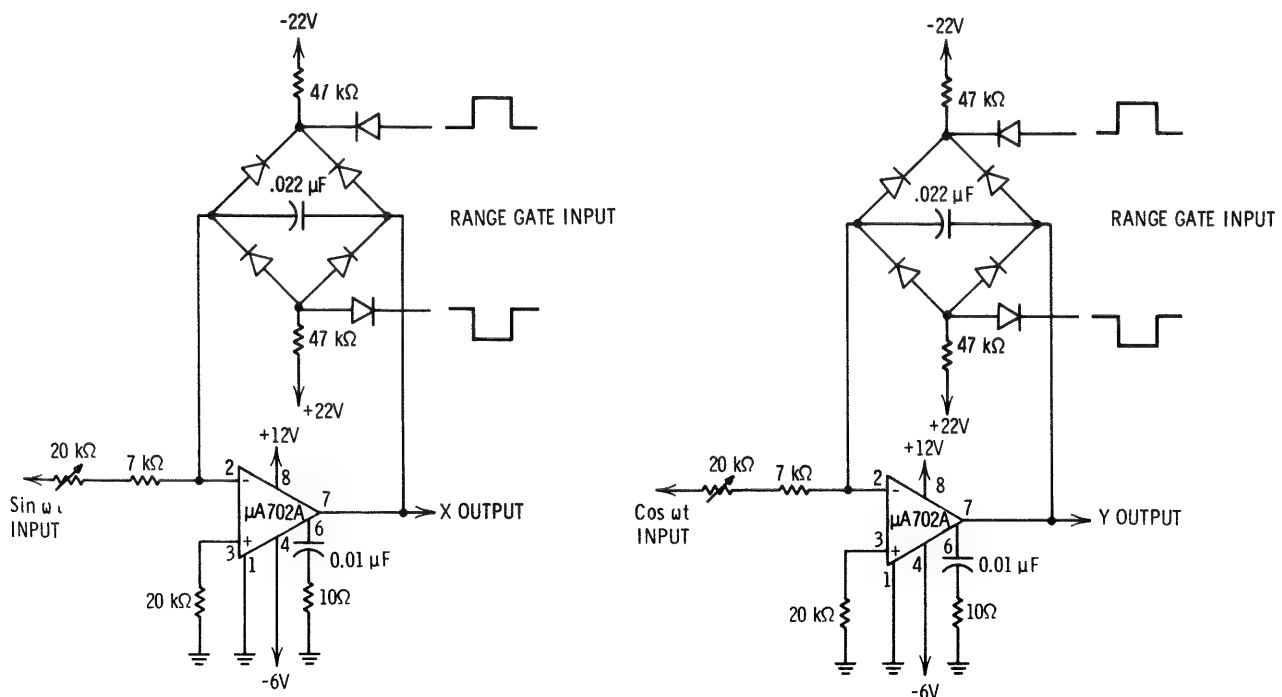
Fig. 5 P.P.I. Sweep Generator.

*Submitted by Donald E. Lancaster of Goodyear Aerospace, Phoenix, Arizona

The circuit in Figure 6 gives a positive output pulse for a negative trigger with $V_{ref} < O$. For $V_{ref} > O$, a negative output pulse for a positive trigger is realized. Positive outputs for positive trigger and negative outputs for negative trigger can also be obtained by connecting the input differentiating capacitor to the non-inverting input. However, the interaction between the trigger and feedback circuitry must be taken into account.
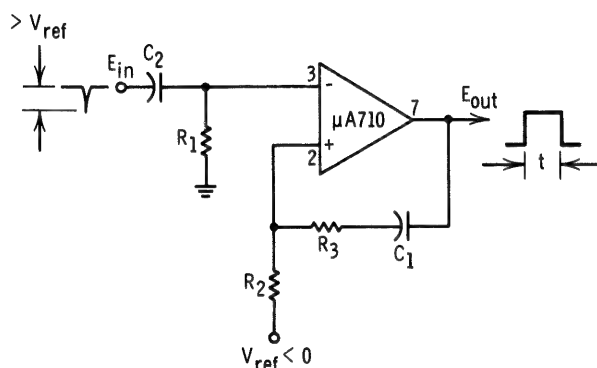
Fig. 6 One-Shot Multivibrator.

A free-running multivibrator using the μA710 is illustrated in Figure 7. A large amount of DC negative feedback, along with a resistor connected to the negative supply, is used to set the output of the μA710 in the center of its active region to ensure starting and reasonable symmetry in the output waveform. The capacitor reduces the negative feedback at high frequencies, giving net positive feedback and oscillation.
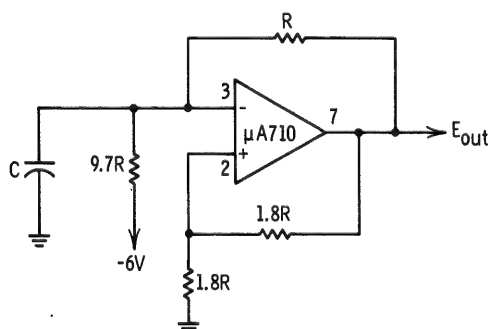
Fig. 7 Free-Running Multivibrator.

The relative resistance values for the multivibrator are computed to give a DC output voltage in the center of the active region of the μA710, assuming that C is removed and the comparator is treated as an operational amplifier. With the relative values given in Figure 7, the period of oscillation is

$$T = 1.8RC\ ln\left[\frac{-\Delta V_0}{0.1V^- + 0.45V_{0(min)}}\right] \quad (5)$$

where the sign of V^- and $V_{0(min)}$ must be observed. Using typical values, Eq. (5) becomes

$$T = 2.7\,RC$$

There are certain restrictions on the range of R in Figure 7. If R is made smaller than about 1$k\Omega$, the output sink current of the μA710 may not be large enough to swing the output all the way negative. On the other hand, if R is made larger than about 24 $k\Omega$, the input offset current could seriously degrade the symmetry of the output waveform and lead to start-up problems.

Because of the fast response of the μA710, the multivibrator circuit can be operated to quite high frequencies. It has been used successfully to frequencies as high as 5 MHz. At high frequencies, performance can be improved somewhat by connecting a small capacitor between the output and the non-inverting input.

SINE WAVE OSCILLATOR

The schematic of a phase-shift oscillator using the μA702A wideband DC amplifier is shown in Figure 8. Negative feedback is applied to the inverting input of the amplifier through R_3 to stabilize the gain and make it essentially independent of the integrated circuit characteristics. The R-C network (R_1, C_1, R_2, and C_2) applies positive feedback to the non-inverting input. As long as this is equal to or greater than the negative feedback, the circuit will oscillate at the frequency where the phase shift through the R-C network is zero. It is desirable to maintain the positive feedback exactly equal to the negative feedback: if the
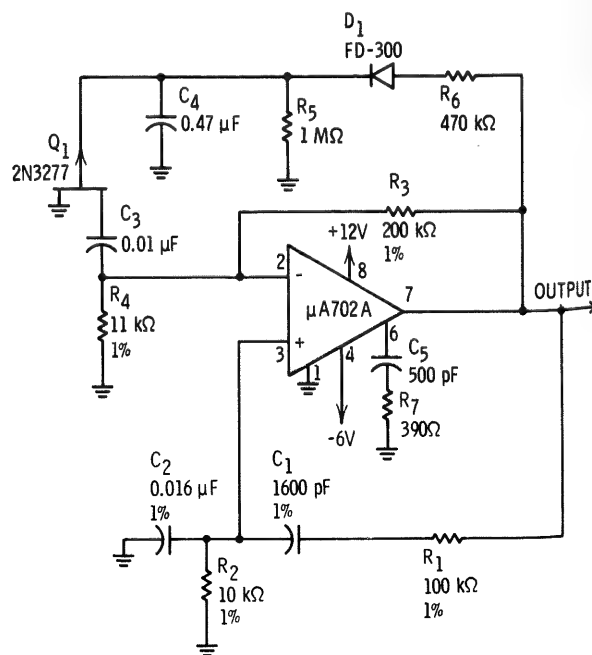
Fig. 8 1 kHz Sine-Wave Oscillator.

positive feedback is greater, the output of the oscillator will build up until it becomes nonlinear, thereby distorting the output sine wave. The positive and negative feedback cannot be made equal with a simple adjustment, since any small component change will either cause the circuit to stop oscillating or to distort. This difficulty is overcome using an AGC circuit which holds the gain at the precise value required to sustain oscillation at the desired output level.

If $R_1C_1 = R_2C_2$, the frequency where the phase shift through the R-C network is zero (and therefore the frequency of oscillation) is given by

$$f = \frac{1}{2\pi R_1 C_1} \tag{7}$$

The attenuation through the network at this frequency is

$$\eta = \frac{1}{1 + 2\frac{R_1}{R_2}} \tag{8}$$

The amplifier gain must make up for this loss for oscillation to be possible. For $R_1 = 10R_2$ the amplifier gain must be exactly 21. A large ratio of R_1 to R_2 is chosen to keep the signal level across the gain-regulating FET low enough to avoid distortion.

The output of the amplifier is rectified by D_1 and filtered by C_4. This voltage, which varies as the AC output of the amplifier, is fed to the gate of the FET, and controls its drain-to-source resistance to hold the output of the amplifier at a constant level. The filter capacitor, C_4, must be large enough to stabilize the AGC loop. The value of C_3 is also important for the AGC stability. To change the frequency of oscillation, C_1, C_2, C_3, and C_4 should all be changed in proportion. The AC output level is determined by the ratio R_5/R_6, and the characteristics of the FET.

With the component values shown, the frequency of oscillation is 1 kHz and the peak-to-peak output voltage is about 8V. The stabilization time from initial turn-on is approximately 50 ms.

CRYSTAL-CONTROLLED DIGITAL CLOCK

The circuit of a crystal-controlled oscillator using the μA710 comparator is shown in Figure 9. Positive feedback is provided from the output via the series-resonant impedance of the crystal to the non-inverting input. The advantage of using the μA710 rather than an operational amplifier is that the output swing of the device has been specifically designed for full compatibility with logic circuitry.
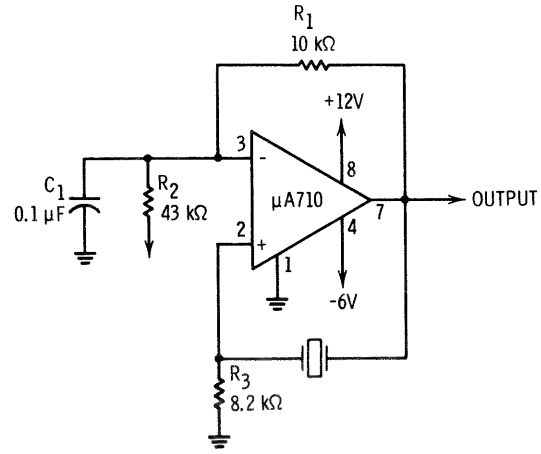
Fig. 9 Crystal Oscillator.

The DC operating point is biased by R_1 and R_2 so that oscillation takes place about the linear region of the output dynamic range, thereby ensuring self-starting under all conditions. The negative feedback is removed at the frequency of oscillation by C_1, which should be chosen such that

$$X_c < \frac{R_1}{1000}. \tag{9}$$

Resistor R_3, in addition to providing the load across which the positive feedback voltage is developed, also helps to stabilize the operating point with respect to temperature variations, and should be equal to the parallel resistance of R_1 and R_2. The value of R_2 is found from

$$R_2 = R_1 \left(\frac{V^-}{-\Delta V_0}\right) \tag{10}$$

With a suitable choice of component values, satisfactory operation up to 5 MHz may be obtained.

QUADRATURE OSCILLATOR

Two sinusoidal signals in quadrature are generated by the circuit of Figure 10, which consists of two cascaded μA709 integrators with regenerative feedback. The output of the first integrator is a sine wave and that of the second is a cosine wave. The condition for oscillation is

$$-\frac{1 + pC_2R_2}{p^2C_2R_2C_3R_3(1 + pC_1R_1)} \geq 1 \tag{11}$$

Thus, for $R_1C_1 = R_2C_2$, the circuit will oscillate at a frequency given by

$$f = \frac{1}{2\pi \sqrt{C_2 R_2 C_3 R_3}} \tag{12}$$

The circuit of Figure 10 is designed for a $1\,kHz$ operating frequency; to ensure sufficient positive feedback for oscillation, R_1 is slightly larger than R_2. Zener diodes D_1 and D_2 limit the amplitude of the output signal without significantly affecting the waveform of the cosine. Because of the filtering the signal received from the $R_1 C_1$, $R_2 C_2$ networks, the sine output will be nearly distortionless. Measured distortion at both outputs is less than 1% at a $15V$ peak-to-peak output level.

Both frequency and output amplitude are stable within 0.5% for power supply variations from $\pm 10V$ to $\pm 15V$. Frequency stability with temperature depends primarily upon the quality of the components used in the phase-shifting networks, and amplitude stability upon the temperature-coefficient of the zeners in the limiter.

10MHz OSCILLATOR

The design of transistor oscillators is complicated by the loading of the tank circuit caused by the decrease in input impedance under large-signal conditions. The usual solution is to provide some sort of impedance isolation between input and output, such as high turns ratio transformers or emitter-followers in the feedback loop.

The input impedance of the $\mu A703$, however, tends to increase with large-signal inputs. This simplifies the oscillator design because the effect of input parameter variations can be neglected (this depends upon the input voltage swing, becoming more valid for larger signals, but is usually permissible for effective loads of $2k\Omega$ or less).

Predictable oscillator performance can be obtained by utilizing the Barkhausen criterion for oscillations, which states that the necessary and sufficient condition for oscillations to occur is:

$$1 - GH = 0 \tag{13}$$

where GH is the loop gain of the system; G is the forward transfer function, and H is the reverse (feedback) transfer function.

Assuming that the input admittance is small compared to the load admittance, and the oscillator frequency is less than the corner frequency of the forward transadmittance, the forward transfer function is given by

$$G = \frac{V_{OUT}}{V_{IN}}$$

$$= \frac{y_{21}}{g}\left[\frac{1}{1 - j\omega L g\left(1 - \frac{\omega^2}{\omega_0^2}\right)}\right] \tag{14}$$
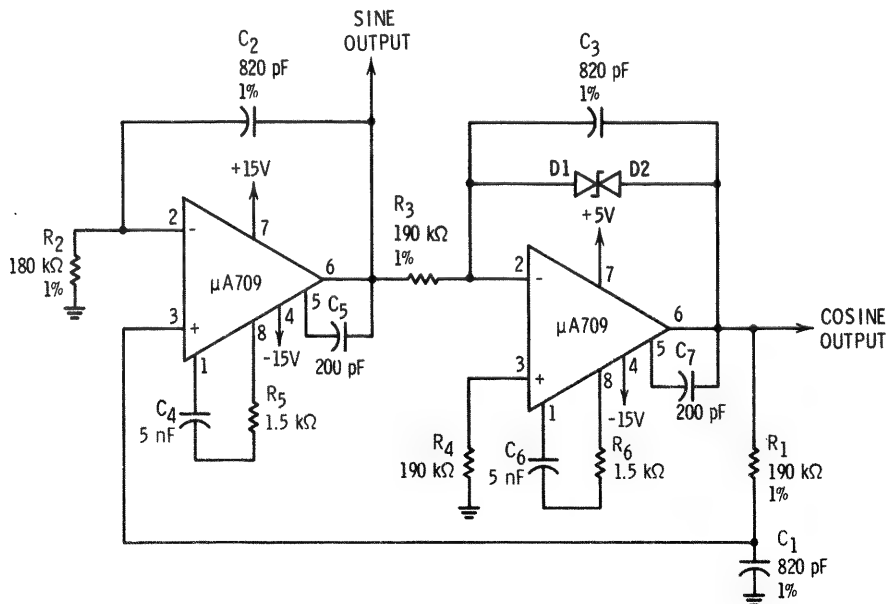
Fig. 10 Quadrature Oscillator.

where

$$\omega_0{}^2 = \frac{1}{LC}$$

C = load capacitance plus amplifier output capacitance

g = load conductance plus amplifier output conductance

Using a feedback transformer with a 1:1 turns ratio, and assuming that the coefficient of coupling is unity (which is usually justified if a toroidal core is used), the reverse transfer function, H, will be equal to one. Therefore, for oscillations to occur at $\omega = \omega_0$, the load conductance must be small enough such that

$$\frac{y_{21}}{g} \geqslant 1 \tag{15}$$

The effect of the phase shift contributed by the high frequency pole of y_{21} is to reduce the actual frequency of oscillation, but since in most tuned oscillators a trimmer is used to set the final frequency, a more exact analysis is not justified. The effect of variations in input parameters was assumed negligible in the preceding discussion; any exact analysis, however, must account for them as well as the transformer coupling coefficient and losses.

The magnitude of the output voltage can be predicted quite well if the total voltage swing at the output collector of the device is allowed to be no more than $5V_{pp}$ (for a 1:1 transformer, the maximum input voltage rating of the device will otherwise be exceeded and the emitter-base junctions may be damaged). Further, the effective collector load resistor must be small enough to ensure that current limiting occurs, but large enough that oscillations are maintained. The value of the load resistor can be determined from the expression

$$R_L = \frac{V_{pp} \, (allowed)}{max \, pp \, output \, current} \tag{16}$$

An oscillator designed using the preceding criteria is shown in Figure 11, together with the results obtained. The circuit was designed for a collector voltage swing of $2V_{pp}$, hence, from Eq. (16), an effective load resistance of 400 Ω is required, using the typical maximum output current of 5 mA. Figure 12 shows the output waveform; frequency stability as a function of power supply is shown in Figure 13.
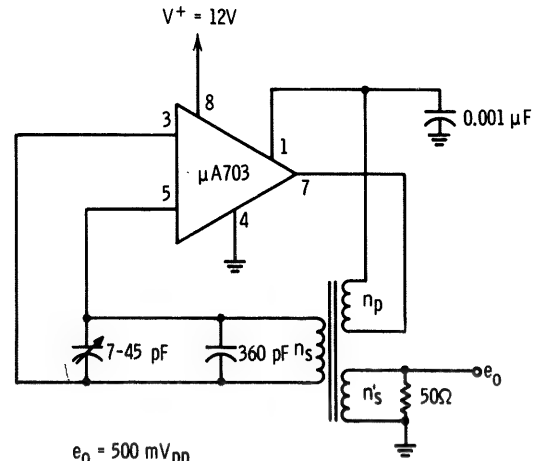
e_0 = 500 mV$_{pp}$

f_{osc} = 10 MHz

n_s = n_p = 10T #24 bifilar wound on Micro-Metals T44-10 Core

n'_s = 5T #24 wound over n_s & n_p

Fig. 11 10 MHz Oscillator.
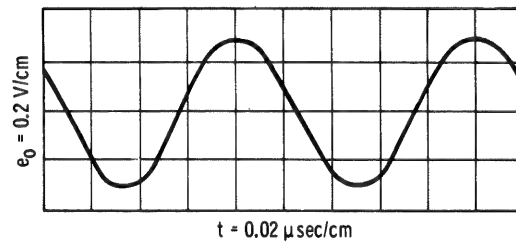
Fig. 12 Oscillator Output Waveform.
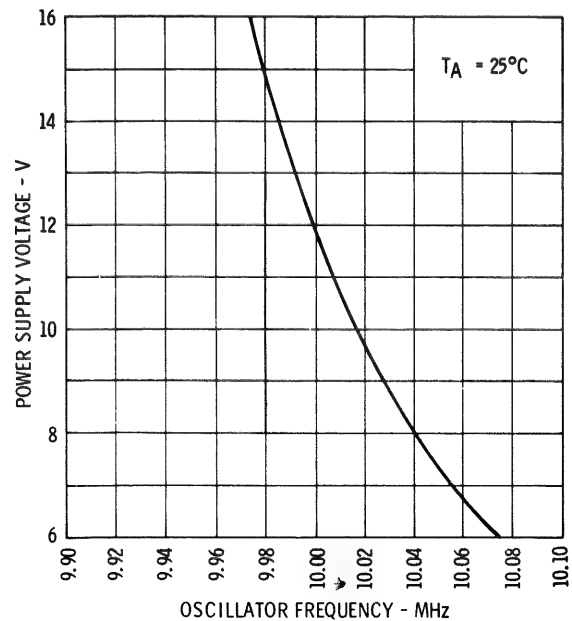
Fig. 13 Frequency Stability of 10 MHz Oscillator.

VOLTAGE-TO-FREQUENCY CONVERTER

Figure 14 shows a voltage-to-frequency converter using a pair of μA702A's. The circuit consists of an integrator, a voltage comparator and switch. The output voltage of the integrator is a negative-going ramp which falls at a rate directly proportional to the DC input signal. When the output of the integrator reaches a predetermined negative level, it is sensed by the comparator, which drives the switch to reset the integrator output to zero; the cycle is then repeated. The time required for the integrator output to go from zero to the preset level is inversely proportional to the input voltage, and so the operating frequency will be proportional to this voltage.

The μA702A is chosen for the integrator because of the fast slewing rate required during the reset interval. However, the μA702A alone does not have enough gain to make the integrator function properly over a wide dynamic range. In addition, lower input currents than are practical with the μA702A are frequently required in this application. Both these limitations are overcome by using a discrete *PNP* matched pair (Q_1 and Q_2) in front of the amplifier. This composite amplifier has a gain greater than 25,000 and input currents less than 0.5 μA. The offset voltage of the input transistors is conveniently balanced out with the potentiometer (R_6) shown in the schematic. Because of the high gain of the complete amplifier, frequency compensation

is done at two points with $R_7 - C_1$ and $R_8 - C_3$ as shown in the figure. The integrating capacitor is C_4. The clamping diodes (D_1 and D_2) prevent overloading of the comparator under abnormal operating conditions.

A second μA702A is used as a voltage comparator at the output of the integrator. A threshold voltage of $-4.0V$ is supplied to the non-inverting input of the comparator from a resistive divider (R_{10} and R_{11}). When the output of the integrator falls to $-4.0V$, the output of the comparator rises rapidly from $-5.0V$, turning on Q_3 which supplies positive feedback to the non-inverting input of the comparator. Q_3 saturates and drives approximately $11 mA$ into the summing node of the integrator; it also holds the non-inverting input of the comparator very near to ground potential. When the integrator output, which is being driven positive by the switch current, reaches zero, the comparator output swings negative and turns off Q_3. The cycle is then repeated. In Figure 14, R_{12} limits the base drive of Q_3 while C_5 and C_6 decrease the turn-on and turn-off times of the switch.

The time required for a given change in the output voltage of the integrator is given in terms of the input voltage and circuit values by

$$t = R_1 C_4 \frac{\Delta E_{OUT}}{E_{IN}} \qquad (17)$$
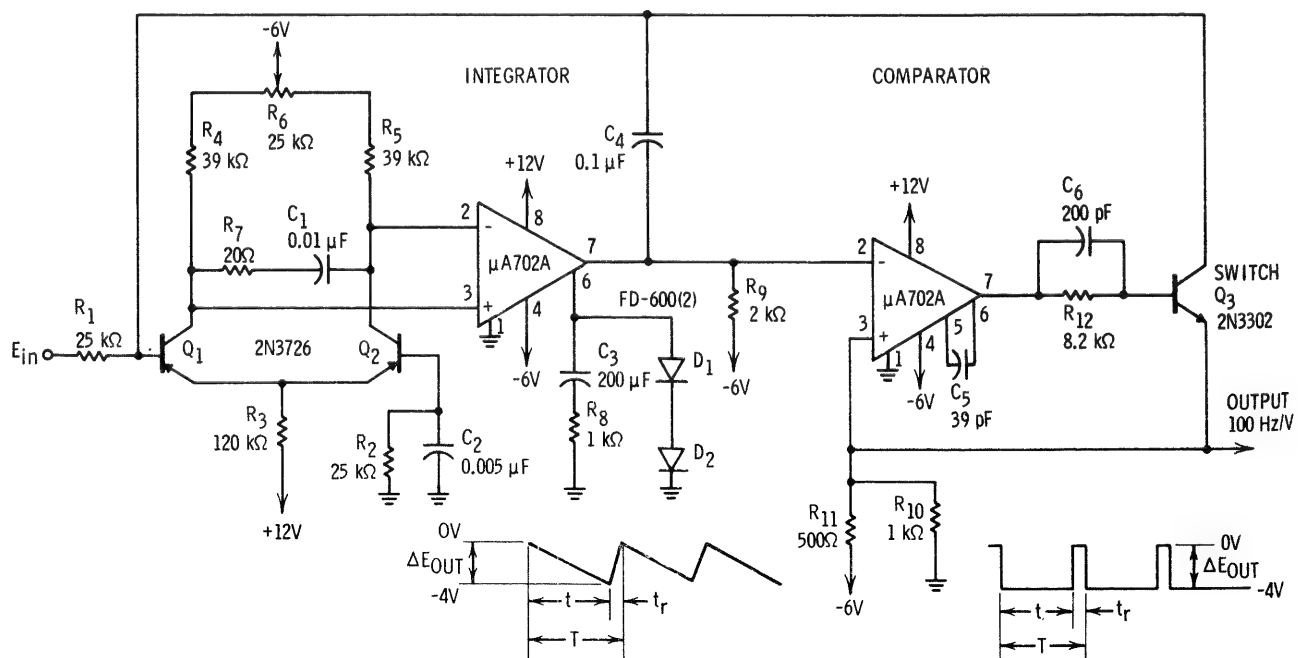
Fig. 14 Voltage-To-Frequency Converter.

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Similarly, when Q_3 is turned on, the reset time is

$$t_r = C_4 \frac{\Delta E_{OUT}}{I_{C3}} \qquad (18)$$

or

$$t_r \cong R_{11} C_4 \frac{\Delta E_{OUT}}{V^-} \qquad (19)$$

The output of the integrator swings from zero to a voltage determined by the resistive divider, R_{10} and R_{11}, so

$$\Delta E_{OUT} = \frac{R_{10} V^-}{R_{10} + R_{11}} \qquad (20)$$

Therefore, the period for one cycle of operation is

$$T = \frac{C_4 R_{10} V^-}{(R_{10} + R_{11})} \left(\frac{R_1}{E_{IN}} + \frac{R_{11}}{V^-} \right) \qquad (21)$$

Since $\frac{R_1}{E_{IN}} >> \frac{R_{11}}{V^-}$, we can write

$$f \cong \frac{(R_{10} + R_{11}) E_{IN}}{C_4 R_1 R_{10} V^-} \qquad (22)$$

This gives a conversion factor of 100 Hz/V.

PRECISION ANALOG GATE

A precision analog gate can be made with an operational amplifier and a pair of *MOS FET* switches, as shown in Figure 15. The gate is opened and closed by the push-pull drive signal to the gates of Q_1 and Q_2. With Q_1 on and Q_2 off, the circuit operates as a normal unity-gain inverting amplifier, and the gate "on" resistance is practically zero, being determined by the inaccuracy of the closed-loop amplifier. If R_1 and R_2 are matched to 0.01%, the effective closed resistance of the gate is about 0.1 Ω when driving a $1k\Omega$ load.

The gate is opened by switching Q_1 off and Q_2 on, thereby disconnecting the amplifier from the load and connecting its output to the summing junction. Almost perfect isolation is achieved between the input signal and the load since the only errors introduced are due to the small error voltage at the summing point and the leakage in Q_1.
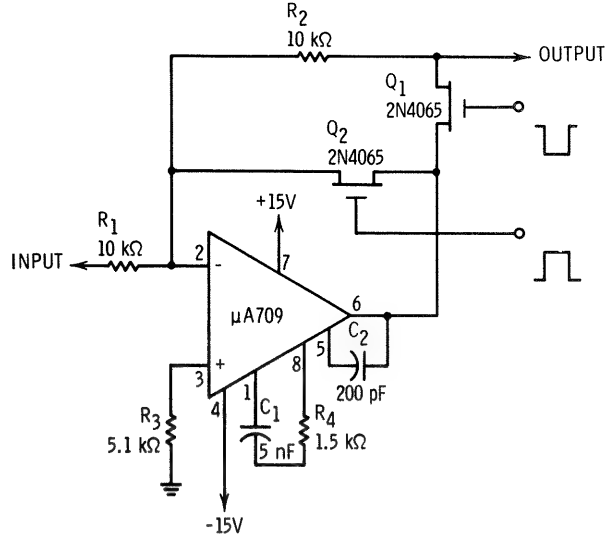
Fig. 15 Precision Analog Gate.

PULSE-WIDTH MODULATOR

A pulse-width modulator develops a train of pulses that have widths proportional to the amplitude of the modulating signal. In the circuit of Figure 16 (a), a 4 V_{pp} square-wave carrier is applied to the input of a μA702A integrator, which converts it into a linear triangular wave. Frequency compensation is provided by $R_4 - C_3$, and R_3 provides DC feedback to maintain the output symmetrical about ground.

The triangular output of the integrator is applied to one input of a μA710 comparator and the modulating signal to the other input. The comparator switches states when the amplitude of the modulating signal equals the amplitude of the triangular signal, as illustrated in Figure 16 (b). The over-all linearity of the pulse-width-modulated signal is a function of the linearity of the triangular reference and the offset of the comparator, and the maximum percentage of modulation is limited by the response time of the comparator. The circuit values given in the schematic are for operation at a carrier frequency of 100 kHz, where extremely linear modulation up to 99% can be obtained, as shown by the curve of Figure 17. With suitable scaling of element values, the circuit will operate at 1 MHz, with a maximum modulation of 92%.
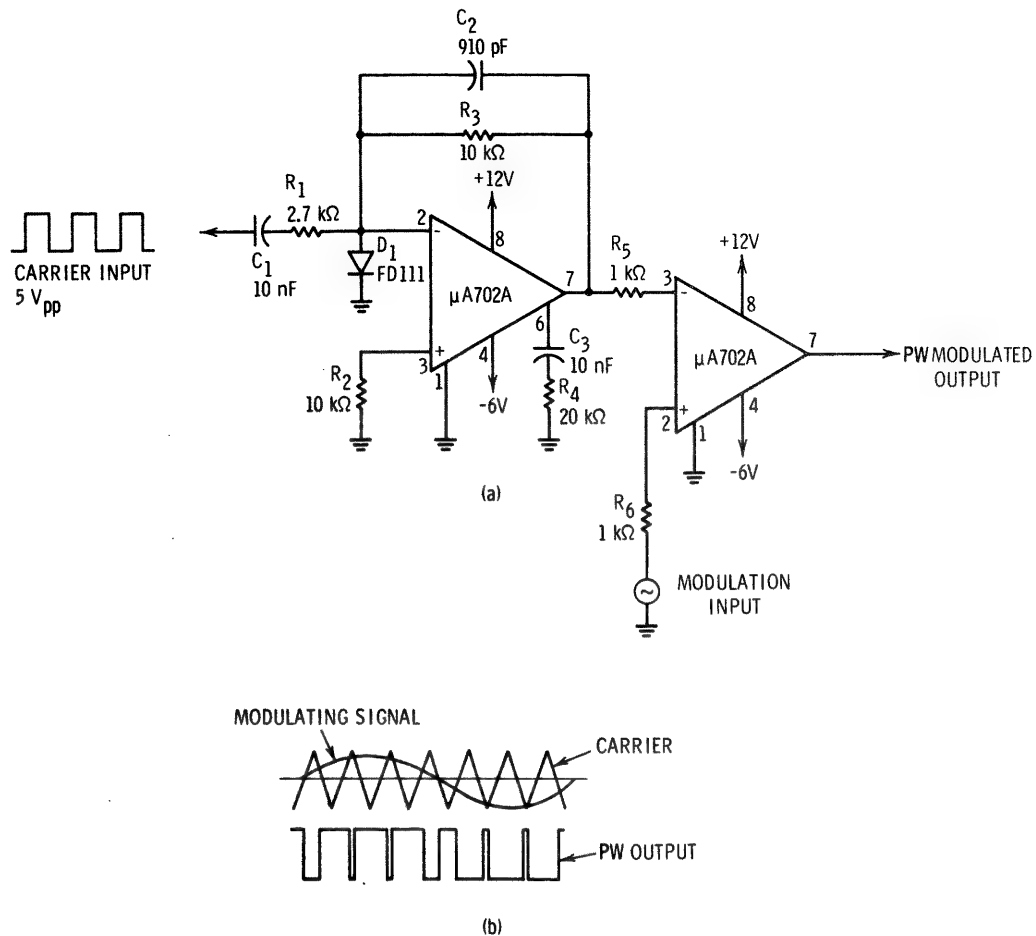
Fig. 16 Pulse Width Modulator.
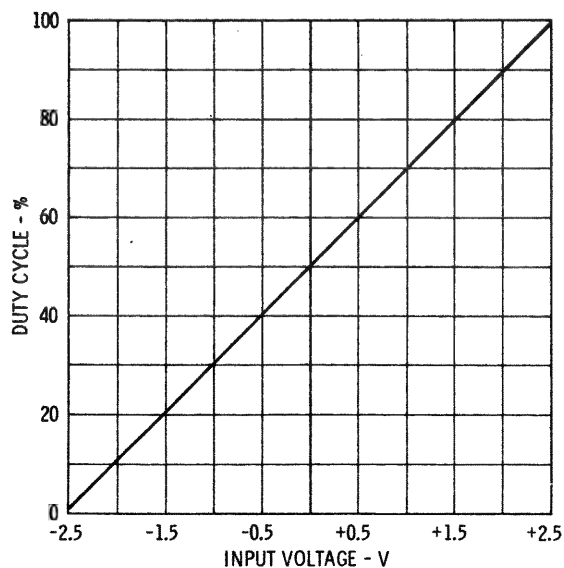
Fig. 17 PW Modulation Linearity.

PULSE-WIDTH DISCRIMINATOR

The circuit of Figure 18 gives a digital output when the width of an input pulse exceeds a preset value. With no input signal, switch Q_1 is biased on, holding the $\mu A702A$ integrator in a reset condition. An input pulse applied to the base of Q_1 turns it off, allowing the integrating capacitor to charge at a rate

$$\frac{V^-}{R_1 C_1} \text{ volts/second} \qquad (23)$$

where V^- is the negative supply voltage.

Thus, the output of the $\mu A702A$ is a ramp that increases linearly with time during the duration of the input pulse.

If the pulse is wide enough to allow the output ramp to reach the reference voltage set by R_5, the $\mu A710$ comparator regeneratively switches on and remains on for a period of time equal to the difference of the input pulse width and the reference pulse width given by

$$\tau_{ref} = \frac{V_{ref}}{V^-} R_1 C_1$$

where V_{ref} is the adjustable voltage at the input to the comparator. If the input pulse width is less than τ_{ref}, there will be no output from the comparator.

The circuit values shown in the figure provide a range of discrimination from about 1 to 100 μs. Longer pulse widths can be detected by increasing R_1.
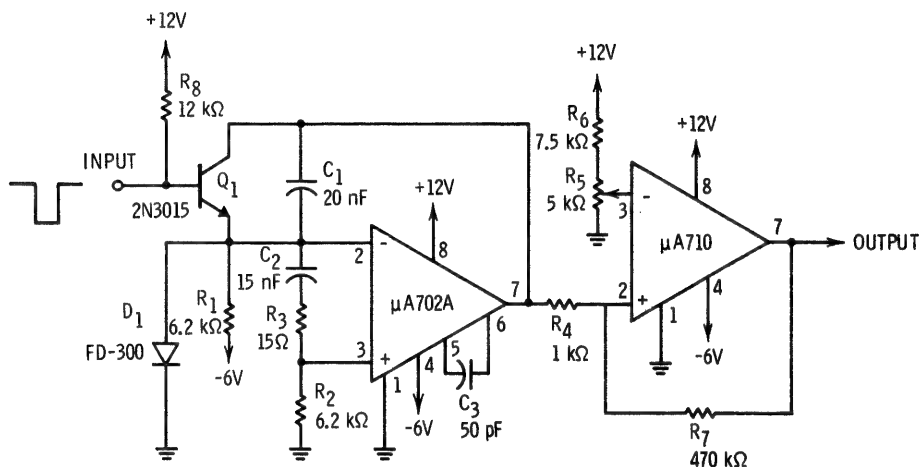
Fig. 18 Pulse Width Discriminator.

SECTION F   COMPARATORS

LEVEL DETECTOR WITH HYSTERESIS

In some applications where there are large amounts of noise on the signal when it is passing through the threshold of a level detector, it is desirable to have some hysteresis in the transfer characteristic. The hysteresis is generally made somewhat greater than the maximum expected noise. A circuit using external positive feedback to produce hysteresis is shown in Figure 1.

The upper and lower trip points of this circuit can be written as follows:

$$V_{UT} = V_{ref} + \frac{R_1 [V_{O(max)} - V_{ref}]}{R_1 + R_2} \qquad (1)$$

and

$$V_{LT} = V_{ref} + \frac{R_1 [V_{O(min)} - V_{ref}]}{R_1 + R_2} \qquad (2)$$

Therefore, the hysteresis is

$$V_H = V_{UT} - V_{LT}$$

$$= \frac{R_1 [V_{O(max)} - V_{O(min)}]}{R_1 + R_2} \qquad (3)$$

The minimum amount of hysteresis obtainable is determined by the forward gain and output swing of the comparator. It should not be made

a. CIRCUIT   b. TRANSFER FUNCTION

Fig. 1 Level Detector with Hysteresis.

Fig. 2 Circuits for Obtaining a Higher Input Resistance.

less than about 5 mV, since oscillation will occur on the positive portion of the transfer function if the small signal gain of the comparator is not greater than the ratio of the feedback resistors. When the comparator is used with logic circuits, reduced hysteresis can usually be obtained by taking the positive feedback from the output of the logic. The additional gain of the logic permits a smaller hysteresis: with the additional gain of a $DT\mu L$ gate, for example, it can be made less than $0.2mV$.

With the connection in Figure 1, the μA710 can be substituted for a Schmitt trigger. It has an advantage in that nonzero trip points can be obtained, and both the upper and lower trip points are easily and independently adjustable over a wide range of positive and negative voltages.

HIGH-INPUT RESISTANCE COMPARATOR

In a number of applications, the input currents of the μA710 and μA711 are high enough to cause significant error due to loading of the signal and reference-voltage sources. In these instances, a transistor pair can be used in front of the comparator to reduce the input currents. Two possible circuits are given in Figure 2. The circuit using the PNP pair is most flexible in that the full input voltage range of $\pm5V$ is still available, but the NPN circuit is quite satisfactory when comparison is made at input voltages above $-2V$. It is possible to balance out the comparator offsets in these circuits by unbalancing the emitter resistors (R_1 and R_2) on the input transistors.

The speed of the comparator is affected somewhat by the addition of the input stage. This is

caused primarily by collector-base capacitance of the input transistors loading the source. The transistors shown in Figure 2 were selected for low collector-base capacitance as well as high current gain, and should load the source with a total capacitance of less than $10pF$.

ZERO-CROSSING DETECTOR*

Often in the processing of electrical analog data, a power spectrum analysis of some particular signal waveform must be performed. This procedure requires that the frequency content of the signal waveform of interest, within a specified passband, be extracted from the broadband signal and noise. A zero-crossing detector using the μA702A operational amplifier provides a simple and effective means of performing such an operation.

A zero-crossing detector is a device that changes state each time the analog input signal passes through zero (or through its average reference level). The input signal is thus converted into a train of frequency-dependent pulse widths, and the resultant zero-crossing intervals may then be examined for frequency content.

This "infinite" clipping of the signal virtually eliminates distortion caused by amplitude fluctuations, circuit variations, and noise, and permits simplification of further data processing through the use of digital techniques. These features are

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especially valuable for information processing systems where signal storage and correlation processes are to be utilized, such as in digital beam-formers and correlators.

The commonly used Schmitt trigger and multistage limiter-clipping circuits can exhibit large errors in zero-crossing information. The Schmitt trigger introduces distortion due to its large "on-off" hysteresis characterstic. The circuit does not change state when the input signal passes through zero, but at different levels for positive-going or negative-going signals. Distortion in multistage limiters is caused by a shift in the average reference level after each successive stage of limiting, arising because the signal cannot be fully clipped in one operation. Large peaks (which may be of one polarity only) are clipped by the first stages of the limiter, thus altering the waveform to produce a different average level. The following limiter stage then clips the resultant signal about the new average level, which can completely change the character of the original signal.

The large voltage gain and dynamic range of the μA702A permit full clipping of a signal by a single stage of processing. The circuit shown in Figure 3 exhibits a nearly ideal transfer characteristic for a zero-crossing detector. The amplifier has full open-loop gain (about 70 dB) when the output is less than the forward voltage limits of the diode network, and it has very little gain outside this range. Thus, an extremely wide dynamic range of input signals, including small voltage excursions on the order of $\pm 500\mu V$, will drive the amplifier to the maximum output of $\pm 1.5V$. Thus, a random analog waveform fed into the input of the circuit will be uniformly clipped with negligible hysteresis or loss of average reference level.

A useful variation of the basic circuit is obtained by replacing R_1 in Figure 3 by a capacitor. The output signal then changes state each time the input signal passes through an amplitude peak, rather than through zero. Since the signal rate-of-change is zero at an amplitude peak, this peak-detector circuit functions as a zero-crossing detector for the first derivative of the input signal.

The use of both zero-crossing detectors and peak detectors results in simple, accurate data
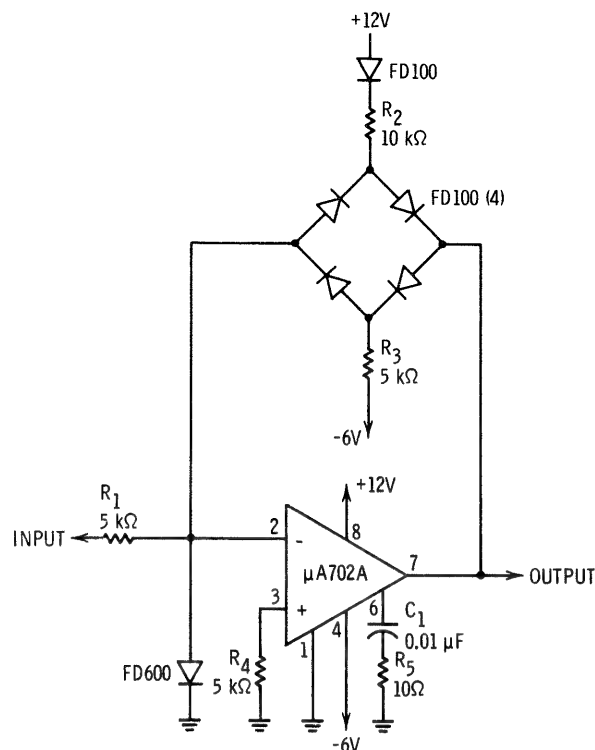
Fig. 3 Zero-Crossing Detector.

processing systems. For example, a position pick-off sensor, monitored by both circuits, would provide precise information regarding the time at which the system being measured passed through its rest position ($x = 0$) and when its velocity reached zero ($dx/dt = 0$). These signals may be used as final output information, or may serve as timing or gating signals to initiate synchronous sampling of other instantaneous functions. The simplicity, reliability, and extremely small size of the μA702A permit many such circuits to perform complex data processing in any easy and convenient manner.

NUCLEAR REACTOR BI-STABLE TRIP*

Bi-stable trips in nuclear reactor safety systems are used to sense dangerous levels of neutron flux, temperature, pressure, etc. The function of these circuits is to sound an alarm and send a logic signal to the automatic safety system when a given output level from the monitoring transducer is exceeded.

An accurate and reliable bi-stable trip using a μA702A operational amplifier is shown in Figure 4.

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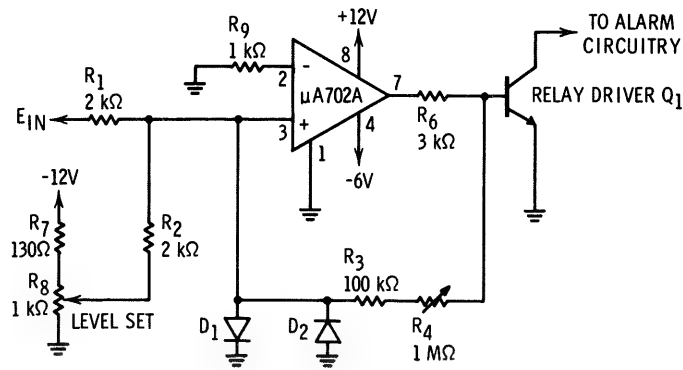
Fig. 4 Nuclear Reactor Bi-stable Trip.

The output of the monitoring system is applied to the non-inverting input through R_1. Since the voltage range of the sensor (0 to $+10$ V) is outside the input voltage limits of the μA702A, the LEVEL SET potentiometer is returned to -12 V to shift the level of the input signal to zero. When the input signal rises a few mV above the threshold voltage determined by the LEVEL SET control, the μA702A will switch on, operating the relay driver and the alarm system. The diodes on the input protect the amplifier from damage due to excessive input voltages.

Adjustable hysteresis of the triggering level is provided by positive feedback through R_3 and R_4. This improves noise immunity and also serves to hold the amplifier on, once the triggering level has been exceeded. The amount of hysteresis is proportional to the output voltage swing and the positive feedback resistors. The output swing is clipped at $0.7V$ in the positive direction by the emitter-base junction of the driver transistor, and at $-5.3V$ by the amplifier. With the resistor values shown, the hysteresis can be set anywhere between 10 mV and 100 mV.

The excellent temperature stability of the μA702A provides a triggering repeatability nearly an order of magnitude better than that of more expensive circuits constructed with discrete components. The great reduction in physical size is also of considerable importance, since a typical nuclear system often employs 50 or more of the trip-type circuits.

PHOTODIODE LEVEL SENSOR

Figure 5 illustrates a light-level sensor using a photodiode as a detector. The circuit as shown functions as a current-operated Schmitt trigger with a $4.0 \pm 0.1\mu A$ trip level and $0.1\mu A$ hysteresis. The differential-input pair provides higher current

resolution than the μA702A alone. The trip level is determined by R_1, while the hysteresis is governed by the positive feedback from the divider, R_5 and R_6, through R_2. Output drive to an RTL gate is provided from the frequency compensation pin. This gives a current-limited drive without the use of clamping diodes.
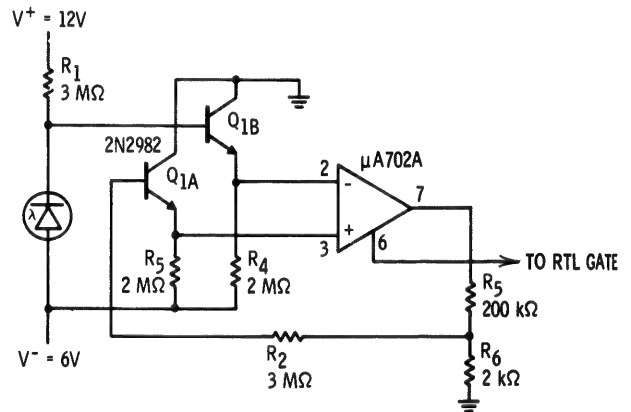
Fig. 5 Photodiode Level Sensor.

TEMPERATURE CONTROLLER

Figure 6 shows an electronic temperature controller for temperature-stabilized ovens. Over $100W$ can be delivered to the heater, and the temperature is held constant within $0.5°C$ of the desired value. The circuit operates in the switching mode to minimize dissipation in the control transistors.

The temperature-sensing diode, D_1, is biased at a constant current by the first operational amplifier. Under this condition, the diode forward voltage has a linear temperature coefficient of about -2.2 $mV/°C$. The diode current is set at 1 mA by R_4 and the $R_1 - R_3$ voltage divider at the μA709 non-inverting input; this divider also establishes a $5V$ common mode level for both amplifiers so that they can be operated from a single $+30V$ supply.
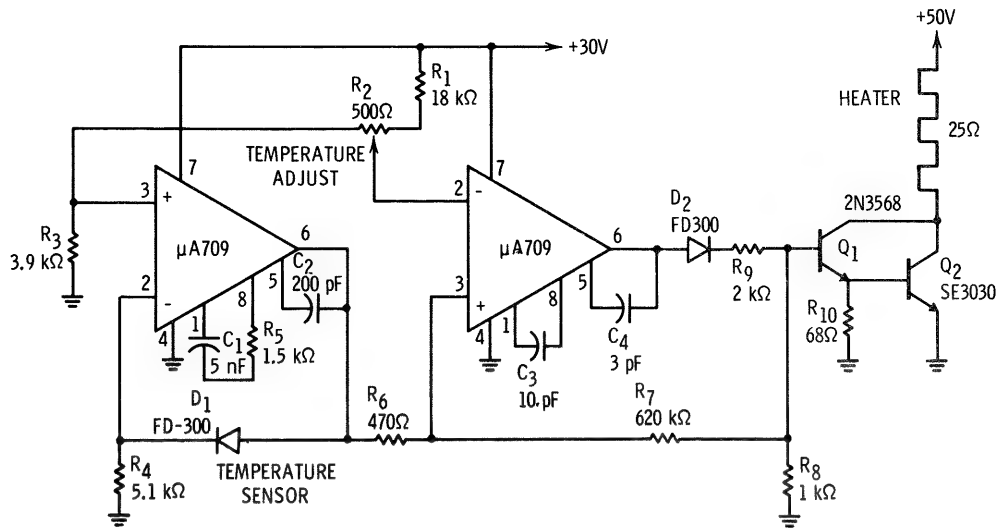
Fig. 6 Temperature Controller.

The diode voltage is fed to the second operational amplifier, which compares it with the voltage determined by the temperature-setting potentiometer, R_2. If the sensor is colder than the pre-set temperature, the amplifier will turn on and drive Q_1 and Q_2 into saturation, thus applying full power to the heater. The power will remain on until the temperature rises slightly above the correct value. The difference in temperature between where the power is turned on and where it is turned off is determined by the hysteresis created by the positive feedback around the amplifier through R_7. The amount of hysteresis is approximately

$$\frac{R_6\,(V_{BE1} + V_{BE2})}{R_6 + R_7} \qquad (4)$$

where the V_{BE}'s are the base-emitter voltage of Q_1 and Q_2.

For the values shown in the figure, the hysteresis is about 1 mV, meaning that the temperature will be controlled to 0.5°C of the desired value.

LINE RECEIVERS

Frequently in the design of digital systems it is necessary to interconnect various equipment over long lines where the possibility of picking up considerable noise exists. In these cases, it is desirable to use a line receiver that has considerably more noise immunity than standard logic circuits to precondition the logic signals. Figure 7 shows a line receiver using a μA710. The resistive divider

on the input of the comparator permits higher level logic signals than are possible with the μA710 alone (up to $\pm 14V$ in this case). It is also possible to put a capacitor at the comparator input (C_1) to make the circuit insensitive to fast noise spikes. Because of the high gain of the comparator, fast-rise output pulses can be obtained even with this integrating capacitor.
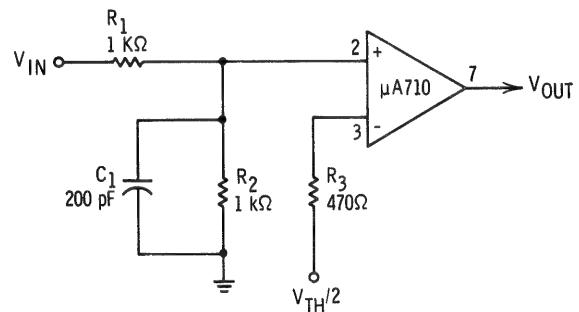
Fig. 7 High Noise-Immunity Line Receiver for Slow, High-Level Logic.

It is sometimes necessary to design a piece of logic equipment to interface with any one of the many types of digital logic (RTL, DTL, CML, CTL, etc.). As these types can have widely different logic levels, the input circuitry must possess considerable flexibility to accommodate all. A circuit that satisfies the requirements is shown in Figure 8. The input threshold voltage can be adjusted over a $\pm 5V$ range with a single control. A μA702A operational amplifier provides an adjustable reference voltage with a very low source impedance. One such amplifier can handle over a hundred comparators.
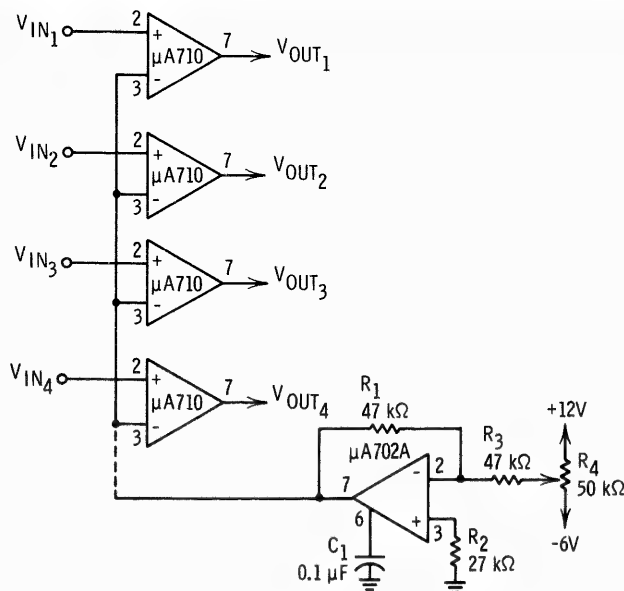
Fig. 8 Adjustable-Threshold, High-Noise-
Immunity Line Receivers.

DOUBLE-ENDED LIMIT DETECTORS

The design of test equipment frequently calls for a circuit that will indicate when a voltage goes outside some preset tolerance limits. The circuit in Figure 9, using a μA711 dual comparator, will accomplish this function. A lower limit voltage (V_{LT}) and an upper limit voltage (V_{UT}) are supplied to the dual comparator. When the input voltage exceeds the upper limit or drops below the lower limit, the output of the comparator swings positive and turns on the lamp driver. A feature of the circuit is that the limit detector can be disabled

when it is not being used by grounding the strobe terminals. In addition, up to eight dual comparators can be wired with common outputs and used to feed a single lamp driver.

The peak output current of the lamp driver is limited by R_2 while the bulb is turning on and the filament resistance is low. R_1 limits the output current of the comparator after the lamp driver saturates. To make the accuracy dependent on offset currents rather than bias currents, the relative values of the source resistances for the signal and reference voltages should be as indicated on the schematic, and should be as low as possible.

A similar level detector circuit* is shown in Figure 10. In this circuit, hysteresis is provided at both the upper and lower threshold levels. A μA709 operational amplifier serves as both a buffer and a difference amplifier. With the component values shown, an output is obtained from the μA711 when the difference between the two input voltages exceeds $0.55V$, and a hysteresis of approximately $50mV$ is obtained.

Even more complex level-sensing circuits are possible. A typical example of where they might be used is in test equipment for grading zener diodes by voltage. The voltage output of the zener being tested could be fed to a number of μA710's. Each of these comparators would sense one of the grade-separation voltages, and the outputs would be fed to logic which would drive the readout circuits. Alternately, a μA711 could be used for each one of the voltage brackets, thereby eliminating the logic.
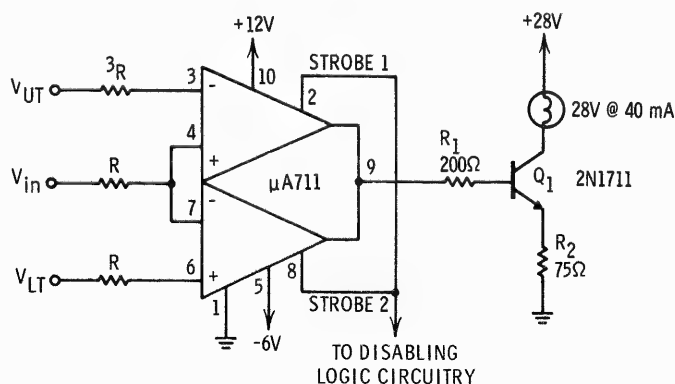
Fig. 9 Double-Ended Limit Detector for Automatic Go/No-Go Test Equipment.

*Suggested by Frank Thomas, Bendix Corp., Eclipse-Pioneer
Division

+12V

R4 20 kΩ

R12 5.6 kΩ

R11 24 kΩ

R3 1.5 kΩ

C1 2000 pF

R6 510Ω

R1 10 kΩ

V_{IN_1}

2

μA709

1

8 6

5

3

μA711

V_{OUT}

R7 510Ω

V_{IN_2}

R2 10 kΩ

R5 20 kΩ

C2 100 pF

R8 510Ω

R9 510Ω

R10 24 kΩ

R13 5.6 kΩ

(a) CIRCUIT

-12V

V_{OUT}

50 mV

50 mV

$V_{IN_2} - V_{IN_1}$

-0.55V +0.55V

(b) TRANSFER FUNCTION
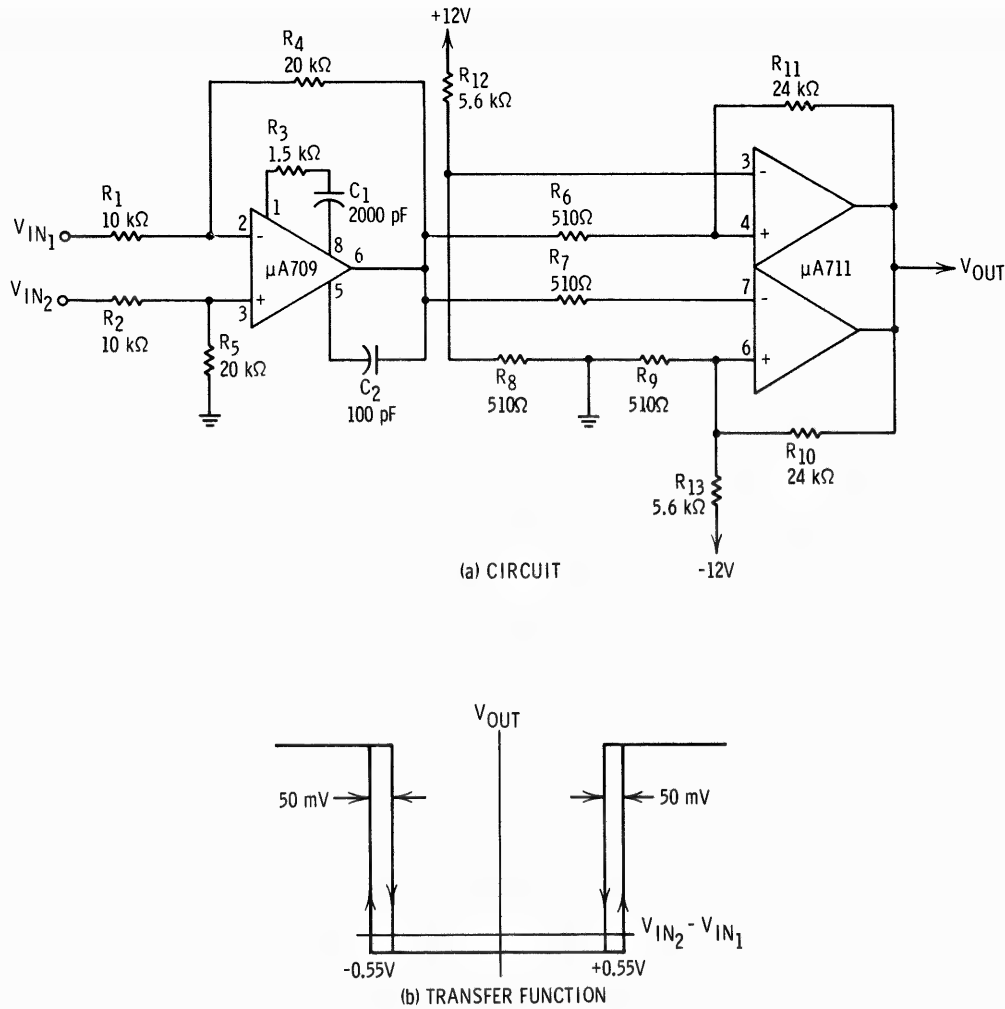
Fig. 10 Double-Ended Differential Threshold Detector with Hysteresis.

SWITCHING POWER AMPLIFIER

A pulse-width-modulator/power switch that can be used to drive DC servo motors, proportional-actuators, or other loads requiring bi-directional control, can also be made with the μA710 or μA711 (see Figure 12). The principle of operation is similar to that of the switching regulator described previously, and can be explained using the simplified schematic in Figure 11.

The power-switch bridge in Figure 11 functions such that if Q_2 is turned on, Q_3 is likewise turned on through R_5, applying the full supply voltage across the load in one direction. Alternately, when Q_5 is turned on, Q_4 is also turned on, applying the supply voltage across the load in the opposite direction. Hence, either Q_2 or Q_5 can be switched on and

off at a high frequency, with the duty cycle determining the average value of the load voltage. Since the power losses in the transistors are small when they are either saturated or cut off, large amounts of power can be controlled without dissipating much power in the control transistors.

The average value of the load voltage is sensed by a μA709 connected as a differential, integrating amplifier. The input signal to the power amplifier (V_{IN}) is also fed to this μA709. The output voltage of the μA709 can be written in terms of these voltages, using standard operational amplifier theory:

$$V_O = V_{IN} - \frac{R_{16}}{R_{17}} V_{OUT} \qquad (5)$$

where it is assumed that $R_{14} = R_{15}$ and $R_{16} = R_{17}$.

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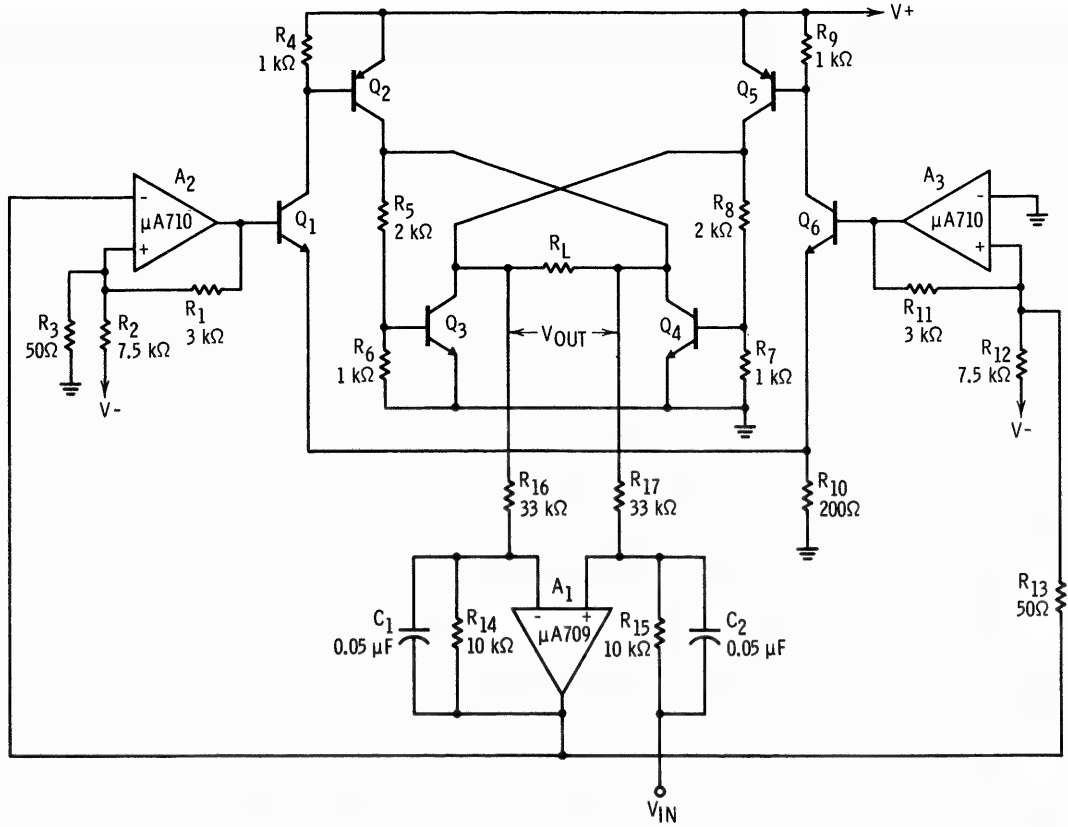
Fig. 11 Simplified Schematic of the Bi-Directional, Switching, Power Amplifier.

The output of the μA709 is fed to two μA710 comparators, which in turn drive a current switch. One comparator (A_2) controls the turn-on of one side of the switching bridge Q_2, while the other controls the opposite side. Positive feedback is used on both comparators to provide hysteresis.

With a positive input voltage, the output of the μA709 will go positive, turning on one comparator (A_3). This will drive one side of the bridge, applying the full supply voltage across the load. The load voltage is then fed to the μA709 in such a direction as to make the output swing negative at a rate determined by the integrating capacitors, C_1 and C_2. Power will continue to be applied to the load until the output of the μA709 falls by an amount equal to the hysteresis of the comparator. The hysteresis is made quite small (50 mV), so the switch will be turned on and off without the output of the μA709 becoming much different than zero. Hence, Eq. (5) can be set equal to zero, giving

$$V_{OUT} = \frac{R_{17}}{R_{15}} V_{IN} \qquad (6)$$

where V_{OUT} is the average value of the output voltage, since A_1 integrates the switched waveform across the load.

With negative input signals, operation is identical, except that A_2 is switched on, giving an output signal of opposite polarity.

The time required for the integrating feedback amplifier to go from the upper threshold voltage of the comparator where the switch turns on to the lower threshold where the switch turns off depends only on the voltage switched across the load, the input resistance of the amplifier (R_{17} or R_{16}), and the integrating capacitor (C_1 or C_2). The voltage switched across the load is also constant and very nearly equal to the supply voltage (V^+). Therefore, for varying input signals, the "on" time of the voltage switched across the load will be constant and the frequency will vary to control the power. The "on" time is given by

$$t = R_{17} C_2 \frac{V_H}{V_+} \qquad (7)$$

where V_H is the hysteresis of the comparator given by Eq. (3). The average value of the voltage across the load will be

$$V_{OUT} = V^+ \left(\frac{t}{T}\right) \qquad (8)$$

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where T is the period of the switched waveform. Hence, the frequency of the pulse-width-modulated output will be

$$f = \frac{V_{OUT}}{tV^+} \qquad (9)$$

It is necessary to ensure that the hysteresis loops of the two comparators do not overlap. Otherwise, the circuit will operate in a class-A mode, alternately switching on one side and then the other for the full duty cycle, even when the input voltage is zero.

The complete schematic of the power amplifier is given in Figure 12. This circuit operates from a single supply voltage (no negative supply) and provides a much increased power output. Emitter-followers (Q_5 and Q_6) have been added to give an output current capability of several amperes. The bases of the bottom transistors in the bridge are driven from separate emitter-followers (Q_9 and Q_{10}). This base drive could be obtained from the emitters of Q_5 and Q_6, except that excessive saturation voltage of one of the lower power transistors could cause the other lower transistor to become turned on. Diodes have been included (D_7, D_8, D_9, and D_{10}) to clamp the current spikes obtained with inductive loads.

A μA711 has been substituted for the two μA710's. Independent, low-level outputs are obtained by using the strobe terminal as an output terminal. Diodes (D_1 through D_4) are used to clamp the voltage being fed to the current switch (Q_1 and Q_3), which drives the power switch. Q_2 and D_6 have been added to ensure that both the positive and negative output channels cannot be driven simultaneously. This is not a problem during operation (since the comparator turn-on points are kept separated by R_3 and R_4), but it is necessary to guarantee that both channels cannot be driven when the power is first turned on.

The μA711 is operated from ground, $+6V$, and $+18V$, while the μA709 is operated between ground and $+18V$. The necessity for a negative supply is eliminated by using a psuedo-ground for the system at some positive voltage that is within the common mode range of the μA711 and μA709 ($+11V$ and $+2V$ for the μA711; $+4V$ and $+14V$ for the μA709). A convenient value for this voltage is $+6V$. The input signal to the amplifier is the voltage difference between the reference and the input terminal.

The location of the integrating capacitors (C_4 and C_5) has been changed to prevent feeding the switching spikes into the input circuitry. The bypass capacitors should be solid tantalum or disc ceramic to ensure removing the switching spikes.
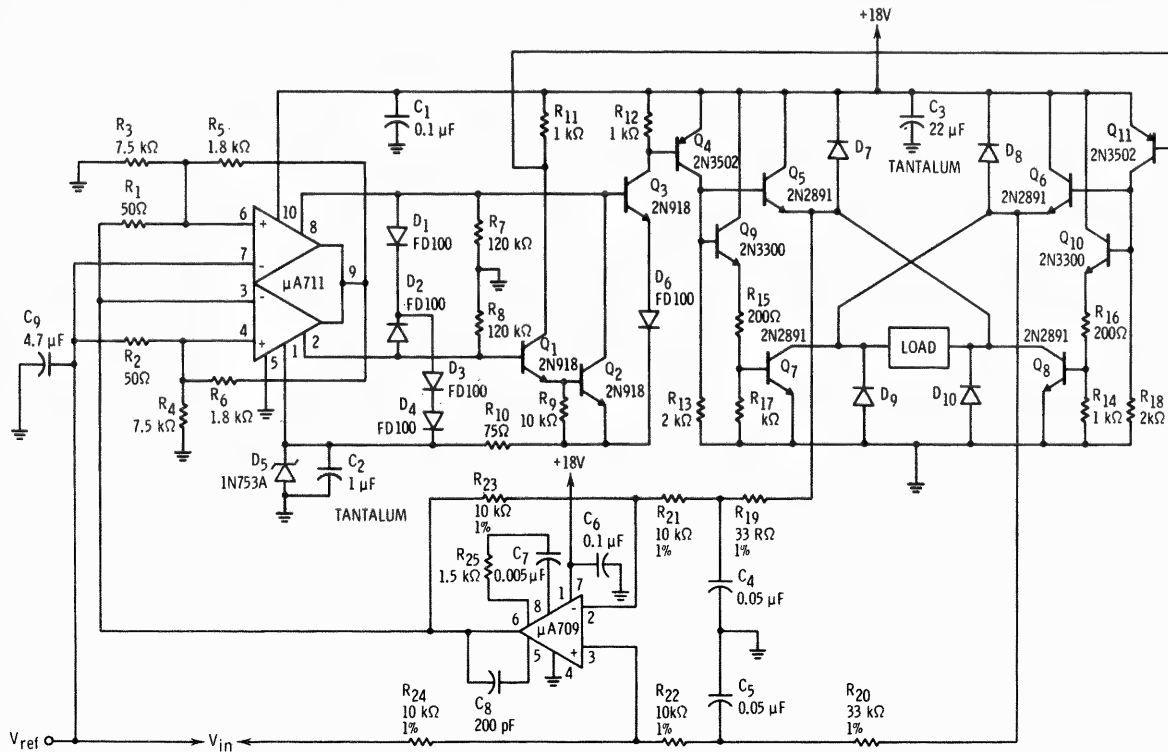
Fig. 12 Complete Schematic of the Switching Power Amplifier.

SECTION G   CONSUMER CIRCUITS

COLOR TV CHROMA REFERENCE SYSTEMS

Accurate reproduction of a televised color image requires the regeneration at the receiver of a 3.58 MHz subcarrier frequency in exact phase with the color burst reference signal transmitted by the station during a portion of the horizontal blanking time.

Three methods are used to re-establish the 3.58 MHz subcarrier in present color receivers: (1) the voltage-controlled crystal oscillator in an APC loop; (2) the injection-locked crystal oscillator; and (3) the narrow band-pass crystal ringing circuit. The most familiar is the crystal oscillator in an APC loop. This system has a wide pull-in range, excellent phase stability and high noise rejection, but requires an external phase detector and frequency controlling element such as a reactance transistor or varicap. The simpler injection-locked oscillator system does not require an APC loop. In this system, the burst is transformer-coupled directly into the oscillator to lock it. The injection-locked system, however, compromises phase stability and noise immunity. For good noise immunity, the circuit Q must be extremely high, meaning that the crystal oscillator must have lower drift than is required in the APC system for acceptable phase stability. Because the system has an output level which is disturbed during burst injection, the circuitry that it drives must be able to accommodate amplitude variations of the reference signal. The ringing system relies on a high Q crystal filter which is energized during the burst period. It continues to ring during the remainder of the horizontal period until reinforced by the next burst. Of the three systems, it is the only one which does not require a killer since there is no demodulation drive in the absence of a burst. However, because it has no output in the absence of a burst, it is not suitable for driving certain types of demodulators.

VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR FOR APC SYSTEM

Figure 1 shows the circuitry for a voltage controlled crystal oscillator. The positive feedback voltage to start and sustain oscillations is taken from a capacitive tap in the tuned circuit at the output of the μA703. This voltage is fed back through a narrow bandpass filter (i.e., the crystal) to the input of the amplifier, completing the regenerative feedback path required for oscillation.
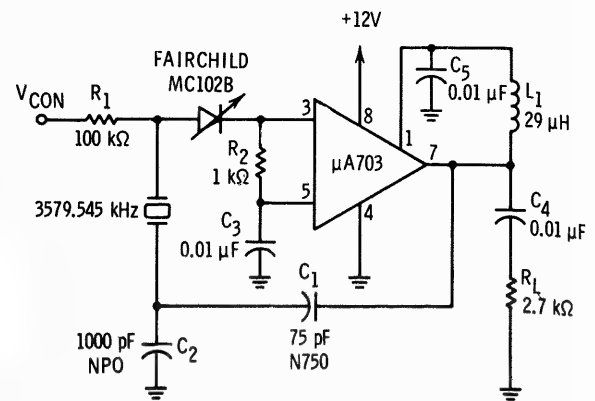
Fig. 1 3.58-MHz Voltage-Controlled Oscillator.

The inductor, L_1, and the series capacitors, C_1 and C_2, make up the reactive components of the temperature-compensated 3.58 MHz output tank circuit. The output signal amplitude (approx. $5V$ peak) is determined by the load resistance, R_L. The loaded Q of the output tank is approximately 5. The inductor, L_1, provides a $\pm 400\ Hz$ oscillator frequency adjustment range with less than a 1 dB change in output level. The range of $\pm 400\ Hz$ is more than sufficient to accommodate the tolerances of all frequency determining components; the more predominant ones being the $\pm .0005\%$ crystal and the $\pm 10\%$ varactor diode in the feedback circuit. A relatively large feedback signal (0.5 V_{pp}) is fed into the "Hi" input of the integrated amplifier to take advantage of its self-limiting properties. The crystal in the feedback circuit is the primary frequency stabilizing element. It operates in the inductive mode and resonates with the capacitance of the varactor diode. The voltage-dependent capacitance of the diode provides a fine frequency control.

The "Hi" input of the μA703 sets approximately 1.5 V above ground and provides an excellent voltage reference point for the varactor diode because of the small change in voltage at this point with variations in temperature and supply. The varactor diode has a nominal capacity of $30 pF$ at 1.5 V reverse bias and $C_{2V}/C_{40V} > 3.1$. With a 1.5 V reverse bias on the diode, a $\pm 1V$ control voltage (which changes the capacitance appreciably) can be applied without forward-biasing the diode. Because the diode always operates reverse-biased, it can be driven from a high impedance phase detector.

The voltage-controlled oscillator frequency and output amplitude versus supply voltage is shown in Figure 2. The frequency drift of the oscillator for changes in ambient temperature is dependent upon the type of crystal used and the over-all layout of the circuit. Figure 3 shows frequency drift vs. temperature with the oscillator being temperature-compensated for only one particular type of crystal in a breadboard layout.
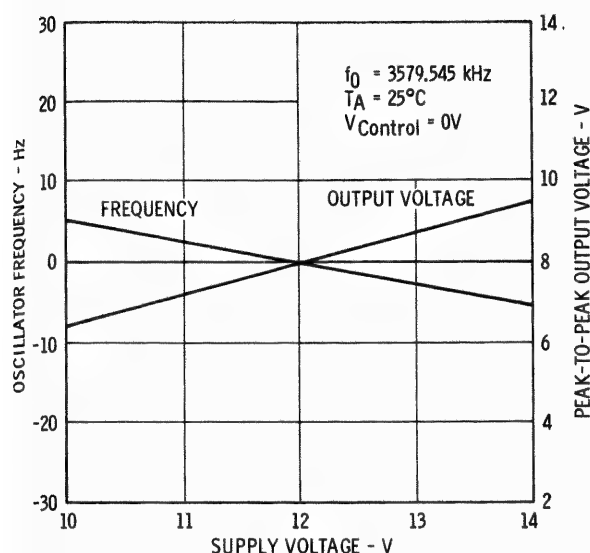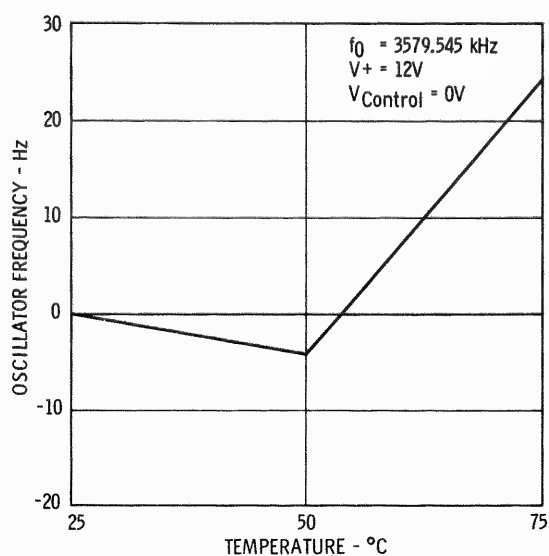
Oscillator sensitivity versus control voltage is shown in Figure 4. The small control voltage needed to compensate for any oscillator drift is easily achieved in a phase detector circuit.

Fig. 2 Normalized Oscillator Frequency and Output Voltage as a Function of Supply Voltage.
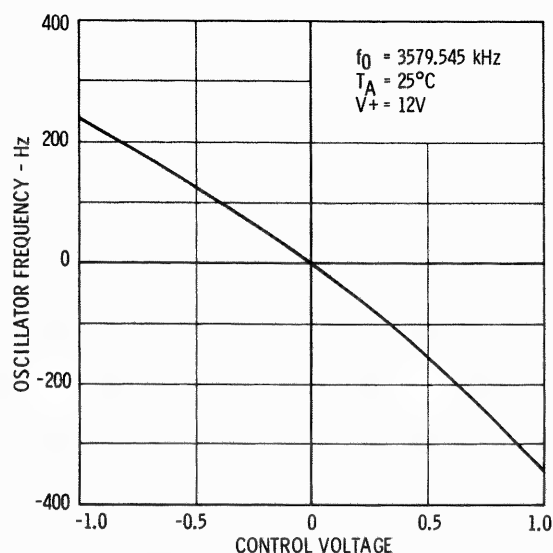
Fig. 4 Normalized Oscillator Frequency as a Function of Control Voltage.

INJECTION-LOCKED CRYSTAL OSCILLATOR

Figure 5 shows the circuitry for an injection-locked crystal oscillator which is basically similar to the voltage-controlled oscillator. The output tuned circuit is the same except that the ratio of C_1 and C_2 is smaller to allow for the additional voltage drop of the burst transformer impedance in the feedback loop. L_1 provides the initial frequency set-up without significantly affecting the output voltage. The crystal in the feedback loop is the primary frequency determining element. It operates in an inductive mode and resonates with capacitor C_3. The burst transformer induces the chroma reference synchronizing voltage into the feedback loop of the oscillator. It is parallel resonant and is tuned for maximum burst amplitude. The total reactance of the feedback loop will be changed during the injection period depending on the frequency difference between the oscillator and the induced voltage. If the ratio of induced voltage to feedback voltage is large, and the frequency difference between the oscillator and induced voltage is small, the oscillator will tend to lock to the induced synchronizing voltage. These two factors will further influence the phase relation between the oscillator and the reference burst in the locked position.

Fig. 3 Normalized Oscillator Frequency as a Function of Ambient Temperature.
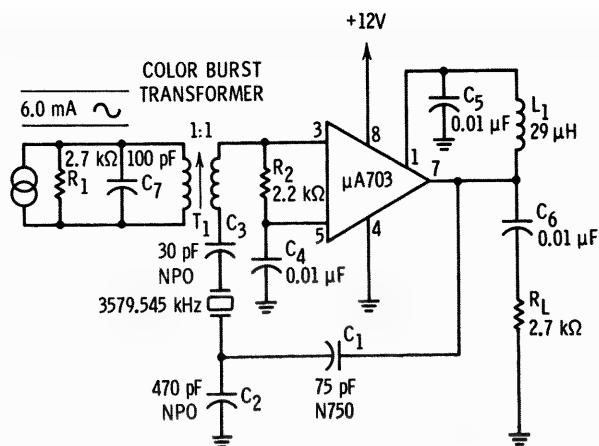
Fig. 5 3.58-MHz Injection-Locked Oscillator.

It has been determined by controlled viewing tests of color scenes that the maximum tolerable phase error in the chrominance signal (or in the regenerated color reference signal) is approximately ±15 degrees. For the burst injection system shown in Figure 5, it was determined experimentally that a burst voltage injected across the crystal and C_3 (which is six times the amplitude of the feedback signal at C_2) would hold the phase error of the locked oscillator to within ±15 degrees for a 100 Hz change in oscillator free-running frequency. Since measured oscillator drift due to all causes is considerably less than 100 Hz (Figure 6 and 7), the expected tint shift in normal set operation would be quite acceptable.
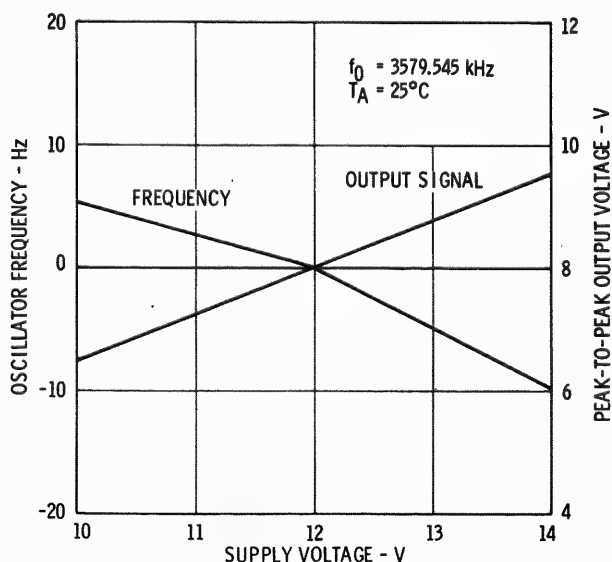
Fig. 6 Normalized Oscillator Frequency and Output Voltage as a Function of Supply Voltage.
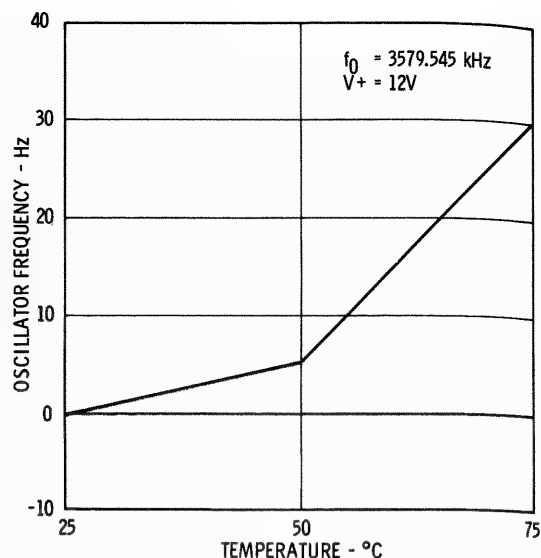
Fig. 7 Normalized Oscillator Frequency as a Function of Ambient Temperature.

The 6 mA peak-to-peak drive current required at the primary of the burst transformer can easily be developed by using another μA703 as a burst amplifier.

In the absence of a synchronizing burst, the injection-locked oscillator frequency and output amplitude versus supply is as shown in Figure 6. Oscillator frequency versus ambient temperature is shown in Figure 7. With a burst voltage six times the amplitude of the feedback signal at capacitor, C_2, injected across the crystal and C_3, the measured phase shift between burst and oscillator signal versus free-running oscillator frequency becomes that shown in Figure 8. Pull-in capability of the
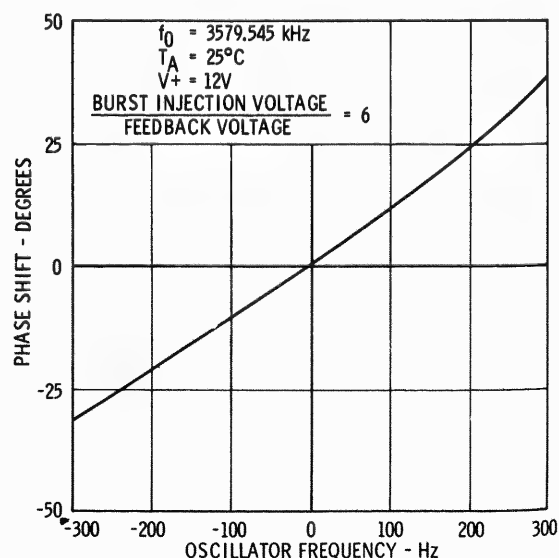
Fig. 8 Normalized Phase Shift as a Function of Normalized Oscillator Frequency.

circuit with a 6:1 injection ratio is $\pm 400\,Hz$—much greater than measured oscillator drift due to all causes.

TV SOUND IF AMPLIFIERS

The μA717 and μA718 have been specifically designed for TV sound IF applications. The basic circuit, using quadrature detection, has been described in Chapter 11.

Figure 9 illustrates the application of the μA717 in an all solid-state black and white TV receiver.

The input signal is coupled into the amplifier via C_1 and L_2; L_1, C_2, and R_2 comprise the quadrature tank for FM detection; de-emphasis is provided by R_4 and C_6, while R_3 controls the gain of the audio amplifier. The output drives a high voltage power stage, Q_2 to develop 1-2W output to the speaker.

A hybrid color TV receiver using the μA718 is shown in Figure 10. Operation of the integrated circuit is the same as above, except that a large output swing is developed to drive the vacuum tube output amplifier.
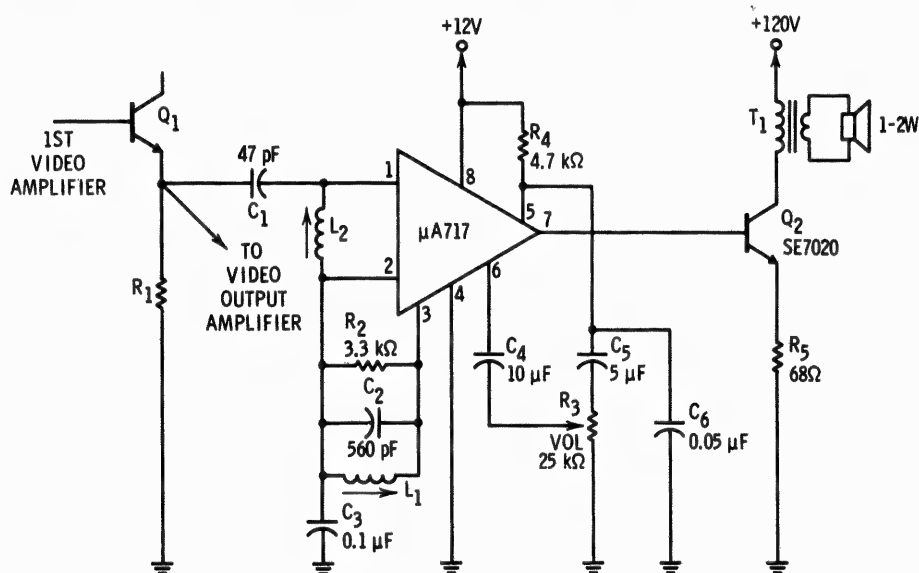
Fig. 9 Black & White TV Sound IF Amplifier.
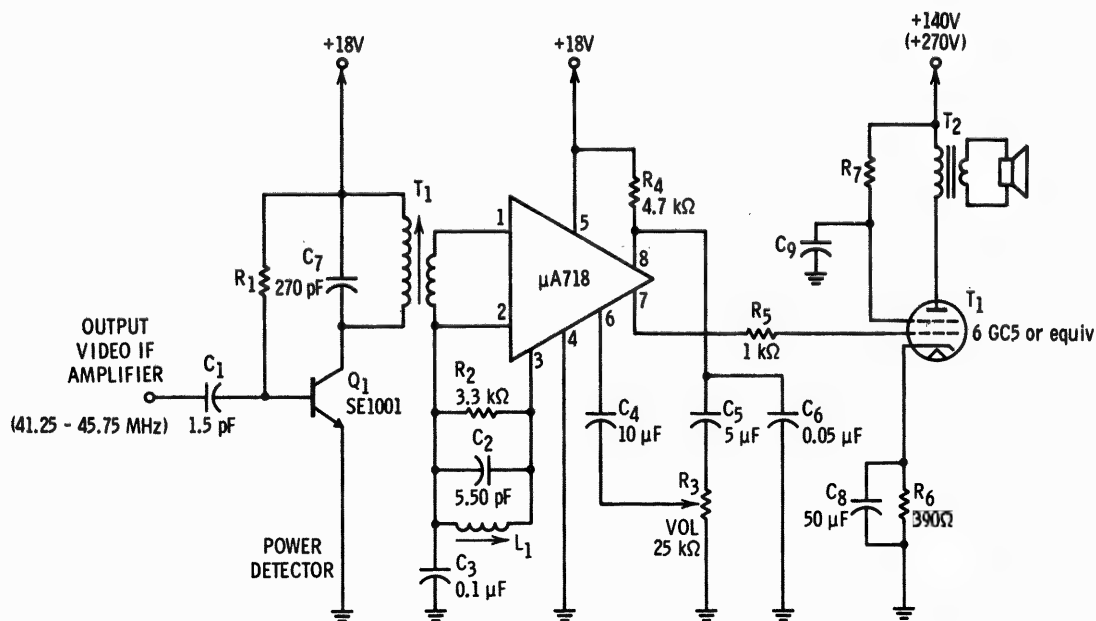
Fig. 10 Color TV Sound IF Amplifier.

FM IF AMPLIFIERS

The excellent limiting characteristics of the μA703 make it particularly suitable for 10.7 MHz IF strips. Figure 11 shows the use of four μA703's in a high-quality FM tuner. Typical performance characteristics are:

Full limiting:	$50\mu V$
Power gain per stage:	26.5 dB
Peak-to-Peak separation of detector:	800 kHz
THD ($\pm75kHz$ deviation at $400Hz$):	$< 0.8\%$
Current consumption:	$27mA$

The basic circuit for using a pair of μA718's in an FM tuner is given in Figure 12. Both the RF and AF sections of the first μA718 are used for amplification, limiting, and selectivity at the IF frequency. The second amplifier provides additional IF gain, FM demodulation, and audio-output.

Figure 13 shows how the μA717 can be used in a table model AM-FM radio to perform the FM limiting and detection functions. Only the power supply and audio sections are shown in detail.
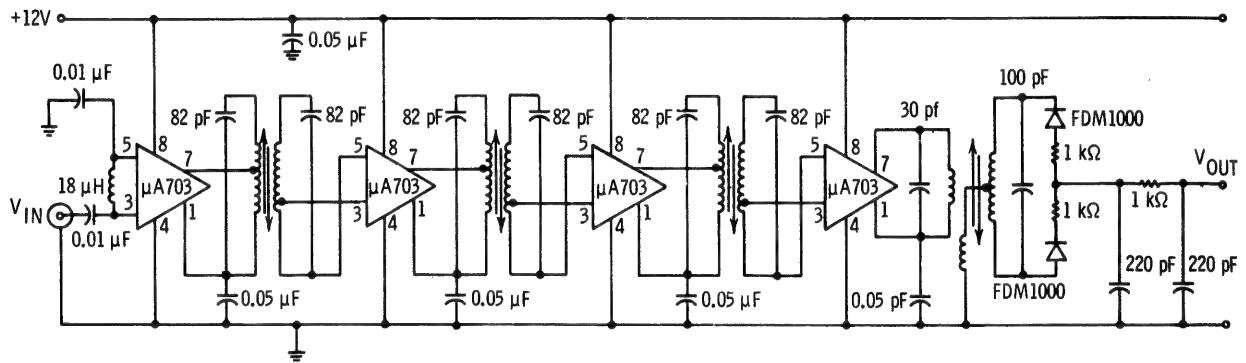
Fig. 11 FM IF Amplifier Using μA703.
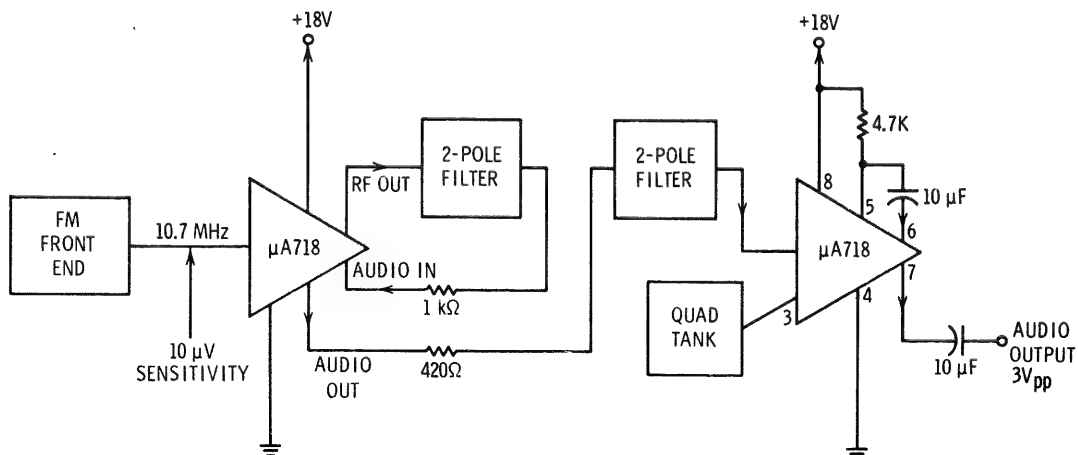
Fig. 12 FM IF Amplifier Using μA718.
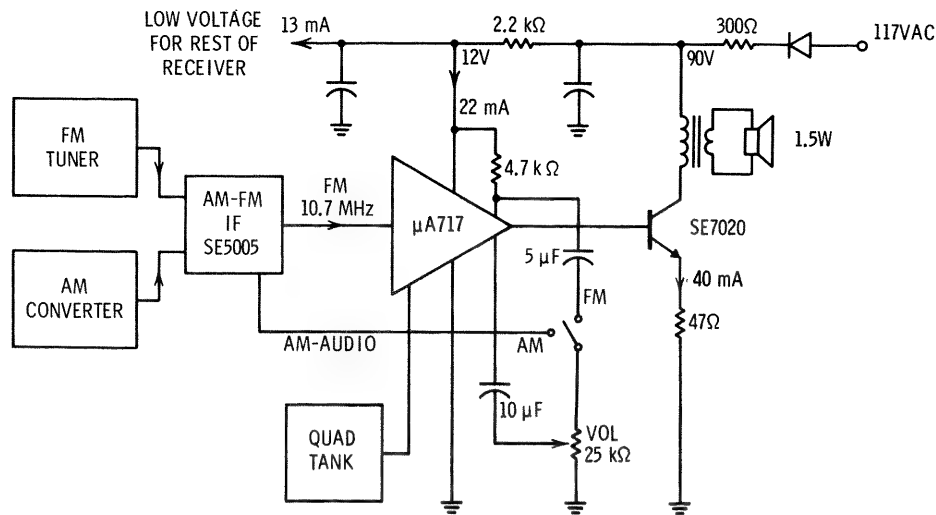
Fig. 13 Table Model AM-FM Radio.

SECTION H   CORE MEMORY SENSE AMPLIFIERS

The μA711 dual comparator can be used as a core memory sense amplifier. This application has the advantage of eliminating many of the tolerance problems encountered in the design of a sense amplifier with the usual differential amplifier/ threshold-detector combination. The method used gives unusual precision and reliability, yet requires from the integrated circuit only what can be done consistently at low cost. Using the dual comparator, the sense amplifier threshold is determined by external resistors and is practically independent of the characteristics of the integrated circuit. Excellent threshold stability over the full military temperature range is inherent in the design.

With this approach, a single integrated circuit can be used as a sense amplifier for practically all coincident current cores presently used. In addition, the circuit is ideally suited to positive "1", negative "0" memories such as bias and nondestructive read. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Up to eight

sense amplifiers can be OR'ed directly. In most applications, the μA711 can be used with only an external resistor network to determine threshold; for very demanding applications, the comparator can be combined with relatively inexpensive discrete parts to obtain the required performance.

The circuit design and operating characteristics of the μA711 have been covered in Chapter 7. Table I lists the typical electrical characteristics of the circuit.

SENSE AMPLIFIER CIRCUITS

Conventional sense amplifiers are usually differential-input, differential-output amplifiers which amplify the output of the cores and eliminate the comparatively large common mode signals present during read. A full-wave rectifier and sense-level threshold are inserted at the output of the amplifier to discriminate between the "0" and "1" outputs of the cores.

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TABLE I

TYPICAL μA711 ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		UNITS
	$(T_A = 25°C, V^+ = 12.0V, V^- = -6.0V$ unless otherwise specified)		
Input Offset Voltage	$V_{out} = +1.4V$, $R_S \leqslant 200\Omega$, $V_{CM} = 0$	1.0	mV
	$V_{out} = +1.4V$, $R_S \leqslant 200\Omega$,	1.0	mV
Input Offset Current	$V_{out} = +1.4V$	0.5	μA
Input Bias Current		25	μA
Voltage Gain		1500	
Response Time (Note 2)		40	ns
Strobe Release Time		12	ns
Input Voltage Range	$V^- = -7.0V$	±5.0	V
Differential Input Voltage Range		±5.0	V
Output Resistance		200	Ω
Positive Output Level	$V_{in} \geqslant 10mV$	4.5	V
Loaded Positive Output Level	$V_{in} \geqslant 10mV$, $I_0 = 5$ mA	3.5	V
Negative Output Level	$V_{in} \geqslant 10mV$	-0.5	V
Output Sink Current	$V_{in} \geqslant 10mV$, $V_{out} \geqslant 0$	0.8	mA
Strobe Current	$V_{strobe} = 100mV$	1.2	mA
Positive Supply Current	$V_{out} \leqslant 0$	8.6	mA
Negative Supply Current		3.9	mA
Power Consumption		130	mW

This approach has the disadvantage that the offset voltage, the differential gain, the output common mode level, the rectifier offset, and the output threshold level must all be accurately controlled to get a precise input-referred threshold level. A much more satisfactory solution is to use a voltage comparator and insert the threshold voltage at the input. In this case, the accuracy is only affected by the offset voltage of the comparator (which similarly affects the differential amplifier in the conventional approach). Variations in voltage gain and frequency response do not affect accuracy as long as these are high enough.

The problem in using a voltage comparator as a sense amplifier has been that the threshold voltage is not easily inserted at the input when common mode rejection is required. A straightforward approach to the problem requires a floating voltage source. The circuit in Figure 1, however, inserts the threshold at the input using a grounded supply, yet it provides respectable common mode rejection. In this circuit, R_1 and R_2 provide termination for the sense line. The sense level is essentially equal to the voltage across R_3 and R_4 caused by the current from the positive supply (V_{adj}) through R_5 and R_6. The grounded tap on the line termination resistors provides a sink for

this current. The use of two comparators enables the circuit to respond to either positive or negative input signals above the preset threshold.

The advantages of using the dual comparator are many. The threshold level is determined by inexpensive external resistors, and so a single dual comparator design can be used for a wide variety of core sizes. This permits standardization and allows production volumes that make use of the true economies of integrated circuits. The threshold voltage can also be easily adjusted to match the optimum value for a particular memory bank. This is done with a single adjustment for the entire battery of sense amplifiers by varying V_{adj}. In addition, because input offset voltage is the prime determinant of threshold inaccuracy, the change of threshold voltage with temperature can be held to a minimum. This is important even though core outputs vary substantially with ambient temperature for a constant current drive. The reason is that if write and read functions are to be done at different temperatures, the core variation must be compensated with the current drive for the cores. If an attempt is made to compensate for core thermal variations with corresponding thermal changes in sense amplifier threshold, it is not
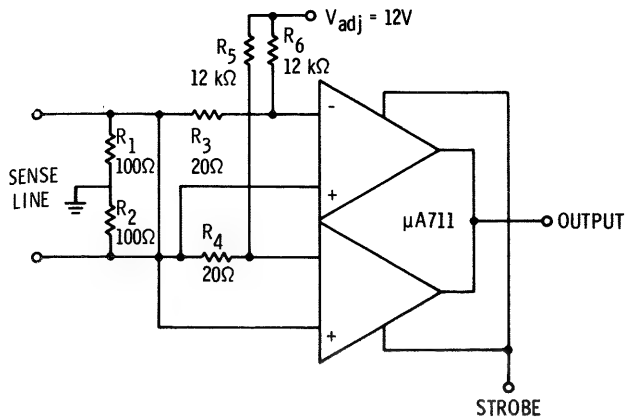
Fig. 1 Basic Sense Amplifier Configuration.

Fig. 2 Sense Amplifier with Improved Insensitivity to Common Mode Signals.

practical to write into the cores at one temperature and read out at another. The best situation is for the sense amplifier to maintain a constant threshold over the full temperature range.

With the circuit in Figure 1, the sense level will be affected by a common mode signal, although only by approximately 8% for a $1V$ signal with V_{adj} = $12V$. This is rarely a problem because in most memories the common mode signal during read is less than $0.5V$. This sensitivity can be reduced by increasing R_5 and R_6 and using a higher voltage to set the threshold. In the unusual case where very large common mode signals are present during read, the circuit in Figure 2 can be used. This circuit uses additional resistors to balance the input bias network to the common mode signal, and it provides at least an order of magnitude better common mode rejection. This circuit is especially useful if the resistor network is purchased as a thin (or thick) film assembly, since the extra resistors add little complexity to the complete assembly and since the tolerance on the balancing resistors can be looser than the tolerance on the threshold-determining resistors.

The high-frequency common mode rejection can be severely degraded by unbalanced stray capacitances on the sense line and on the comparator input. For this reason, low-capacitance resistors should be used for R_5 and R_6; the physical layout should also be such as to minimize strays.

Because the comparator is directly coupled and employs low storage time devices, the recovery from either differential or common mode overloads is less than 50 ns — regardless of their amplitude. The direct coupling also removes the pattern sensitivity of threshold voltage seen with AC coupled amplifiers.
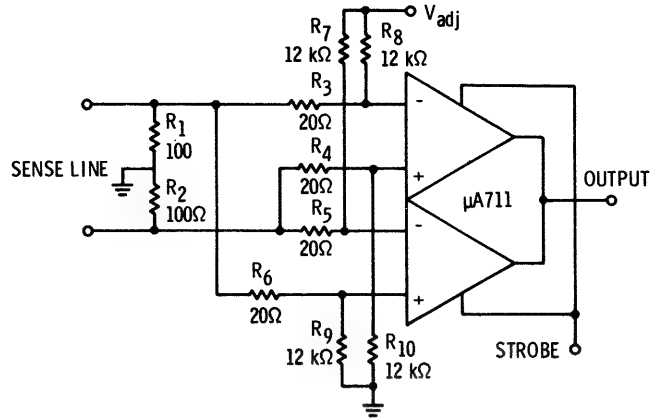
The response of the sense amplifier to a typical input "1" is shown in Figure 3. With an input signal that is $7mV$ above the discrimination level for 45 ns, an output pulse that is above the logic threshold for 50 ns is obtained. Longer output pulses can be obtained using the pulse stretching techniques described in Chapter 7.
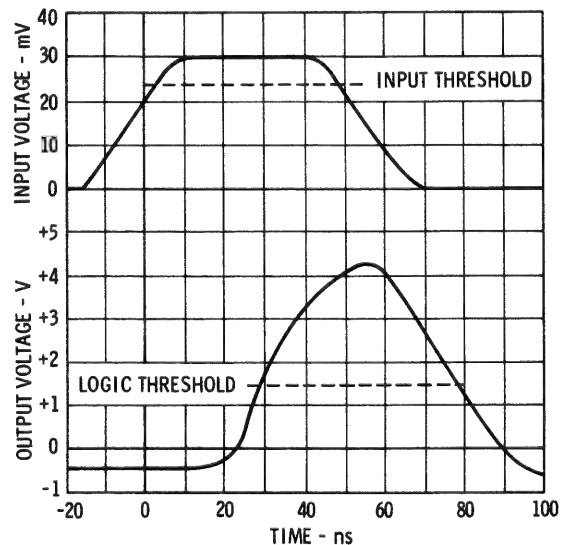
Fig. 3 Response of the Basic Sense Amplifier Circuit, with a 23 mV Threshold Setting to a 30 mV Input Pulse.

In determining the recovery time of the sense amplifier to an overload or to a maximum "0" when time strobing is used, only the response time of the input stage need be considered because the second stage is held in saturation by the strobe. Hence, when the amplifier is recovering from the input signal, the feedback capacitance of the second stage does not slow the recovery. Since the overall response time of the device is limited by this

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feedback capacitance (and second stage storage), recovery is exceptionally fast; the strobe signal can therefore be applied almost immediately after the input signal goes below the input discrimination level without obtaining a false output.

When working with very small cores, the output signal can be so small as to approach the offset of the comparator. In this case, some sort of amplification is required before going into the sense amplifier. In addition, since DC offset will be a basic limitation on discrimination level in the pre-amplifier stage, AC coupling is also required. A method of accomplishing this is shown in Figure 4. A differential input stage is used as a preamplifier with a gain of 10. Its output is coupled into the dual comparator connected as a sense amplifier, with a threshold voltage setting of 50 mV, in a circuit similar to that in Figure 1. An inductor (L_1) is used to remove the offset of the input stage transistors so that a matched pair does not have to be used. The differential preamplifier achieves temperature-compensated operation, within a few percent, over the entire $-55°C$ to $+125°C$ temperature range without the use of emitter degeneration resistors. This is an advantage in that degenera-tion resistors deteriorate common mode rejection and give non-optimum high frequency character-istics. The gain of the preamplifier, and therefore the equivalent input-referred threshold voltage, are most conveniently set by adjusting R_7.

The circuit as shown in Figure 4 has a sense threshold of 5 mV. Both the input stage and the dual comparator circuit provide common mode rejection. The response of the sense amplifier to a 10 mV input signal is shown in Figure 5; this can be improved by operating the preamplifier stage at a higher current than the nominal 1 mA in the indicated design.

A number of sense lines can be combined into a single sense amplifier using a circuit similar to that in Figure 4. Individual differential amplifiers and compensated current sources are used for each sense line. These differential amplifiers are com-bined into a single set of load resistors. If more than two (or possibly three) differential amplifiers are used, the inductor, L_1, should be removed, and a pair of inductors should be connected across the load resistors, R_1 and R_2, to prevent excessive DC voltage drop across them.
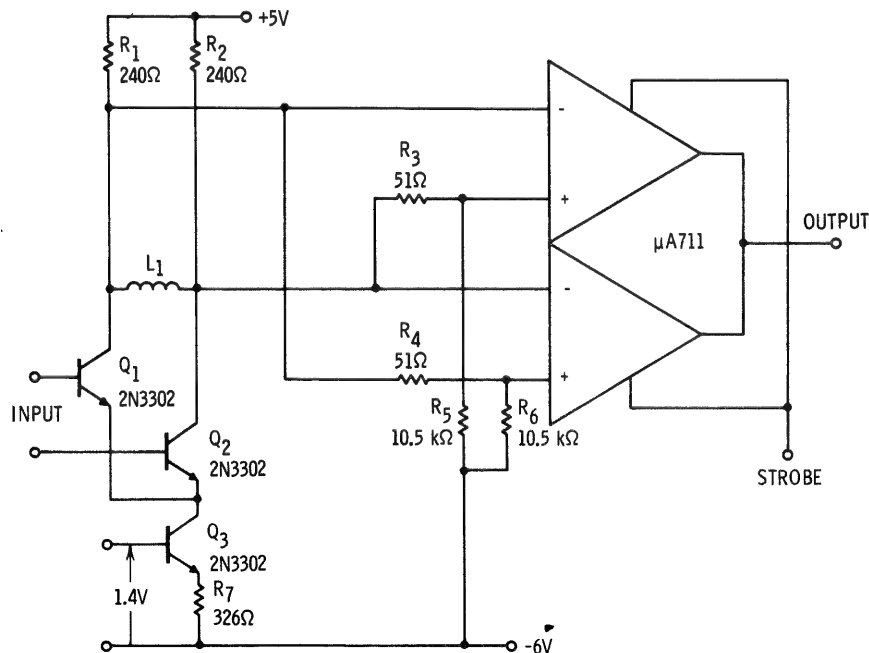
Fig. 4 Sense Amplifier Circuit Using Temperature Compensated Preamplifier for Increased Threshold Sensitivity.
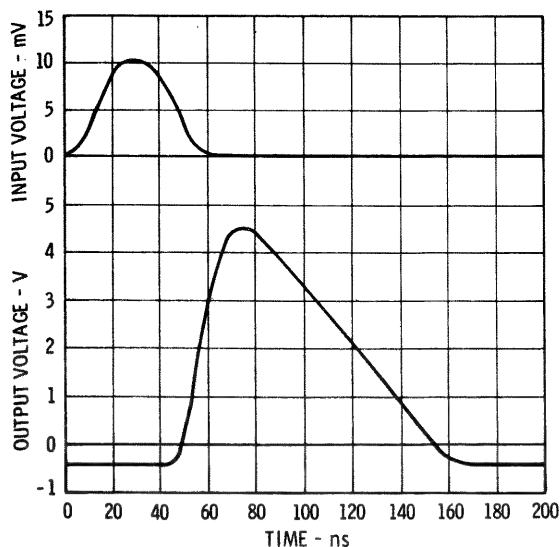
Fig. 5 Response to 10 mV Input Pulse for 5 mV Threshold.

In the design of a memory, it is sometimes convenient to gate a number of sense lines into a single sense amplifier. A circuit which accomplishes this is shown in Figure 6. Differential preamplifiers are employed on each sense line, and are operated from a single temperature-compensated current source. The digital gate signal is applied to the center tap on the line termination resistors. The differential pair that has the highest input common mode signal will operate, while the remainder will be cut off since their emitter-base junctions will be reverse-biased. The common-collector outputs of the preamplifiers are fed to a μA711 connected as a sense amplifier as shown in Figure 4.

If the inductor in Figure 4 is used with the front end in Figure 6, the circuit should be gated on for a long time (as compared to the time constant of the inductor and the collector load resistors) before trying to read. This is required to settle out the collector current imbalance caused by offset between the differential transistors. The inductor, however, can be eliminated if matched input transistors (2N3729) are used, and if the offset of the input transistors is small by comparison to the desired threshold.

The logic drive circuitry should present a low impedance to the center tap on the line termination resistors so that an excessive common mode signal is not developed. The gain of the preamplifiers and, therefore, the threshold setting are best adjusted by varying the emitter resistance in the current source as shown in Figure 6.
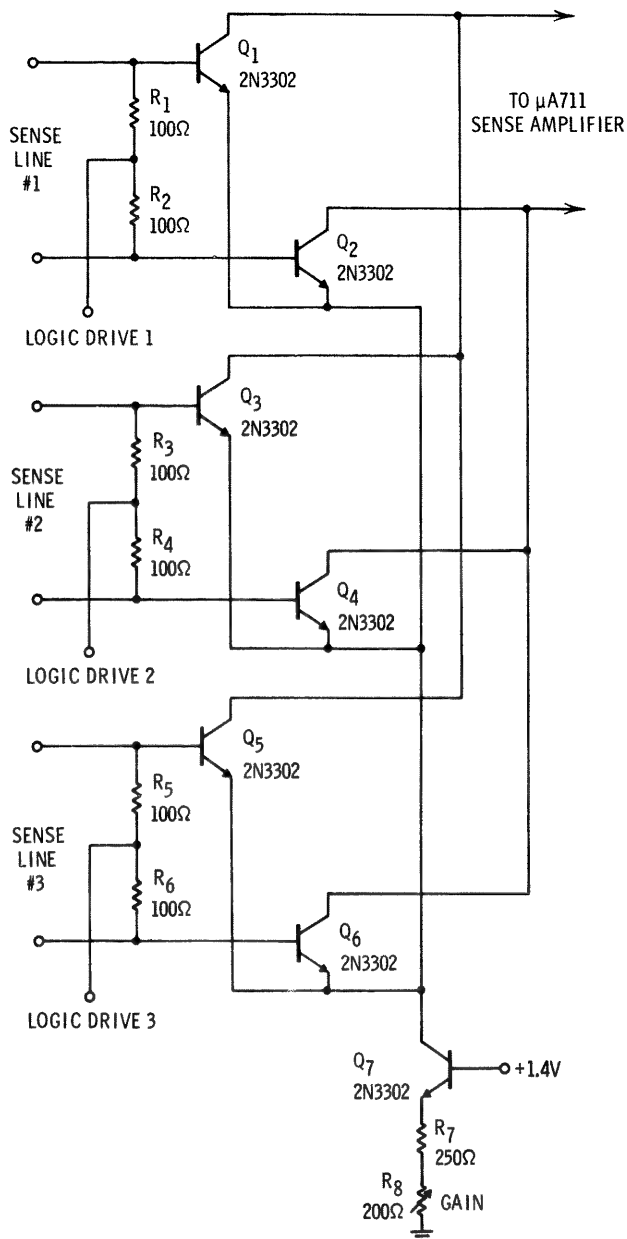
Fig. 6 Three-Channel Gated Preamplifier for Sense Amplifier.

Certain types of memories (i.e., bias or non-destructive read) give an output of one polarity for a "1" and an output of the opposite polarity for a "0". In these applications, one-half of the μA711 can be used as a sense amplifier. No resistor network need be employed on the input to determine threshold since the comparator alone is designed to detect zero crossing. The complete μA711 can be used as a dual sense amplifier with common outputs, which can be separated (as far as the system logic is concerned) by using the independent strobe terminals. A circuit for this is shown in Figure 7.

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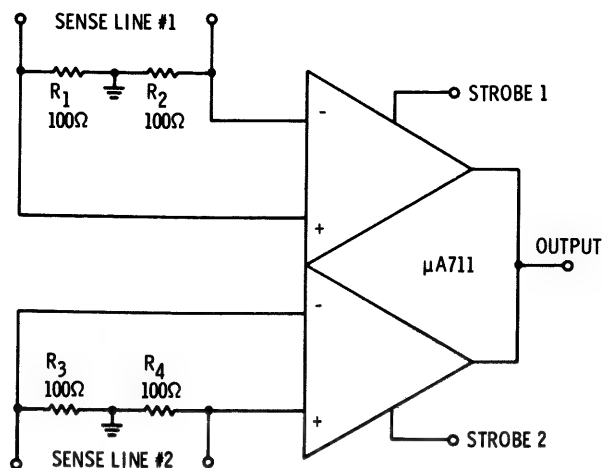
Fig. 7 Dual Sense Amplifier for Positive-One,
Negative-Zero Memory Systems.

Most often with positive "1", negative "0" memories, the output pulse amplitude is comparable to the offset of the μA711. In this case, the circuit in Figure 7 cannot be used alone. A preamplifier with AC coupling must be used to amplify the signal to a level that can be detected easily by the μA711. A circuit for doing this is shown in Figure 8. It is similar to the preamplifier in Figure 4 except that

no attempt is made to control the gain since its actual magnitude is unimportant as long as it is high enough. As with the circuit in Figure 4, the inductors remove the offset of the preamplifier transistors so that matched pairs do not have to be used. Since the preamplifier shown has a gain of 10, the circuit will be able to discriminate a zero crossing within 0.5 mV.

In many military systems, it is desirable to hold the sense amplifier dissipation to a minimum to lower power consumption, or because of heat removal problems associated with high packing densities. If this is the case, power supply strobing can be used with the μA711 to reduce power consumption from the typical $130mW$ to about 40 mW per package. A circuit for doing this is shown in Figure 9. The positive supply voltage is strobed from $+5V$ in the non-operating state to $+12V$ for operation. With $+5V$ and $-6V$ supply voltages, the input and output stages of the comparator function in the normal manner (for zero output), and only the second stage is affected. As a result, neither the sense lines nor the logic circuits on the output are disturbed by lowering the positive supply. When the positive supply is applied, the sense amplifier
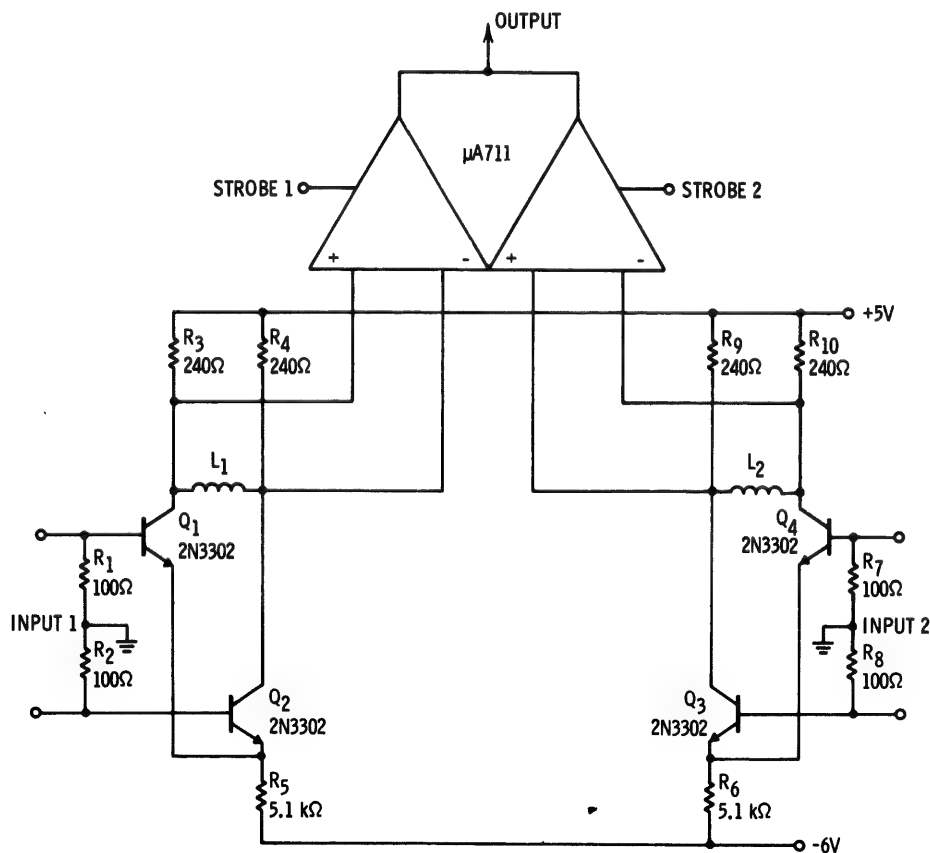
Fig. 8 Dual Sense Amplifier for Positive-One, Negative-Zero Memory Systems Including Preamplifiers.

stabilizes and is ready to function within 30 *ns*; no perturbations are sent out on the sense line. The supply strobing must be employed along with the strobe on the usual terminal because a feedthrough pulse of approximately 10 *ns* width will come through the sense amplifier even with an input "0" if the output strobe terminal is not held down. Normally, the supplies can be strobed along with the core drivers, and the output strobe terminal can be driven after the usual delay required for the sense line to settle down.

The circuit in Figure 9 provides a simple way of accomplishing supply strobing. This circuit is capable of driving at least ten sense amplifiers. With a logic "0" input to Q_1, Q_2 is cut off and the zener diode determines the low-state, positive input to the sense amplifiers. When the logic signal is applied, Q_1 turns on, applying full voltage to the circuits. The speed-up capacitor, C_1, assists in rapid turn-on. The turn-off is not too rapid because

of the storage time of Q_2, but this is usually of little significance as the sense amplifier can be quieted by using the output strobe terminal.
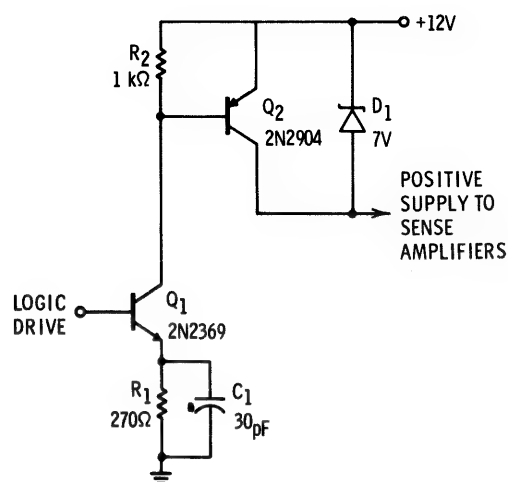
Fig. 9 Positive-Supply Strobe Circuit.

The purpose of a data sheet is to specify the performance and limitations of the integrated circuit in as complete a manner as possible so that the device may be used with confidence by the circuit designer in his application. All Fairchild linear integrated circuit data sheets follow the same format: the front page begins with a brief description of the circuit and its intended applications, followed by a listing of maximum ratings, circuit schematic, pin connections, and package outline.

ABSOLUTE MAXIMUM RATINGS

The figures given in the maximum ratings indicate the levels beyond which the useful life of the device may be impaired. In other words, if the limits are exceeded, there is no guarantee that the device will continue to operate, meet specifications, or even survive.

Most of the terms specified are standard and easily understood (supply voltage, peak current, temperature extremes, etc.).

However, some misunderstanding may exist concerning the specifications on differential input voltage, input voltage, and power dissipation. Differential input voltage is applicable to those circuits having a differential input stage, and is the maximum voltage that may be applied *between* the two input terminals. Input voltage, on the other hand, is the maximum voltage that may be applied between either input and ground.

Power dissipation is the maximum power that may be dissipated within the device for any condition of power supply, output level, or loading. This rating may change with temperature, depending upon the package type and temperature

range. If so, the appropriate derating factors are given in a footnote; the reciprocal of the $mW/°C$ derating factor is the package thermal resistance.

PRODUCT CODE

Included with each package outline drawing on the data sheet is a 10-digit part number. When ordering a particular device, this code should always be given, since it specifies the basic device, the package, and the grade. The meaning of the digits and their position are as follows:

I. Generic Device Type: U5 B 7 709 31 X
For microcircuits, this digit is always "U".

II. Package Designation: U 5B 7 709 31 X

This consists of two digits, a number followed by a letter. The package designations used for linear circuits are:

- 3A - 1/4″ × 1/8″, metal flat pack, 10-lead
- 3G - 1/4″ × 1/4″, ceramic flat pack, 10-lead
- 3H - 1/4″ × 1/4″, glass flat pack, 10-lead
- 5B - metal TO-99, 8-lead configuration
- 5D - metal TO-99, 8-lead configuration, but with leads 2 and 6 missing
- 5F - metal TO-100, 10-lead
- 5J - metal TO-5, 10-lead
- 6E - epoxy, 14 lead dual in line package
- 8B - epoxy, 8-lead configuration, but with leads 2 and 6 missing

III. Microcircuit type code: U 5B 7 709 31 X
For linear circuits, this number is always "7".

IV. Device number: U 5B 7 <u>709</u> 31 X

These are the popular numbers generally used when referring to a device: $\mu A709$, $\mu A703$, etc.*

V. Grade designation: U 5B 7 709 <u>31</u> X

These two numbers define the operating temperature range. Present designations are:

31 - Operating temperature range of −55°C. to +125°C.

39 - Operating temperature range of 0°C. to +70,C.

32 - Operating temperature range of 0°C to +85°C.

VI. Extra Digit: U 5B 7 709 31 <u>X</u>

This space is reserved for special designation. For standard devices, this is an "X". In some cases, this digit is used to indicate special electrical performance classifications:

1 - High performance military
2 - Standard military
3 - Ground-based military and Industrial/Computer
4 - Consumer

ELECTRICAL CHARACTERISTICS AND PERFORMANCE

The second page of the data sheet gives a table of guaranteed electrical characteristics. All special test conditions are specified for each device parameter, along with the guaranteed minimum and maximum limits that will be obtained from the production distribution of units. The most critical parameters are also specified over the operating temperature range. Definitions for each term can be found on the back of the data sheet.

The remainder of the data sheet consists of performance curves, showing the typical behavior of the device as a function of temperature, supply voltage, frequency, etc. In some cases, the curves may also be used to indicate maximum or minimum guaranteed limits.

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*Some confusion has existed concerning the $\mu A702A$ designation. This arose because the design of the original $\mu A702$ (UXX7702XXX) amplifier was improved after introduction (in particular, an additional connection was brought out to increase the versatility of the device). The improvement required a new designation − $\mu A702A$ − the "A" suffix indicating that the device was a plug-in replacement for the $\mu A702$, but with improved characteristics. The internal product code for the improved circuit then became UXX7712XXX because of the lack of a digit space for the "A" in the 10-digit numbering system.This decision has caused much confusion when ordering the device. Since there is now no requirement for the old device ($\mu A702$), the product code for the $\mu A702A$ has been changed back to UXX7702XXX in order to be consistent with all other products.

FAIRCHILD
LINEAR
INTEGRATED
CIRCUITS

1967

µA702A
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **2500 MINIMUM VOLTAGE GAIN**
- **10 µV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The µA702A is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 Volts to −6.0 V
Internal Power Dissipation	
TO-99 [Note 1]	300 mW
Flat Package [Note 2]	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B770231X†

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)
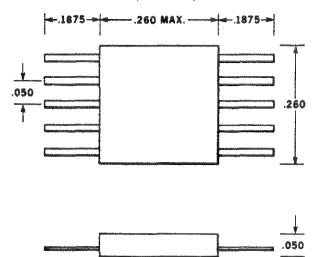
ORDER PART NO. U3H770231X

SCHEMATIC DIAGRAM

TO-99 CONNECTION DIAGRAM (TOP VIEW)

Note: Pin 4 connected to case.
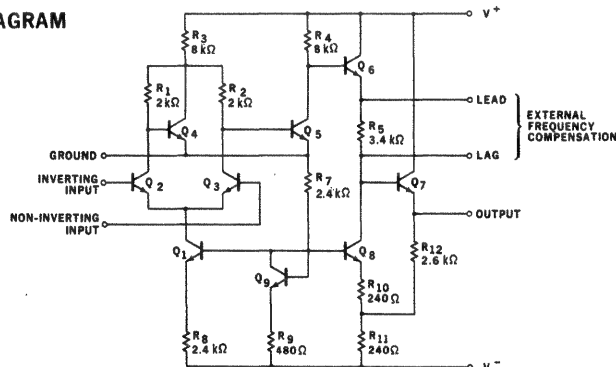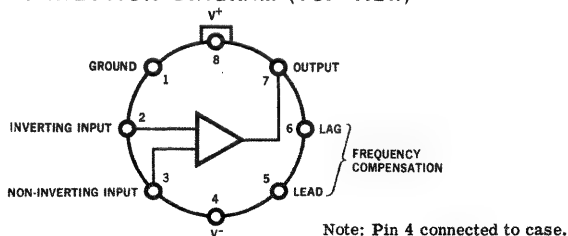
FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)
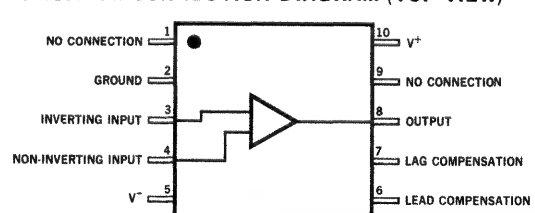
Notes on page 2

* Planar is a patented Fairchild process.
† Equivalent to U5B771231X and U3H771231X

FAIRCHILD
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A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	$V^+ = 12.0\,V, V^- = -6.0\,V$ MIN.	TYP.	MAX.	$V^+ = 6.0\,V, V^- = -3.0\,V$ MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 2\,k\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_s \leq 2\,k\Omega$, $f \leq 1\,kHz$	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100\,k\Omega$, $V_{out} = \pm5.0\,V$	2500	3600	6000				
	$R_L \geq 100\,k\Omega$, $V_{out} = \pm2.5\,V$				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0.01\,\mu F$, $R_1 = 20\,\Omega$, $R_L \geq 100\,k\Omega$, $V_{in} = 10\,mV$							
Risetime			25	120				ns
Overshoot	$C_L \leq 100\,pF$		10	50				%
Transient Response (×100 gain)	$C_3 = 50\,pF$, $R_L \geq 100\,k\Omega$, $V_{in} = 1\,mV$							
Risetime			10	30				ns
Overshoot			20	40				%

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 2\,k\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s = 50\,\Omega$, $T_A = 25°C$ to $T_A = +125°C$		2.5	10		3.5	15	μV/°C
	$R_s = 50\,\Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125°C$		80	500		50	500	nA
	$T_A = -55°C$		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55°C$		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_s \leq 2\,k\Omega$, $f \leq 1\,kHz$	70	95		70	95		dB
Supply Voltage Rejection Ratio	$V^+ = 12\,V$, $V^- = -6\,V$ to $V^+ = 6\,V$, $V^- = -3\,V$ $R_s \leq 2\,k\Omega$		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\,k\Omega$, $V_{out} = \pm5.0\,V$	2000		7000				
	$R_L \geq 100\,k\Omega$, $V_{out} = \pm2.5\,V$				500		1750	
Output Voltage Swing	$R_L \geq 100\,k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\,k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

TRANSIENT RESPONSE TEST CIRCUITS

UNITY-GAIN AMPLIFIER (LAG COMPENSATION)

X100 AMPLIFIER (LEAD COMPENSATION)

TRANSIENT RESPONSE

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

µA702B
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 µV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The µA702B is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For improved specifications, see µA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V⁺ and V⁻ Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55° C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

ORDER PART NO.
U3H7702313

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

(TOP VIEW)
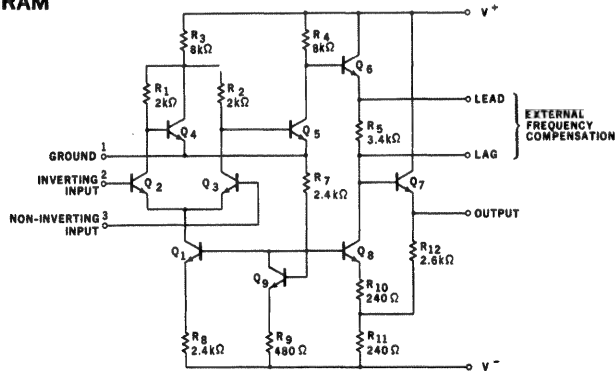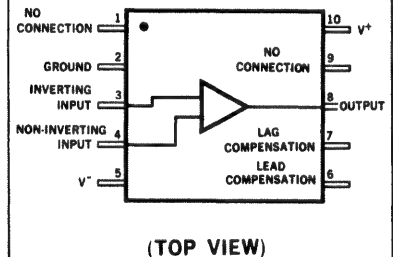
NOTE 1: Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	V$^+$ = 12.0 V, V$^-$ = −6.0 V MIN.	TYP.	MAX.	V$^+$ = 6.0 V, V$^-$ = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	R$_s$ ≤ 2 kΩ		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	R$_s$ ≤ 2 kΩ, f ≤ 1 kHz	70	92		70	92		dB
Large-Signal Voltage Gain	R$_L$ ≥ 100 kΩ, V$_{out}$ = ±5.0 V	2000	3400	6000				
	R$_L$ ≥ 100 kΩ, V$_{out}$ = ±2.5 V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	V$_{out}$ = 0		5.0	6.7		2.1	3.3	mA
Power Consumption	V$_{out}$ = 0		90	120		19	30	mW
Transient Response (unity gain)	C$_i$ = 0.01 μF, R$_i$ = 20Ω R$_L$ ≤ 100 kΩ, V$_{in}$ = 10 mV							
Risetime			25	120				ns
Overshoot	C$_L$ ≤ 100 pF		10	50				%
Transient Response (×100 gain)	C$_3$ = 50 pF, R$_L$ ≥ 100 kΩ, V$_{in}$ = 1 mV							
Risetime			10	30				ns
Overshoot			20	40				%

The following specifications apply for 0°C ≤ T$_A$ ≤ +70°C:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	R$_s$ ≤ 2 kΩ			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	R$_s$ = 50 Ω, T$_A$ = +70°C to T$_A$ = 0°C		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	T$_A$ = 25°C to T$_A$ = +70°C		4.0	10		3.0	8.0	nA/°C
	T$_A$ = 25°C to T$_A$ = 0°C		6.0	20		5.5	18	nA/°C
Input Bias Current	T$_A$ = 0°C		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	R$_s$ ≤ 2 kΩ, f ≤ 1 kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	V$^+$ = 12 V, V$^-$ = 6 V to V$^+$ = 6 V, V$^-$ = 3 V R$_s$ ≤ 2 kΩ		90	300		90	300	μV/V
Large-Signal Voltage Gain	R$_L$ ≥ 100 kΩ, V$_{out}$ = ±5.0 V	1500		7000				
	R$_L$ ≥ 100 kΩ, V$_{out}$ = ±2.5 V				400		1750	

The following specifications apply for −55°C ≤ T$_A$ ≤ +125°C:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	R$_S$ ≤ 2 kΩ			7.5			8.0	mV
Input Offset Current	T$_A$ = +125°C		0.2	2.0		0.14	2.0	μA
	T$_A$ = −55°C		1.2	4.0		0.8	4.0	μA
Input Bias Current	T$_A$ = −55°C		5.5	20		3.4	15	μA
Input Resistance		3.0			4.0			kΩ
Common Mode Rejection Ratio	R$_S$ ≤ 2 kΩ, f ≤ 1 kHz	60	80		60	80		dB
Large Signal Voltage Gain	R$_L$ ≥ 100 kΩ, V$_{out}$ = ±5.0 V	1200						
	R$_L$ ≥ 100 kΩ, V$_{out}$ = ±2.5 V				300			
Output Voltage Swing	R$_L$ ≥ 100 kΩ	±5.0	±5.3		±2.5	±2.7		V
	R$_L$ ≥ 10 kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current	T$_A$ = +125°C, V$_{out}$ = 0		4.4	6.7		1.7	3.3	mA
	T$_A$ = −55°C, V$_{out}$ = 0		5.0	7.5		2.1	3.9	mA
Power Consumption	T$_A$ = +125°C, V$_{out}$ = 0		80	120		15	30	mW
	T$_A$ = −55°C, V$_{out}$ = 0		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

TRANSIENT RESPONSE TEST CIRCUITS

UNITY-GAIN AMPLIFIER (LAG COMPENSATION)

X100 AMPLIFIER (LEAD COMPENSATION)

TRANSIENT RESPONSE

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)

FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

FREQUENCY COMPENSATION CIRCUITS
(Refer to Fairchild APP-117 for further details)

LAG COMPENSATION

LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION

µA702C
HIGH GAIN, WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- IMPROVED SPECIFICATIONS
- 5 mV MAXIMUM OFFSET VOLTAGE
- 2000 MINIMUM VOLTAGE GAIN
- 20 µV/°C MAXIMUM OFFSET VOLTAGE DRIFT

GENERAL DESCRIPTION — The µA702C is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For full temperature range operation (−55°C to +125°C) see µA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V$^+$ and V$^-$ Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation [Note 1]	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B770239X

SCHEMATIC DIAGRAM

TO-99 CONNECTION DIAGRAM

(TOP VIEW)

NOTE: Pin 4 connected to can.
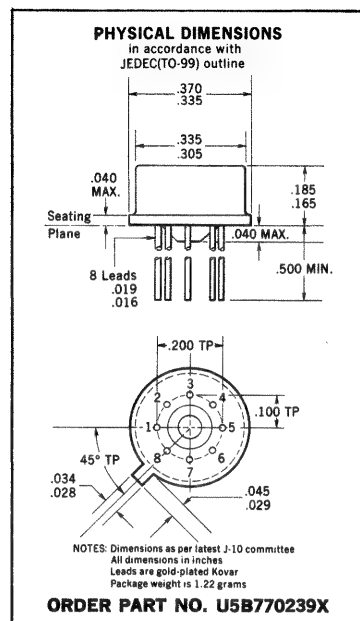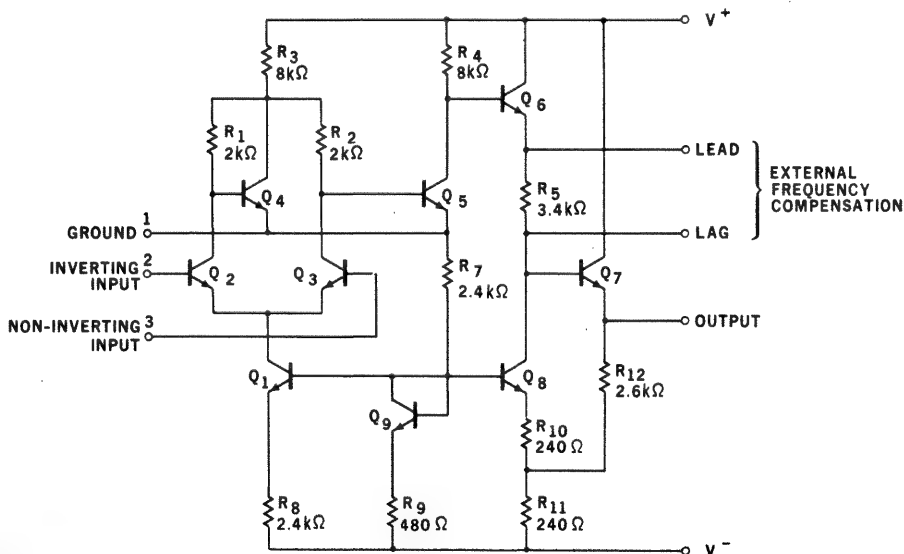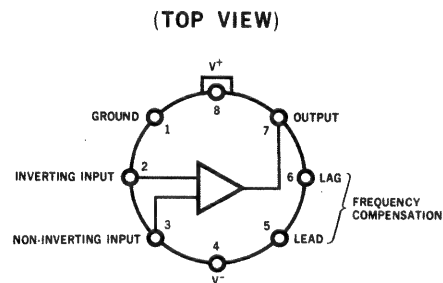
NOTES:
(1) Rating applies for ambient temperatures to +70°C.
(2) For Flat Package see µA702B data sheet.

* Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	$V^+ = 12.0\,V, V^- = -6.0\,V$ MIN.	TYP.	MAX.	$V^+ = 6.0\,V, V^- = -3.0\,V$ MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 2\,k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		$k\Omega$
Input Voltage Range		-4.0		$+0.5$	-1.5		$+0.5$	V
Common Mode Rejection Ratio	$R_s \leq 2\,k\Omega$, $f \leq 1\,kHz$	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\,k\Omega$, $V_{out} = \pm 5.0\,V$	2000	3400	6000				
	$R_L \geq 100\,k\Omega$, $V_{out} = \pm 2.5\,V$				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_i = 0.01\,\mu F$, $R_i = 20\Omega$ $R_L \leq 100\,k\Omega$, $V_{in} = 10\,mV$							
Risetime			25	120				ns
Overshoot	$C_L \leq 100\,pF$		10	50				%
Transient Response ($\times 100$ gain)	$C_3 = 50\,pF$, $R_L \geq 100\,k\Omega$, $V_{in} = 1\,mV$							
Risetime			10	30				ns
Overshoot			20	40				%

The following specifications apply for $0°C \leq T_A \leq +70°C$:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 2\,k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s = 50\,\Omega$, $T_A = +70°C$ to $T_A = 0°C$		5.0	20		7.5	25	$\mu V/°C$
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		4.0	10		3.0	8.0	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0°C$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		$k\Omega$
Common Mode Rejection Ratio	$R_s \leq 2\,k\Omega$, $f \leq 1\,kHz$	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12\,V$, $V^- = 6\,V$ to $V^+ = 6\,V$, $V^- = 3\,V$ $R_s \leq 2\,k\Omega$		90	300		90	300	$\mu V/V$
Large-Signal Voltage Gain	$R_L \geq 100\,k\Omega$, $V_{out} = \pm 5.0\,V$	1500		7000				
	$R_L \geq 100\,k\Omega$, $V_{out} = \pm 2.5\,V$				400		1750	
Output Voltage Swing	$R_L \geq 100\,k\Omega$	± 5.0	± 5.3		± 2.5	± 2.7		V
	$R_L \geq 10\,k\Omega$	± 3.5	± 4.0		± 1.5	± 2.0		V
Supply Current	$V_{out} = 0$		5.0	7.0		2.1	3.9	mA
Power Consumption	$V_{out} = 0$		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE
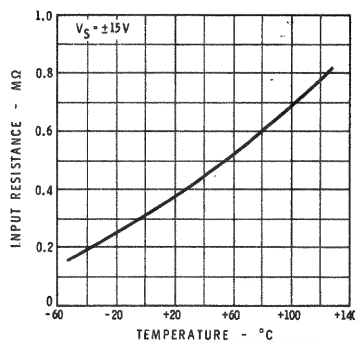

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

### COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

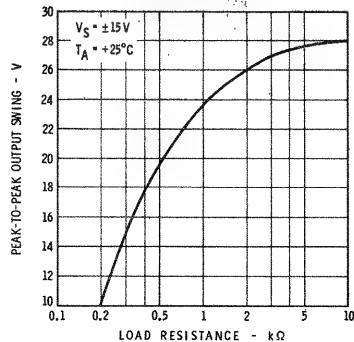

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

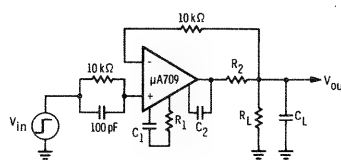
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

TRANSIENT RESPONSE TEST CIRCUITS

UNITY-GAIN AMPLIFIER (LAG COMPENSATION)

X100 AMPLIFIER (LEAD COMPENSATION)

TRANSIENT RESPONSE

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

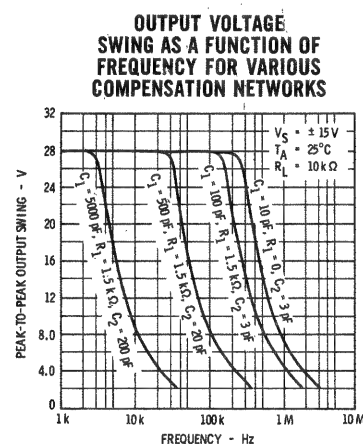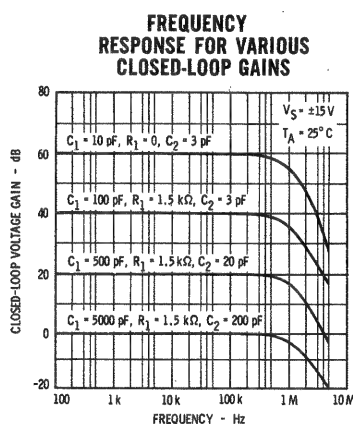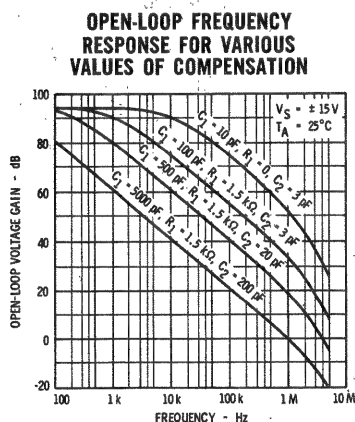OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

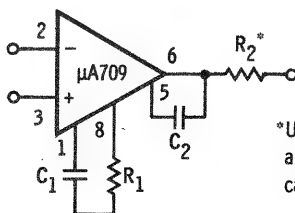TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

FREQUENCY RESPONSE FOR
VARIOUS CLOSED-LOOP GAINS
(LAG COMPENSATION)

FREQUENCY RESPONSE
WITH CONSERVATIVE
COMPENSATION NETWORK

FREQUENCY RESPONSE FOR
VARIOUS CLOSED-LOOP GAINS
(LEAD-LAG COMPENSATION)

OUTPUT VOLTAGE SWING
AS A FUNCTION OF
FREQUENCY FOR VARIOUS
LAG COMPENSATION NETWORKS

FREQUENCY COMPENSATION CIRCUITS
(Refer to Fairchild APP-117 for further details)

LAG
COMPENSATION

LEAD-LAG
COMPENSATION

OUTPUT VOLTAGE SWING
AS A FUNCTION OF FREQUENCY
WITH LEAD-LAG COMPENSATION

GENERAL DESCRIPTION - The µA703 is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or nonlimiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 seconds)	300°C

PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-99 outline)
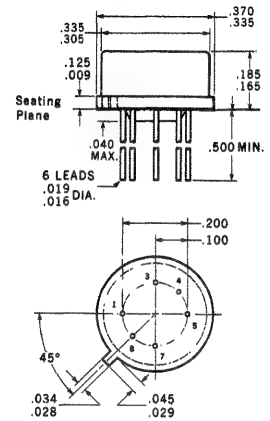
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.27 grams

ORDER PART NO. U5D770331X

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

(TOP VIEW)

V+
DECOUPLING
OUTPUT
INPUT HIGH
INPUT LOW
GROUND

NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 125°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	$e_{in} = 0$		110	170	mW
Quiescent Output Current	$e_{in} = 0$	2.1	2.5	3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	4.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f $\leq$ 1kHz	29	35		mmho
Input Conductance	e_{in} < 10 mV rms, f $\leq$ 5 MHz		0.30	0.43	mmho
Input Capacitance	e_{in} < 10 mV rms, f $\leq$ 5 MHz		7.0	16.0	pF
Output Capacitance	f $\leq$ 5 MHz		2.0	3.0	pF
Output Conductance	$e_o \leq$ 100mVrms, f $\leq$ 5MHz		0.02	0.04	mmho
Noise Figure	f = 30 MHz, R_s = 500 Ω		6.5		dB
	f = 100 MHz, R_s = 500 Ω		8.0		dB

The following specifications apply for -55°C $\leq T_A \leq$ +125°C

Parameter	Conditions	Min.	Typ.	Max.	Units
Quiescent Output Current	$e_{in} = 0$	1.7		3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f $\leq$ 1kHz	21			mmho
Input Conductance	e_{in} < 10 mV rms, f $\leq$ 5 MHz			1.2	mmho
Output Conductance	$e_o \leq$ 100mVrms, f $\leq$ 5MHz			0.05	mmho

TYPICAL PERFORMANCE CURVES

INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE

INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

TYPICAL PERFORMANCE CURVES

MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

TRANSADMITTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

DEFINITION OF TERMS

POWER CONSUMPTION - The DC power required to operate the device with no signal applied.

QUIESCENT OUTPUT CURRENT - The DC current delivered to the load with the input terminals short-circuited.

PEAK-TO-PEAK OUTPUT CURRENT - The short-circuit output current excursion for a large-signal input voltage.

OUTPUT SATURATION VOLTAGE - The minimum voltage to which the output collector may be reduced without degrading circuit performance.

TRANSADMITTANCE - The ratio of the output current to the input voltage.

INPUT ADMITTANCE - The admittance between the input terminals with the output short-circuited.

OUTPUT ADMITTANCE - The admittance between the output terminals with the input short-circuited.

GENERAL DESCRIPTION - The μA703C is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device. For full range operation (-55°C to +125°C) see μA703 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 second)	300°C

PHYSICAL DIMENSIONS
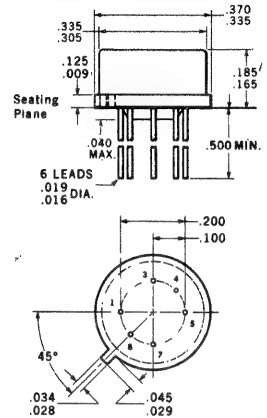
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.?? grams

ORDER PART NO. U5D770339X

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

(TOP VIEW)

NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 70°C.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	$e_{in} = 0$		110	170	mW
Quiescent Output Current	$e_{in} = 0$	1.9	2.5	3.3	mA
Peak-to-Peak Output Current	$e_{in} = 400$ mV rms, f = 1 kHz	3.6			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	$e_{in} = 10$ mV rms, f $\leq$ 1kHz	23	33		mmho
Input Conductance	$e_{in} < 10$ mV rms, f $\leq$ 5 MHz		0.35	0.50	mmho
Input Capacitance	$e_{in} < 10$ mV rms, f $\leq$ 5 MHz		9.0	16.0	pF
Output Capacitance	f $\leq$ 5 MHz		2.0	3.0	pF
Output Conductance	$e_o \leq 100$mVrms, f $\leq$ 5MHz			0.05	mmho
Noise Figure	f = 30 MHz, $R_s = 500$ Ω		6.5		dB
	f = 100 MHz, $R_s = 500$ Ω		8.0		dB

The following specifications apply for $0°C \leq T_A \leq 70°C$:

Parameter	Conditions	Min.	Typ.	Max.	Units
Quiescent Output Current	$e_{in} = 0$	1.7		3.5	mA
Peak-to-Peak Output Current	$e_{in} = 400$ mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	$e_{in} = 10$ mV rms f $\leq$ 1kHz	22			mmho
Input Conductance	$e_{in} < 10$ mV rms, f $\leq$ 5 MHz			0.71	mmho
Output Conductance	$e_o \leq 100$mVrms, f $\leq$ 5MHz			0.06	mmho

TYPICAL PERFORMANCE CURVES
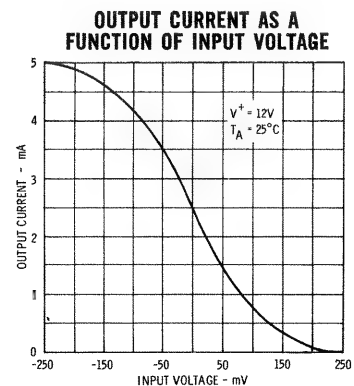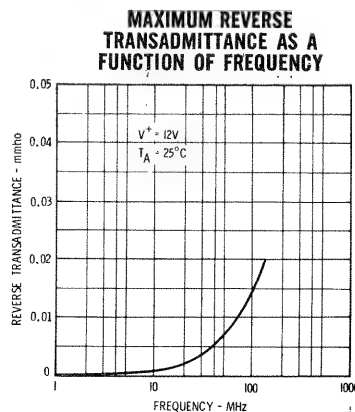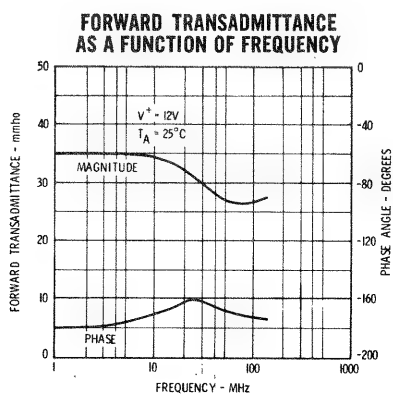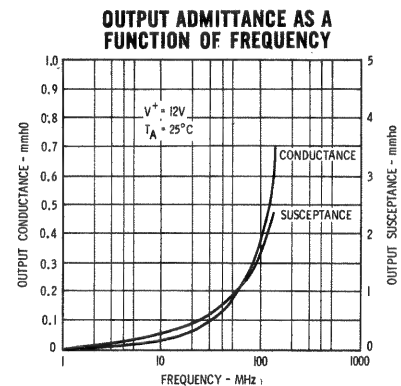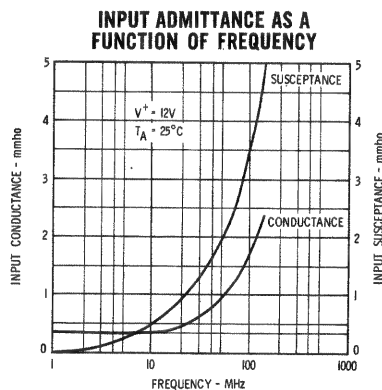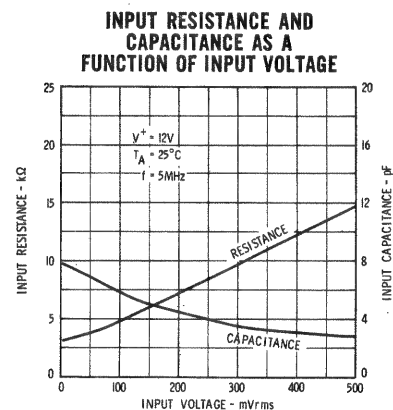
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE

INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

GENERAL DESCRIPTION - The µA703E is a linear integrated circuit with useful unneutralized power gain to frequencies in excess of 100 MHz. It features the capability of nonsaturating limiter operation with a suitable output load, making it ideally suited for FM–IF limiter applications.

Applications include FM–IF limiter–amplifier, TV sound IF amplifier, chroma reference oscillator for color TV, and fixed–gain amplifiers to 100 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (Soldering - 10 seconds)	260°C

PHYSICAL DIMENSIONS

EPOXY PACKAGE

.325 MAX. DIA.

.240 MAX.

.500 MIN.

Ceramic

6 LEADS
.019 .016 DIA.

.200

.100

45°

FLAT
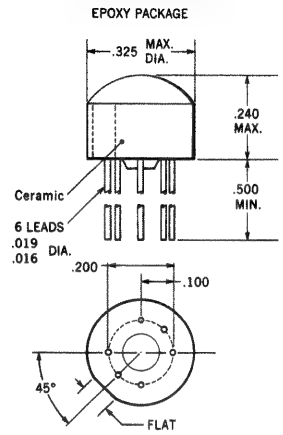
NOTES: All dimensions in inches
Leads are gold-plated nickel
Package weight is 0.31 gram

ORDER PART NO. U8B770339X

SCHEMATIC DIAGRAM
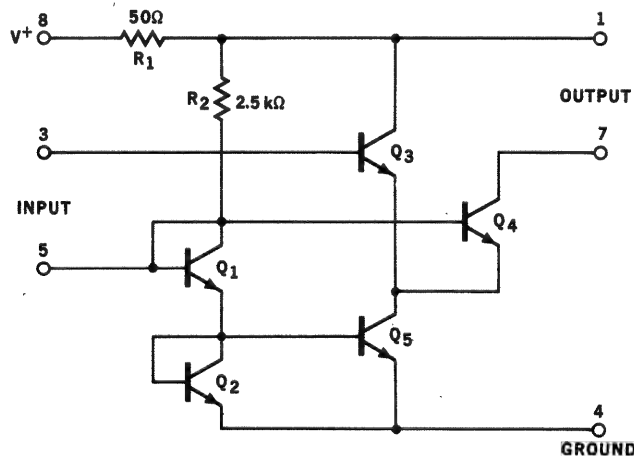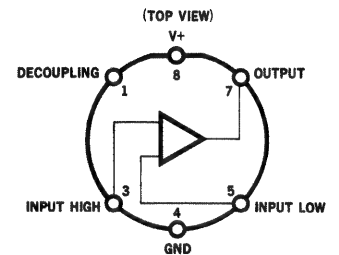
CONNECTION DIAGRAM

(TOP VIEW)

NOTE 1: Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C, V$^+$ = 12 V, f = 10.7 MHz unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current			2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms	3.0	5.0		mA
Output Saturation Voltage			1.4	1.7	Volts
Forward Transadmittance	e_{in} = 10 mV rms	24	35		mmhos
Reverse Transadmittance			0.002		mmho
Input Conductance	e_{in} < 10 mV rms		.33	1.0	mmho
Input Capacitance	e_{in} < 10 mV rms		9.0	18.0	pF
Output Conductance			0.03	0.05	mmho
Output Capacitance			2.6	4.0	pF
Noise Figure	R_S = 500 Ω		6.0		dB
	R_S = 500 Ω, f = 100 MHz		8.0		dB
Maximum Stable Gain			40		dB

TYPICAL PERFORMANCE CURVES

INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE
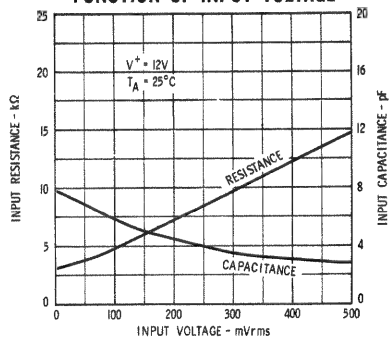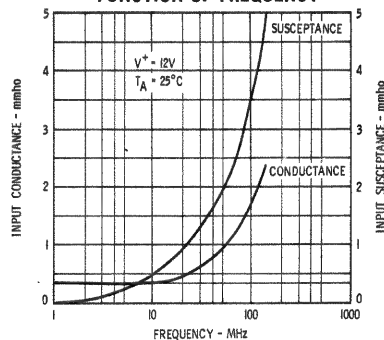
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY
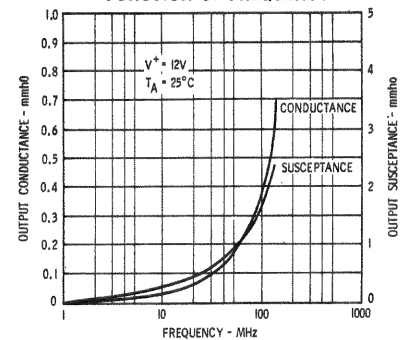
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY
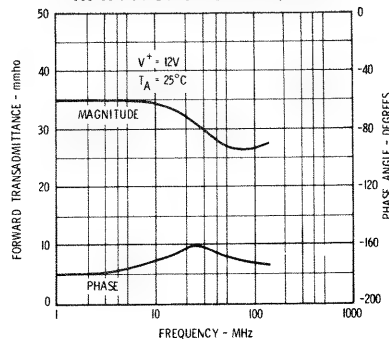
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY
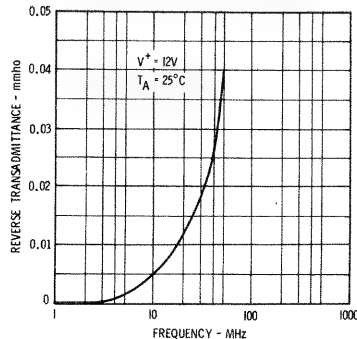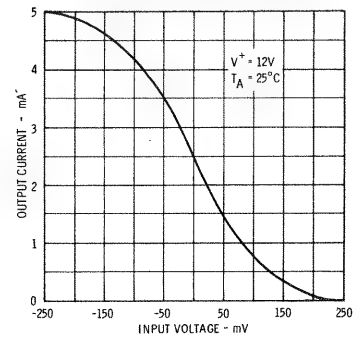
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

TYPICAL CIRCUIT APPLICATIONS

COLOR TV SOUND-IF AMPLIFIER

PERFORMANCE
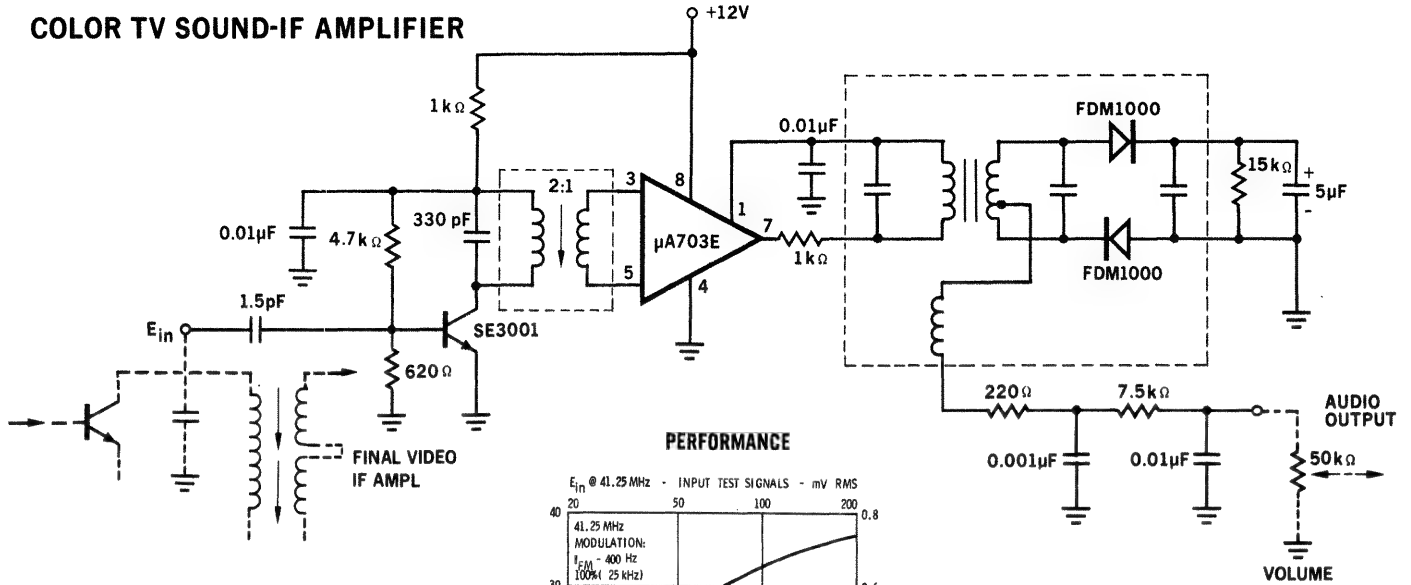
3.58-MHz VOLTAGE-CONTROLLED OSCILLATOR
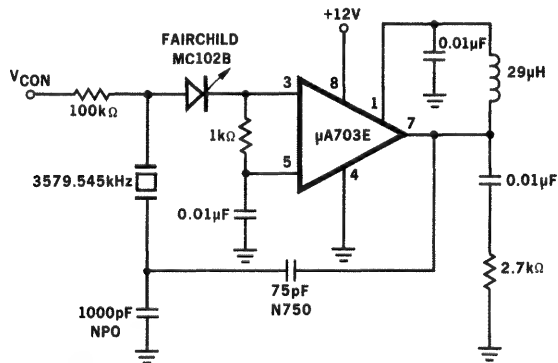
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE
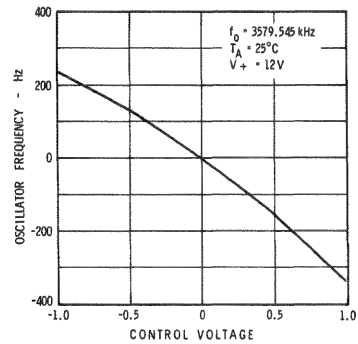
NORMALIZED OSCILLATOR FREQUENCY AND OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE

3.58-MHz INJECTION-LOCKED OSCILLATOR

NORMALIZED PHASE SHIFT AS A FUNCTION OF NORMALIZED OSCILLATOR FREQUENCY

NORMALIZED OSCILLATOR FREQUENCY AND OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE

FOUR-STAGE FM-IF AMPLIFIER

Full limiting with $V_{in} < 50 \mu V$.

Current consumption 27 mA.

Power gain / stage 26.5 dB.

Peak-to-Peak separation of detector 800 kHz.

THD $< 0.8\%$ with ± 75 kHz deviation @ 400 Hz.
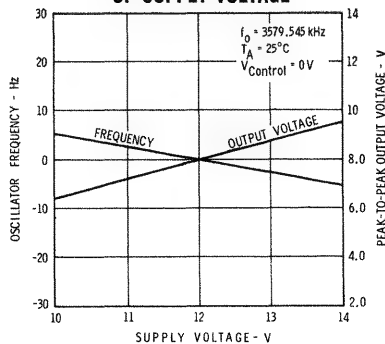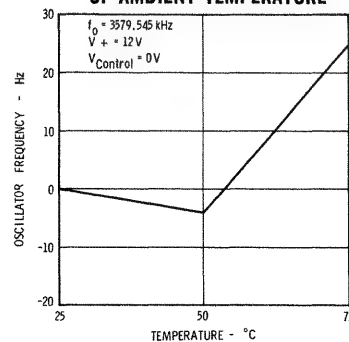
μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTIONS - The μA709 is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

ABSOLUTE MAXIMUM RATINGS

|	
Supply Voltage	± 18 V
Internal Power Dissipation TO-99 (Note 1)	300 mW
Dual-In-Line	300 mW
Differential Input Voltage	± 5.0 V
Input Voltage	± 10 V
Output Short-Circuit Duration (T_A = 25°C)	5 sec
Storage Temperature Range	-65°C to + 150°C
Operating Temperature Range	-55°C to + 125°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches
Dimensions as per latest J-10 committee
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B770931X

CONNECTION DIAGRAMS

(Top View)

NOTE: Pin 4 connected to case.
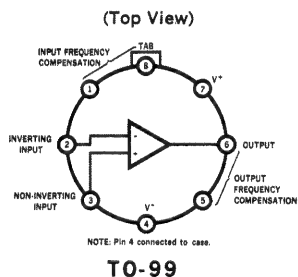
TO-99
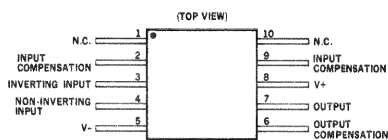
FLAT-PAK

SCHEMATIC DIAGRAM
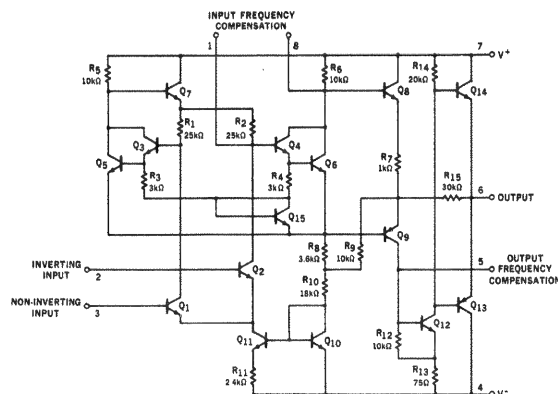
TYPICAL FLAT PACKAGE
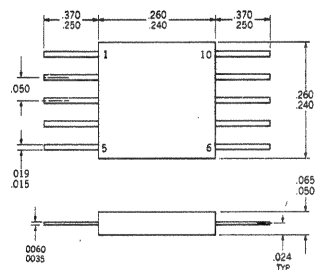
NOTES: All dimensions in inches

ORDER PART NO. U3F770931X

NOTES:
1. Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.
2. Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +30°C.

FAIRCHILD

SEMICONDUCTOR

A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ± 9 V $\leq V_S \leq \pm 15$ V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		kΩ
Output Resistance			150		Ω
Power Consumption	$V_S = \pm 15$ V		80	165	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ,				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ,		0.3	1.0	μs
	$C_2 = 200$ pF, $R_2 = 50$ Ω				
Overshoot	$C_L \leq 100$ pF		10	30	%

The following specifications apply for -55°C $\leq T_A \leq$ +125°C:

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Large-Signal Voltage Gain	$V_S = \pm 15$ V, $R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000	45,000	70,000	
Output Voltage Swing	$V_S = \pm 15$ V, $R_L \geq 10$ kΩ	± 12	± 14		V
	$V_S = \pm 15$ V, $R_L \geq 2$ kΩ	± 10	± 13		V
Input Voltage Range	$V_S = \pm 15$ V	± 8.0	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	150	μV/V
Input Offset Current	$T_A = +125$°C		20	200	nA
	$T_A = -55$°C		100	500	nA
Input Bias Current	$T_A = -55$°C		0.5	1.5	μA
Input Resistance		40	100		kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

VOLTAGE GAIN

OUTPUT VOLTAGE SWING
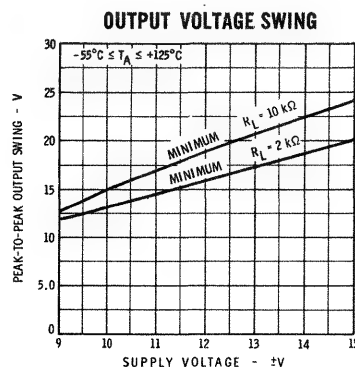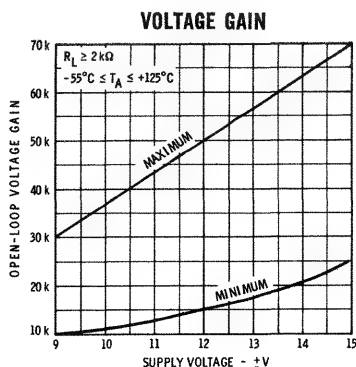
GUARANTEED ELECTRICAL CHARACTERISTICS (CONT'D)

INPUT COMMON MODE VOLTAGE RANGE
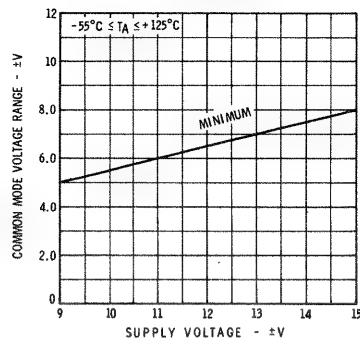
POWER CONSUMPTION
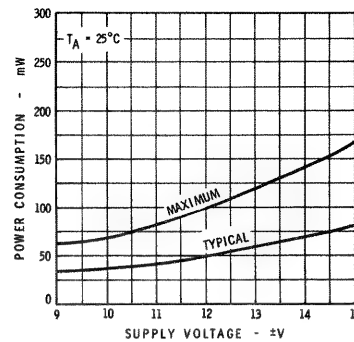
TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC
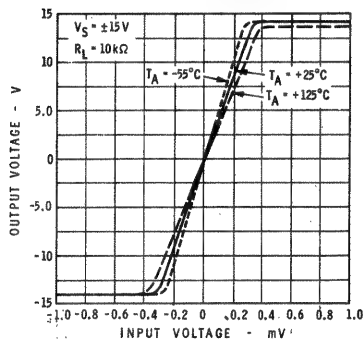
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE
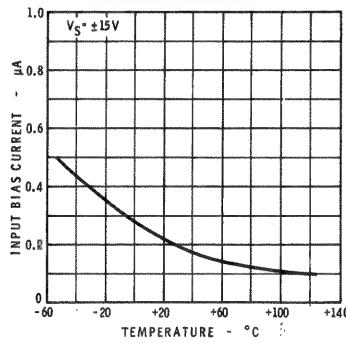
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE
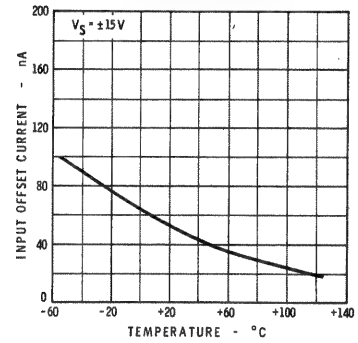
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE
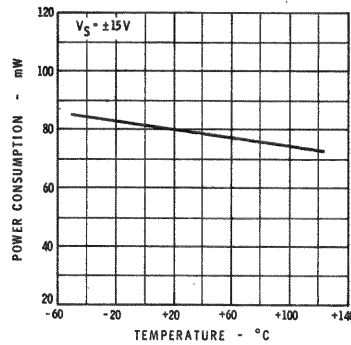
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
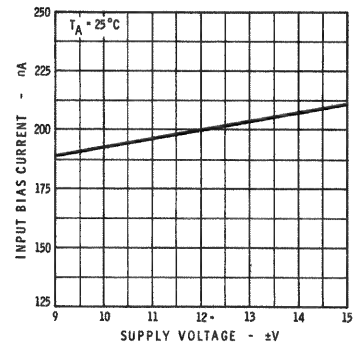
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

TRANSIENT RESPONSE TEST CIRCUIT

TRANSIENT RESPONSE

6-28

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

FREQUENCY COMPENSATION CIRCUIT

*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

µA709A
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **2 mV MAXIMUM OFFSET VOLTAGE**
- **50 nA MAXIMUM OFFSET CURRENT**
- **GUARANTEED DRIFT CHARACTERISTICS**

GENERAL DESCRIPTION — The µA709A is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a 14-36 V range of total supply voltage with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, low-level instrumentation applications, and for the generation of special linear and nonlinear transfer functions. Although it features improved performance, the µA709A is a direct plug-in replacement for the µA709 operational amplifier.

ABSOLUTE MAXIMUM RATINGS

|	
Total Supply Voltage	36 V
Internal Power Dissipation TO-99 (Note 1)	300 mW
Flat Package (Note 2)	300 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = +25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS

in accordance with
JEDEC(TO-99) outline
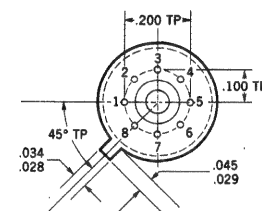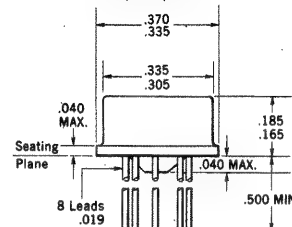
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7709311

CONNECTION DIAGRAMS

(Top View)
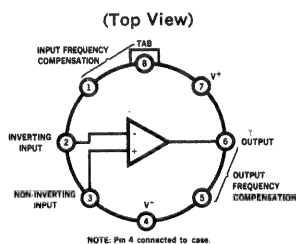
NOTE: Pin 4 connected to case.

TO-5
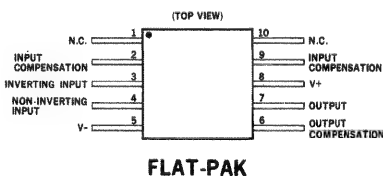
FLAT-PAK

SCHEMATIC DIAGRAM
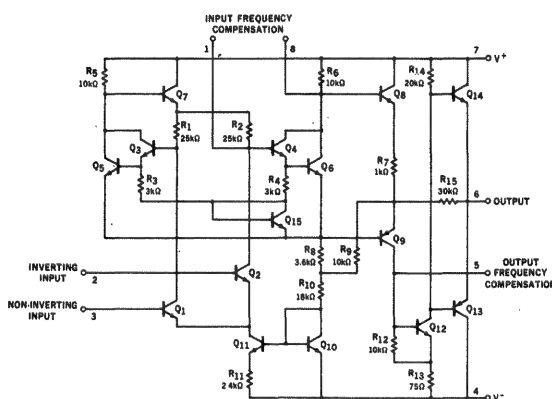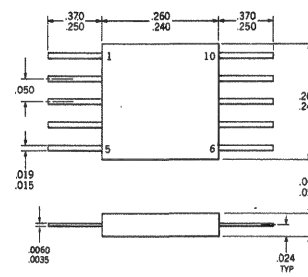
FLAT PACKAGE

NOTES: All dimensions in inches

ORDER PART NO. U3F7709311

*Planar is a patented Fairchild process.

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.
(2) Rating applies for case temperatures to +125°C; derate linearly for ambient temperatures above +30°C.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9\,V \leq V_S \leq \pm 15\,V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		0.6	2.0	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		$k\Omega$
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\,V$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\,V$		75	108	mW
Transient Response	$V_S = \pm 15\,V$, $V_{in} = 20\,mV$, $R_L = 2\,k\Omega$, $C_1 = 5\,nF$, $R_1 = 1.5\,k\Omega$, $C_2 = 200\,pF$, $R_2 = 50\,\Omega$				
Risetime				1.5	μs
Overshoot	$C_L \leq 100\,pF$			30	%

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

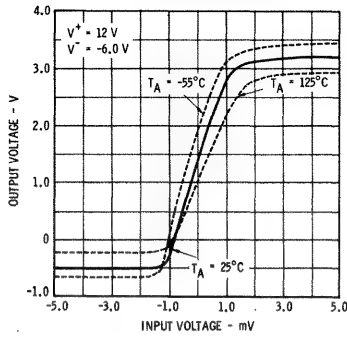| PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\,\Omega$, $T_A = +25°C$ to $T_A = +125°C$		1.8	10	$\mu V/°C$
	$R_S = 50\,\Omega$, $T_A = +25°C$ to $T_A = -55°C$		1.8	10	$\mu V/°C$
	$R_S = 10\,k\Omega$, $T_A = +25°C$ to $T_A = +125°C$		2.0	15	$\mu V/°C$
	$R_S = 10\,k\Omega$, $T_A = +25°C$ to $T_A = -55°C$		4.8	25	$\mu V/°C$
Input Offset Current	$T_A = +125°C$		3.5	50	nA
	$T_A = -55°C$		40	250	nA
Average Temperature Coefficient of Input Offset Current	$T_A = +25°C$ to $T_A = +125°C$		0.08	0.5	nA/°C
	$T_A = +25°C$ to $T_A = -55°C$		0.45	2.8	nA/°C
Input Bias Current	$T_A = -55°C$		300	600	nA
Input Resistance	$T_A = -55°C$	85	170		$k\Omega$
Input Voltage Range	$V_S = \pm 15\,V$	± 8.0			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		40	100	$\mu V/V$
Large-Signal Voltage Gain	$V_S = \pm 15\,V$, $R_L \geq 2\,k\Omega$, $V_{out} = \pm 15\,V$	25,000		70,000	
Output Voltage Swing	$V_S = \pm 15\,V$, $R_L \geq 10\,k\Omega$	± 12	± 14		V
	$V_S = \pm 15\,V$, $R_L \geq 2\,k\Omega$	± 10	± 13		V
Supply Current	$T_A = +125°C$, $V_S = \pm 15\,V$		2.1	3.0	mA
	$T_A = -55°C$, $V_S = \pm 15\,V$		2.7	4.5	mA
Power Consumption	$T_A = +125°C$, $V_S = \pm 15\,V$		63	90	mW
	$T_A = -55°C$, $V_S = \pm 15\,V$		81	135	mW

GUARANTEED ELECTRICAL CHARACTERISTICS
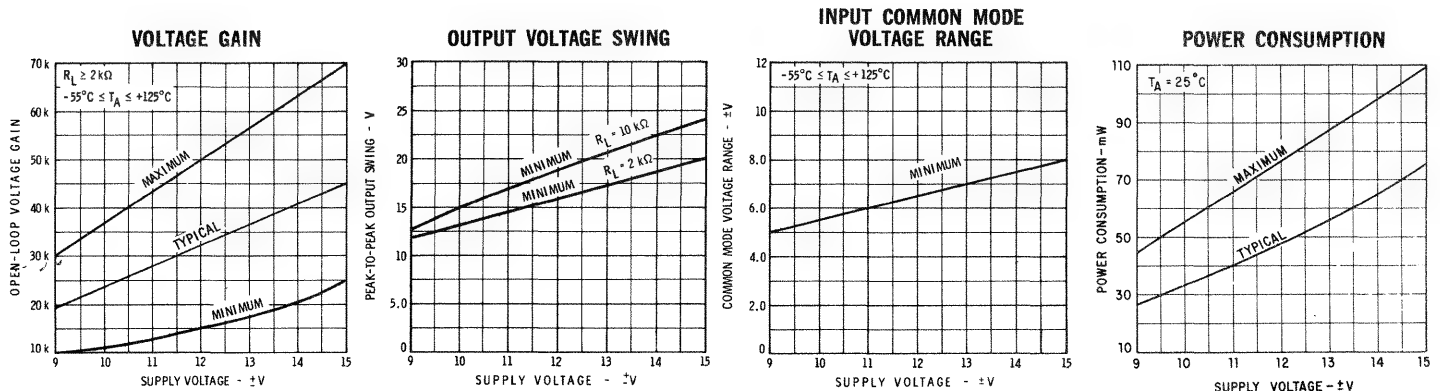
VOLTAGE GAIN

OUTPUT VOLTAGE SWING

INPUT COMMON MODE VOLTAGE RANGE

POWER CONSUMPTION

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC
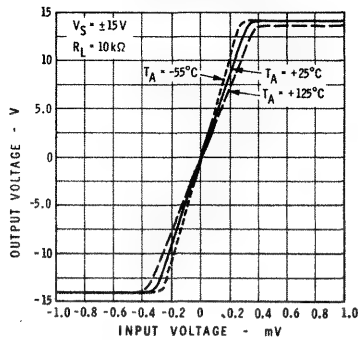
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE
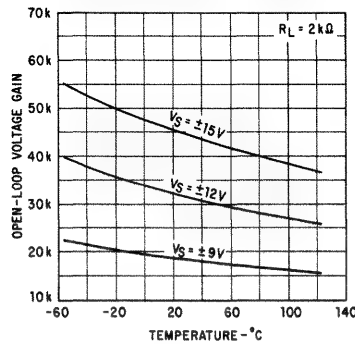
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE
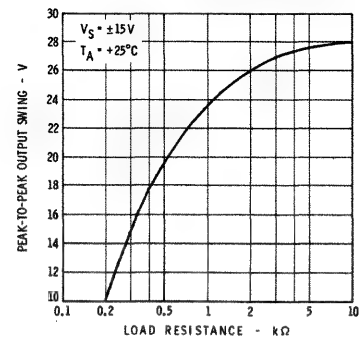
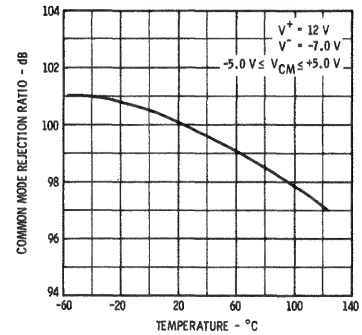### INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE
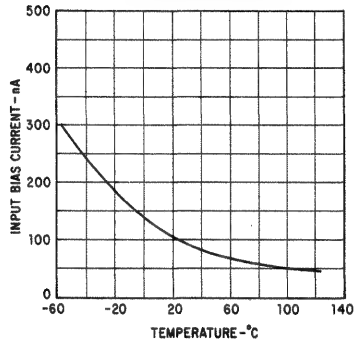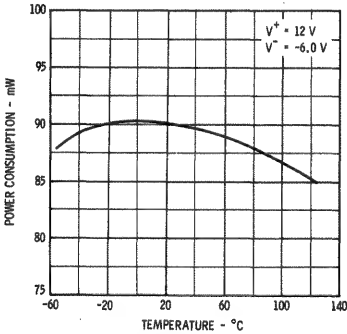
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
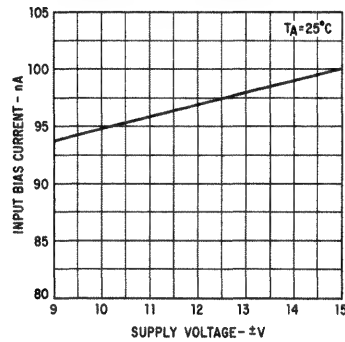
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE
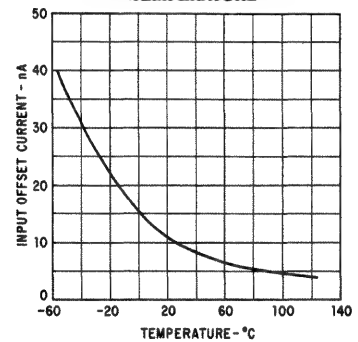
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

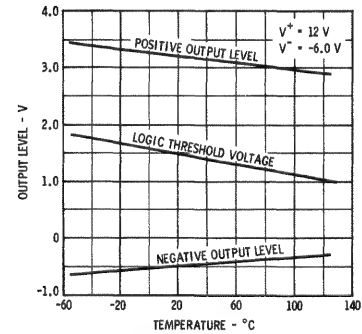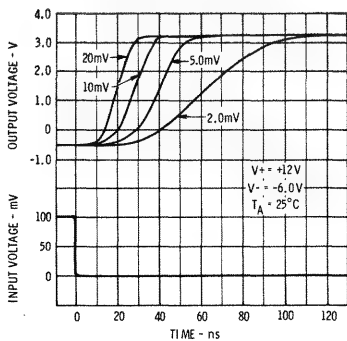### INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE
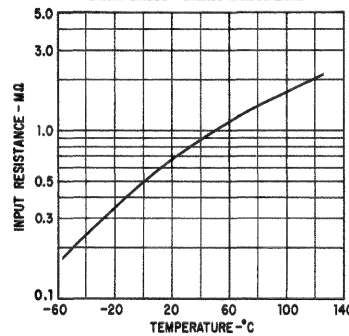
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE
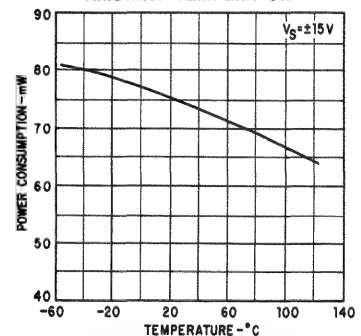
TRANSIENT RESPONSE
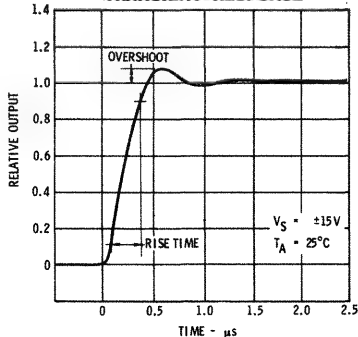
TRANSIENT RESPONSE TEST CIRCUIT
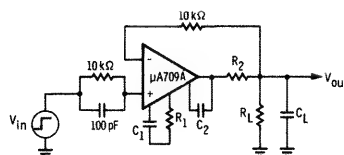
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT·COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

FREQUENCY COMPENSATION CIRCUIT

*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY COMPENSATION CIRCUIT
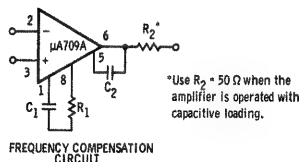
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE
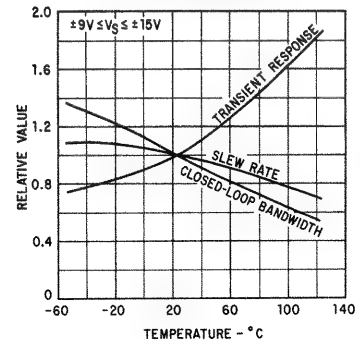
µA709B
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA709B is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For improved specifications, see µA709A or µA709 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration (T_A = 25°C)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
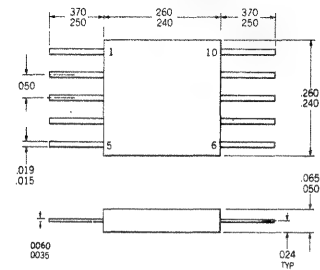
NOTES: All dimensions in inches

ORDER PART NO. U3F7709313

SCHEMATIC DIAGRAM
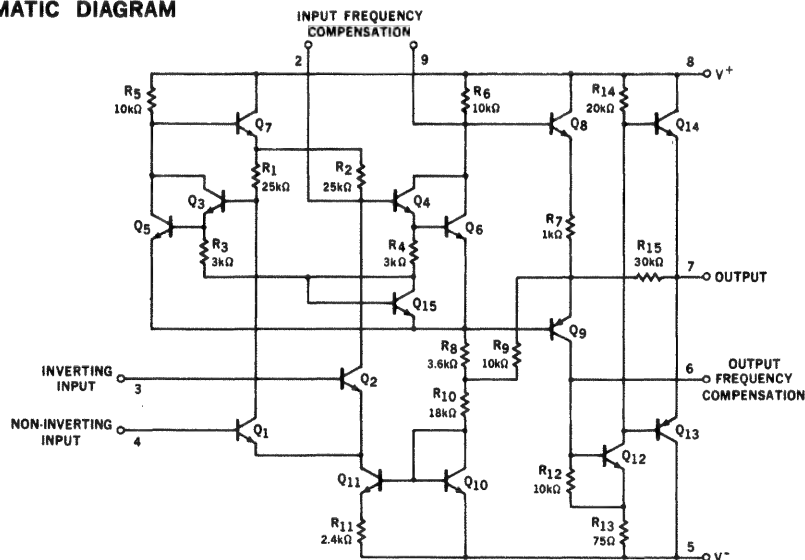
CONNECTION DIAGRAM

*Planar is a patented Fairchild process.

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +60°C.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_S = \pm15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ±9 V $\leq V_S \leq \pm15$ V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm10$ V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ,				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ,		0.3		μs
	$C_2 = 200$ pF, $R_2 = 50$ Ω				
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for 0°C $\leq T_A \leq$ +70°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ±9 V $\leq V_S \leq \pm15$ V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm10$ V	12,000			
Input Resistance		35			kΩ
The following specifications apply for −55°C $\leq T_A \leq$ +125°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ±9 V $\leq V_S \leq \pm15$ V			12.5	mV
Input Offset Current				1.2	μA
Input Bias Current				3.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm10$ V	10,000			

GUARANTEED ELECTRICAL CHARACTERISTICS

VOLTAGE GAIN

OUTPUT VOLTAGE SWING

INPUT COMMON MODE VOLTAGE RANGE

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

FREQUENCY COMPENSATION CIRCUIT

*Use $R_2 = 50$ Ω when the amplifier is operated with capacitive loading.
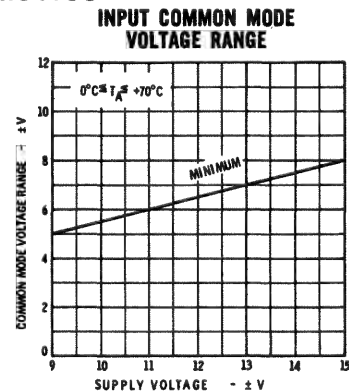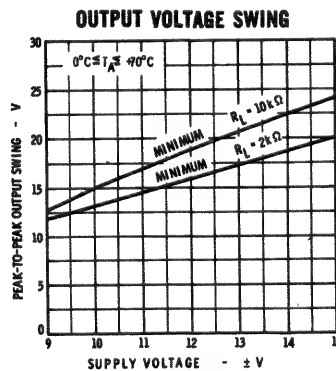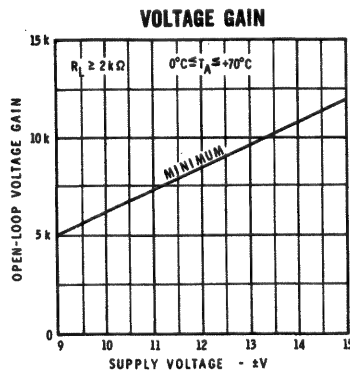
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS
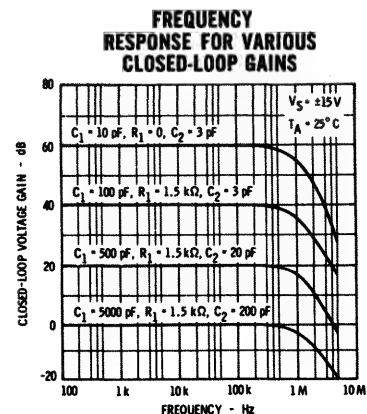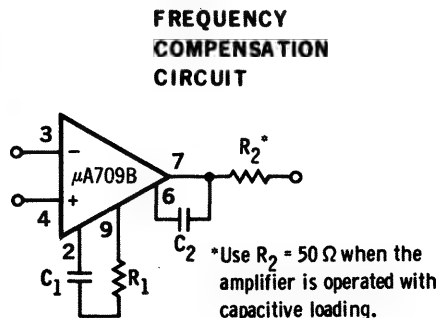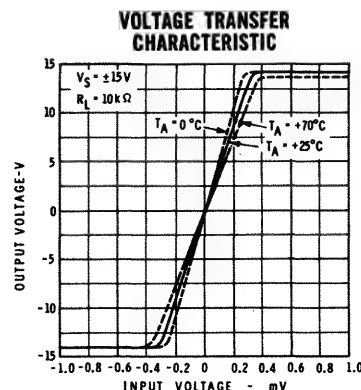
µA709C
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The µA709C is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range operation (-55°C to +125°C) see µA709 or µA709A data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	250 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range TO-99		-65°C to + 150°C
	Dual-In-Line	-55°C to +125°C
Operating Temperature Range		0°C to +70°C
Lead Temperature	TO-99 (Soldering, 60 sec)	300°C
	Dual-In-Line (Soldering, 10 sec)	260°C

PHYSICAL DIMENSIONS
in accordance with JEDEC(TO-99) outline

NOTES. Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B770939X

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

(Top View)

NOTE: Pin 4 connected to case

CONNECTION DIAGRAM

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches

ORDER PART NO.
U6E7709393

NOTE 1: Rating applies for ambient temperatures to +70°C.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15\,V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$, $\pm 9\,V \leq V_S \leq \pm 15\,V$		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	µA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, $V_{out} = \pm 10\,V$	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	± 12	± 14		V
	$R_L \geq 2\,k\Omega$	± 10	± 13		V
Input Voltage Range		± 8.0	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		25	200	µV/V
Power Consumption			80	200	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2\,k\Omega$,				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5\,k\Omega$,		0.3		µs
	$C_2 = 200$ pF, $R_2 = 50\,\Omega$				
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$, $\pm 9\,V \leq \pm 15\,V$			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	µA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{out} = \pm 10\,V$	12,000			
Input Resistance		35			kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

VOLTAGE GAIN

OUTPUT VOLTAGE SWING

INPUT COMMON MODE VOLTAGE RANGE

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

FREQUENCY COMPENSATION CIRCUIT

*Use $R_2 = 50\,\Omega$ when the amplifier is operated with capacitive loading.
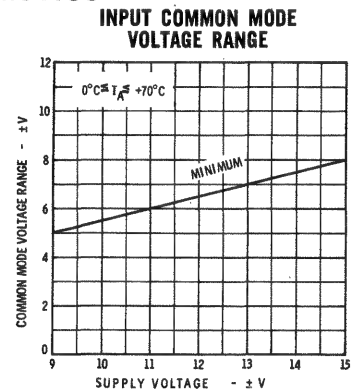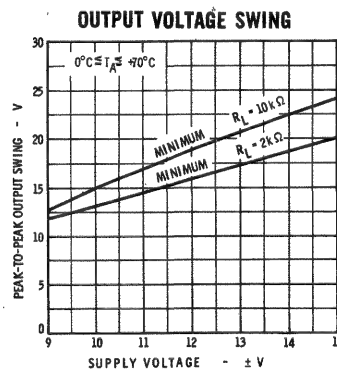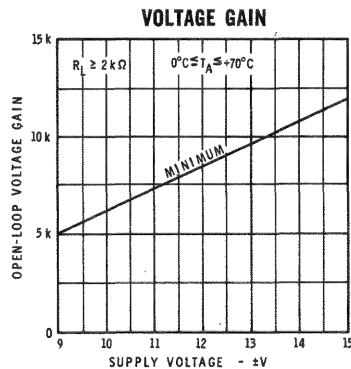
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS
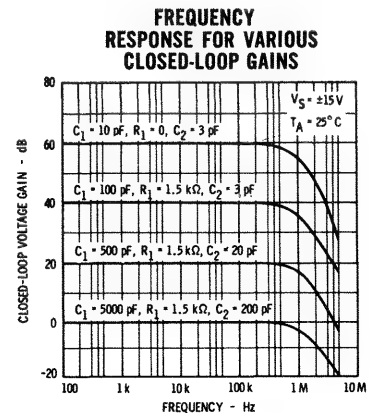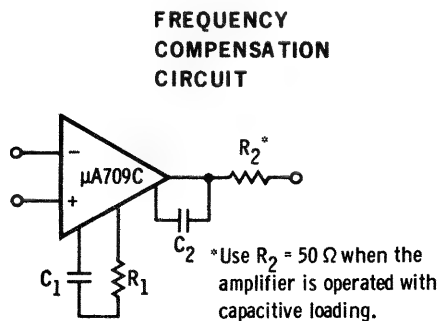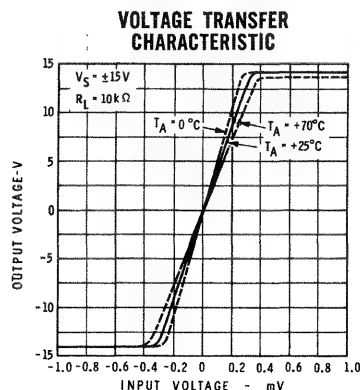
µA710
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- IMPROVED SPECIFICATIONS
- 2 mV MAXIMUM OFFSET VOLTAGE
- 3 µA MAXIMUM OFFSET CURRENT
- 1250 MINIMUM VOLTAGE GAIN
- 10 µV/°C MAXIMUM OFFSET VOLTAGE DRIFT

GENERAL DESCRIPTION — The µA710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation	
TO-99 [Note 1]	300 mW
Flat Package [Note 2]	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B771031X

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

Note: Pin 4 connected to case.

FLAT PACKAGE CONNECTION DIAGRAM
(TOP VIEW)

SCHEMATIC DIAGRAM

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)
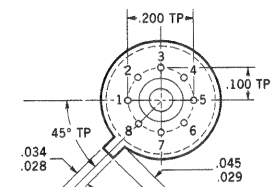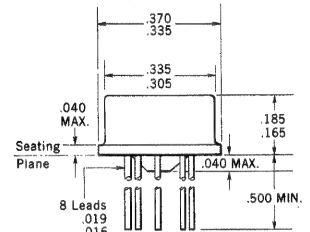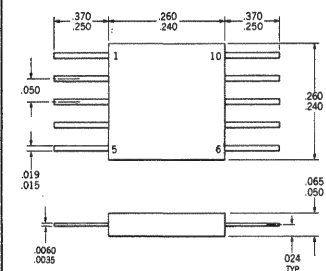
NOTES: All dimensions in inches

ORDER PART NO. U3F771031X

Notes on page 2

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 4)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 200\Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	2.0	2.5		mA
Response Time [Note 3]			40		ns

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 200\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$		3.5	10	μV/°C
	$R_s = 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.7	10	μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		5.0	25	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7.0V$	± 5.0			V
Common Mode Rejection Ratio	$R_s \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		± 5.0			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	-1.0	-0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at -55°C, 1.4V at +25°C and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

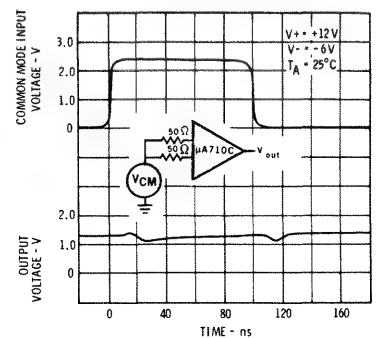### COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

COMMON MODE PULSE RESPONSE

DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.
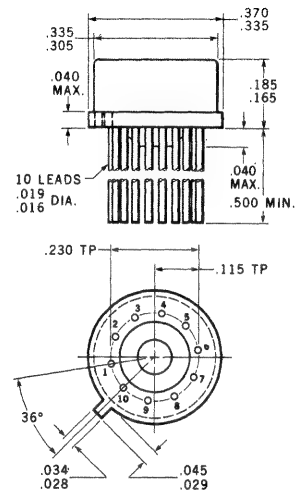
μA710B
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- 5 mV MAXIMUM OFFSET VOLTAGE
- 5 μA MAXIMUM OFFSET CURRENT
- 1000 MINIMUM VOLTAGE GAIN
- 20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT

GENERAL DESCRIPTION — The μA710B is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

For improved specifications, see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

|	
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

NOTES: All dimensions in inches

ORDER PART NO. U3F7710313

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

(TOP VIEW)

*Planar is a patented Fairchild process.

Notes on page 2

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD LINEAR INTEGRATED CIRCUITS μA710B

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\,\Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns

The following specifications apply for $0°C \leq T_A \leq +70°C$:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\,\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\,\Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Voltage Gain		800			
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\,\Omega$			7.5	mV
Input Offset Current	$T_A = +125°C$ $T_A = -55°C$		0.9 3.8	5.0 15	μA μA
Input Bias Current	$T_A = -55°C$		34	80	μA
Input Voltage Range	$V^- = -7.0$ V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\,\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		500			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	-1.0	-0.5	0	V
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:
(1) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.
(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at -55°C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C, and 1.0V at +125°C.
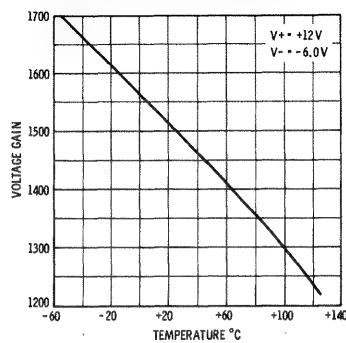
TYPICAL PERFORMANCE CURVES

### VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

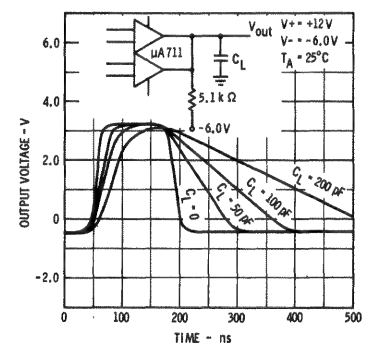### INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

COMMON MODE PULSE RESPONSE

DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

µA710C
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **IMPROVED SPECIFICATIONS**
- **5mV MAXIMUM OFFSET VOLTAGE**
- **5µA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20µV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION— The µA710C is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.
For full temperature range operation (−55°C to +125°C) see µA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation [Note 1]	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range TO-99	−65°C to +150°C
Dual-In-Line	−55°C to +125°C
Lead Temperature TO-99 (Soldering, 60 sec)	300°C
Dual-In-Line (Soldering, 10 sec)	260°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B771039X

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows,
.300 centers

ORDER PART NO.
U6E7710393

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

Note: Pin 4 connected to case

CONNECTION DIAGRAM
(TOP VIEW)

SCHEMATIC DIAGRAM

Notes on page 2

* Planar is a patented Fairchild process

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ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 200\Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5\,mV$, $V_{out} = 0$	1.6	2.5		mA
Response Time [Note 2]			40		ns

The following specifications apply for $0°C \leq T_A \leq +70°C$:

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_s \leq 200\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s = 50\Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_s \leq 200\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{in} \geq 5\,mV$, $0 \leq I_{out} \leq 5.0\,mA$	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5\,mV$	-1.0	-0.5	0	V
Output Sink Current	$\Delta V_{in} \geq 5\,mV$, $V_{out} = 0$	0.5			mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Ratings apply for ambient temperatures to +70°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

COMMON MODE PULSE RESPONSE

DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

GENERAL DESCRIPTION - The µA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The µA711, which is similar to the µA710 differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar*epitaxial process.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	± 5.0 V
Input Voltage	± 7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation TO - 100 (Note 1)	300 mW
Flat-Package (Note 2)	300 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

**ORDER PART NO.
U5F771131X**

CONNECTION DIAGRAM

TO-100

Note: Pin 3 is connected to case.
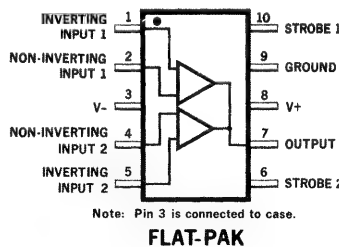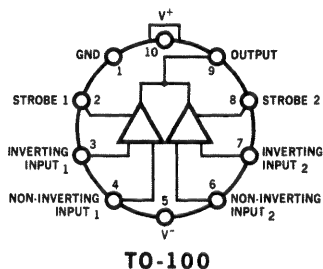
FLAT-PAK

SCHEMATIC DIAGRAM
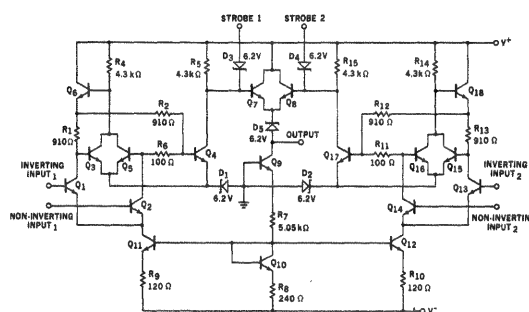
FLAT PACKAGE
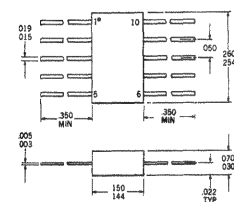
ORDER PART NO. U3T771131X

Notes on page 2

* Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0$ V, $V^- = -6.0$ V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$V_{out} = +1.4$ V, $R_S \leq 200\,\Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$V_{out} = +1.4$ V, $R_S \leq 200\,\Omega$		1.0	5.0	mV
Input Offset Current	$V_{out} = +1.4$ V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 3)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0$ V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{strobe} = 100$ mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW

The following specifications apply for $-55°C \leq T_A \leq +125°C$:

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage (Note 4)	$R_S \leq 200\,\Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 4)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

(2) Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +40°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC
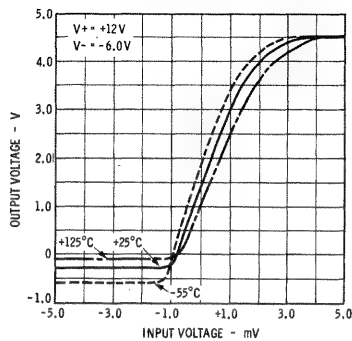
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES
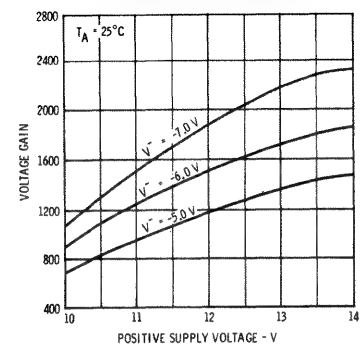
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES
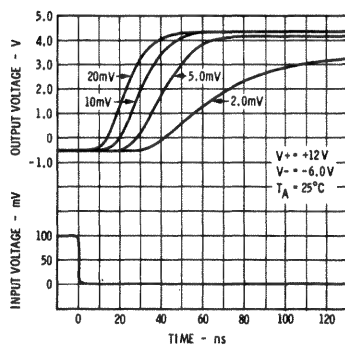
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES
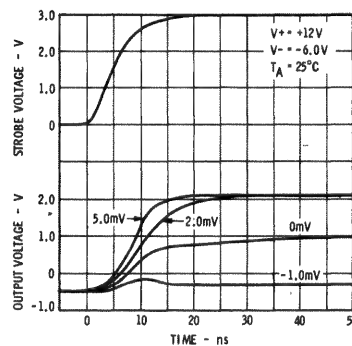
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

COMMON MODE PULSE RESPONSE

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

µA711C
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The µA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The µA711C, which is similar to the µA710C differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar epitaxial process.

For full temperature range operation (-55°C to +125°C) see µA711 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	± 5.0 V
Input Voltage	± 7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation TO - 100 (Note 1)	300 mW
Flat-Package (Note 2)	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline

NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F771139X

CONNECTION DIAGRAMS

TO-100

Note: Pin 3 is connected to case.
FLAT-PAK

SCHEMATIC DIAGRAM

FLAT PACKAGE

ORDER PART NO. U3T771139X

Notes on page 2

* Planar is a patented Fairchild process.

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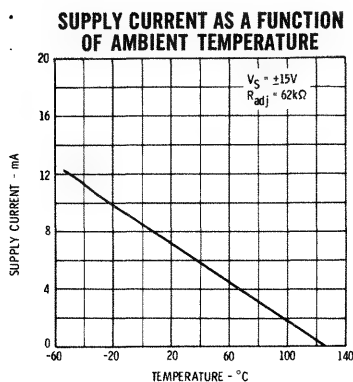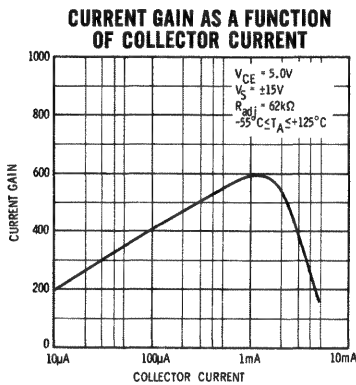313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS   ($T_A = 25°C$, $V^+ = 12.0$ V, $V^- = -6.0$ V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max	Units
Input Offset Voltage	$V_{out} = +1.4$ V, $R_S \leq 200\,\Omega$, $V_{CM} = 0$		1.0	5.0	mV
	$V_{out} = +1.4$ V, $R_S \leq 200\,\Omega$		1.0	7.5	mV
Input Offset Current	$V_{out} = +1.4$ V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 3)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0$ V	± 5.0			V
Differential Input Voltage Range		± 5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{strobe} = 100$ mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW

The following specifications apply for $0°C \leq T_A \leq +70°C$:

Parameter	Conditions	Min.	Typ.	Max	Units
Input Offset Voltage (Note 4)	$R_S \leq 200\,\Omega$, $V_{CM} = 0$			6.0	mV
	$R_S \leq 200\,\Omega$			10	mV
Input Offset Current (Note 4)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage				5.0	μV/°C
Voltage Gain		500			

NOTES:
(1) Rating applies for ambient temperatures to +70°C.
(2) Rating applies for case temperatures to + 70 °C; derate linearly at 2. 5 mW/°C for ambient temperatures above +40°C.
(3) The response time specified is for a 100-mV input step with 5-mV overdrive.
(4) The input offset voltage is specified for a logic threshold voltage of 1.5 V at 0°C, 1.4 V at +25°C and 1.2 V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS
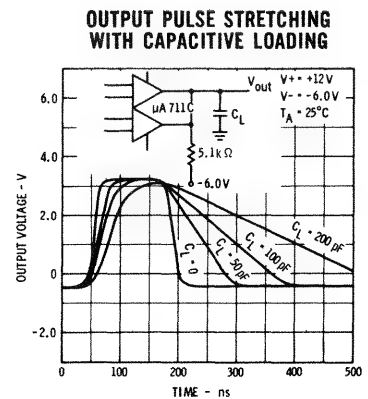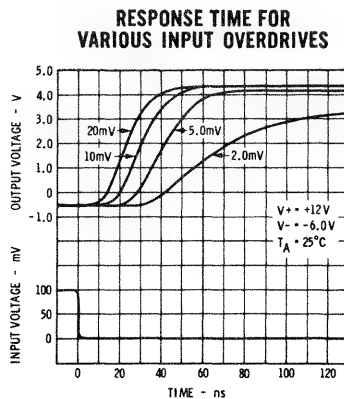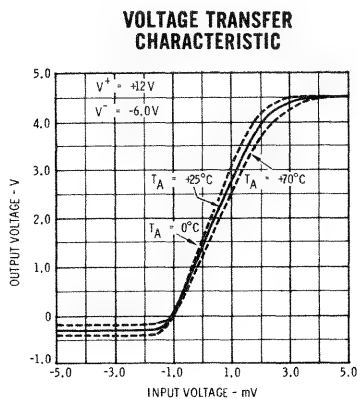
VOLTAGE TRANSFER CHARACTERISTIC

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

µA716
FIXED-GAIN, LOW DISTORTION AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA716 is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or a general-purpose audio preamplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100, and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	27 V
Internal Power Dissipation (Note 1)	400 mW
Input Voltage	± 5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	− 65°C to + 150°C
Operating Temperature Range	− 55°C to + 125°C
Lead Temperature (soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS
similar to
JEDEC(TO-99) outline
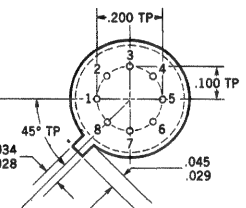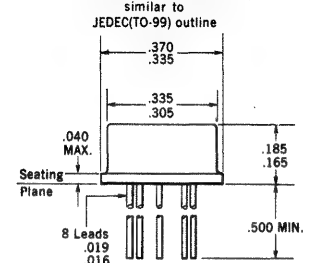
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar

ORDER PART NO. U5K7716312

SCHEMATIC DIAGRAM
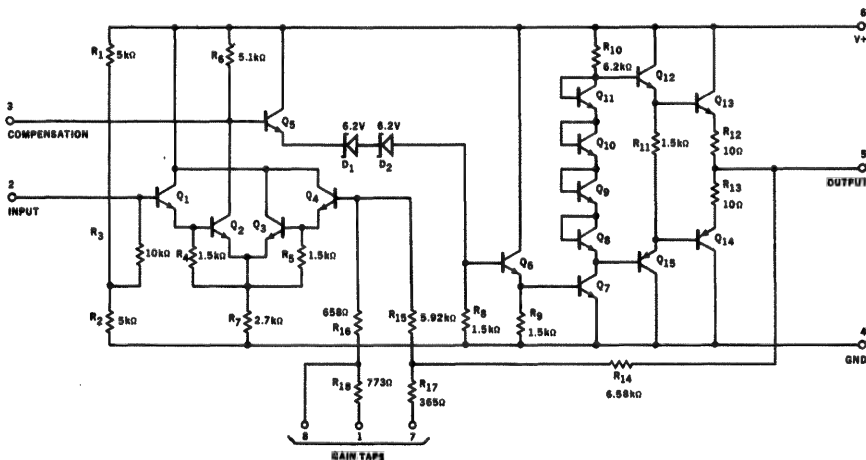
CONNECTION DIAGRAM
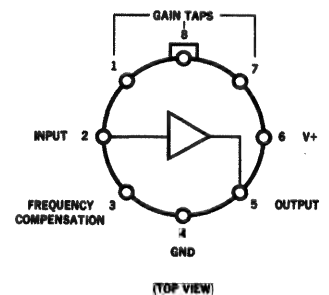
NOTE: Pin 4 internally connected to case.

NOTE 1: Rating applies for case temperatures to +125°C; derate linearly at 8.4 mW/°C for ambient temperature above +110°C.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

µA716C
FIXED-GAIN, LOW DISTORTION AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA716C is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or general purpose audio amplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100 and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	27 V
Internal Power Dissipation	600 mW
Input Voltage	±5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

in accordance with JEDEC(TO-99) outline
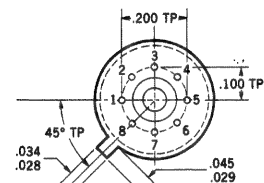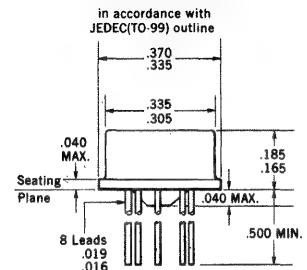
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B771639X

SCHEMATIC DIAGRAM
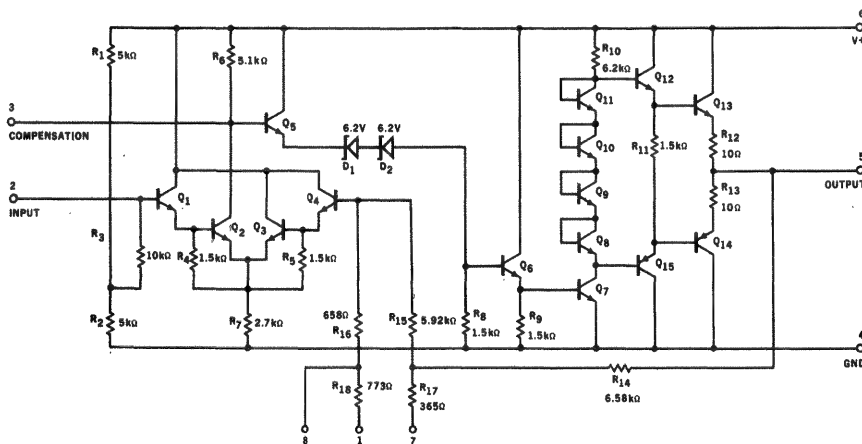
CONNECTION DIAGRAM
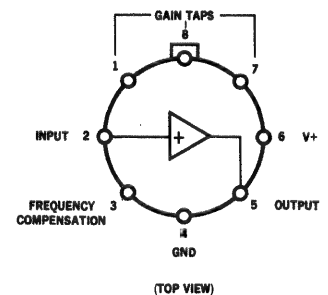
NOTE: Lead No. 4 internally connected to case

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V^+ = 21V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Quiescent Power Consumption	$T_A = 25°C$		280	350	mW
Total Harmonic Distortion	$A_V = 10$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\,\Omega$		0.01	0.05	%
	$A_V = 100$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\,\Omega$		0.10	0.50	%
Input Noise Voltage	$R_S = 600\,\Omega$, $T_A = 25°C$, $B_n = 16$ Hz to 150 kHz		8.0		μV_{rms}
Output Voltage Swing	$R_L = 150\,\Omega$	10	14		V_{p-p}
	$R_L \geq 5k\,\Omega$	15	17		V_{p-p}
Input Resistance		9.0	11		$k\Omega$
Output Resistance			1.0		Ω
Voltage Gain	See Table I				
10x		9.0	10	11	
20x		18	20	22	
100x		95	105	115	
200x		185	205	225	
Bandwidth	$T_A = 25°C$		2.0		MHz
Temperature Stability of Voltage Gain	$T_{ref} = 25°C$				
10x			±0.02	±0.25	dB
20x			±0.02	±0.25	dB
100x			±0.02	±0.25	dB
200x			±0.05	±0.50	dB

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

TRANSIENT RESPONSE
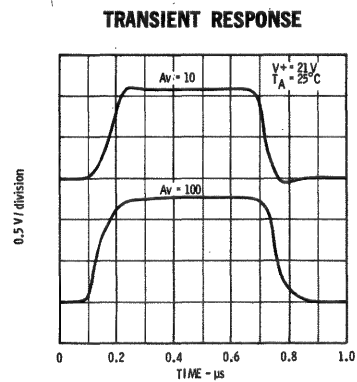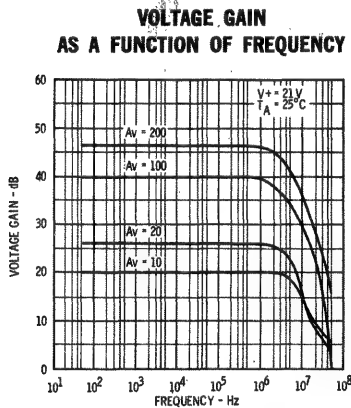
TYPICAL PERFORMANCE CURVES

TOTAL POWER CONSUMPTION AND INTERNAL DEVICE DISSIPATION AS A FUNCTION OF OUTPUT POWER

V+ = 21 V
R_L = 150 Ω
f = 1kHz
T_A = 25°C

Total power consumption

internal device dissipation

POWER - mW

OUTPUT POWER - mW

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER

V+ = 21 V
T_A = 25°C
f = 1kHz
R_L = 150 Ω

Av = 200

Av = 100

Max. THD Av = 20, 10

TOTAL HERMONIC DISTORTION - %

OUTPUT POWER - mW

POWER OUTPUT AS A FUNCTION OF FREQUENCY 5% AND 1% THD

V+ = 21 V
R_L = 150 Ω
T_A = 25°C

5% THD
1% THD

Av = 100
Av = 200
Av = 20
Av = 10
Av = 20
Av = 10
Av = 100
Av = 200

POWER OUTPUT - mW

FREQUENCY - Hz

RELATIVE VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

T_A = 25°C

Av = 10, 20
Av = 100
Av = 200

VOLTAGE GAIN CHANGE - %

SUPPLY VOLTAGE - V

VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

T_A = 25°C
f = 1kHz

$R_L \geq 5$ kΩ
R_L = 150 Ω

VOLTAGE SWING - Vpp

SUPPLY VOLTAGE - V

QUIESCENT POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

T_A = 25°C

QUIESCENT POWER CONSUMPTION- mW

SUPPLY VOLTAGE - V

RELATIVE VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

Av = 10, 20
Av = 100
Av = 200

VOLTAGE GAIN CHANGE - %

TEMPERATURE - °C

CONNECTION DIAGRAM AND COMPONENT TABLE FOR AVAILABLE GAIN OPTIONS

V+
C_1 R_1
FREQUENCY COMPENSATION
C_2
V_{IN}
μA716C
V_{OUT}
DECOUPLING CAPACITOR
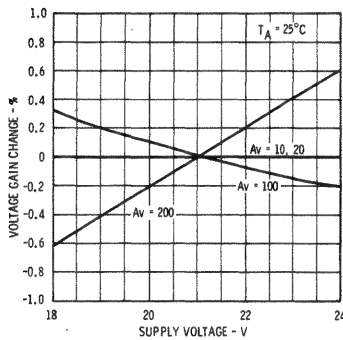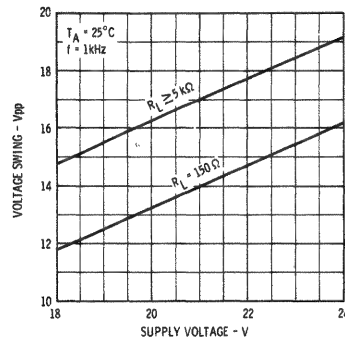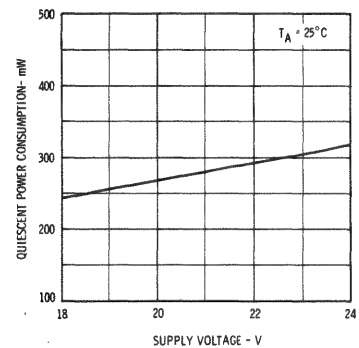
Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8

TABLE I

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

µA717E
MULTI-PURPOSE AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA717E is a multi-purpose circuit designed primarily for TV sound systems and general FM-audio applications. In TV sound systems it functions as a 4.5 MHz amplifier, limiter and FM detector (simple quadrature type), audio preamplifier and driver. Special features of the µA717E include (a) operation at supply voltages from 6 to 15 volts with simple rebiasing by the use of an external resistor, and (b) the option of using the microcircuit without the quadrature detector as a high gain amplifier from 100 kHz to 50 MHz.

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	15 V
Output Collector Voltage (RF Section)	20 V
Voltage Between "High Input" and "Low Input" Terminals	±5 V
Power Dissipation (Note 1)	350 mW
Maximum Internal Temperature (Note 2)	125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 second time limit)	260°C

PHYSICAL DIMENSIONS
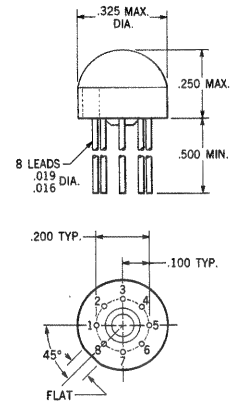
ORDER PART NO.
U8A771739X

SCHEMATIC DIAGRAM
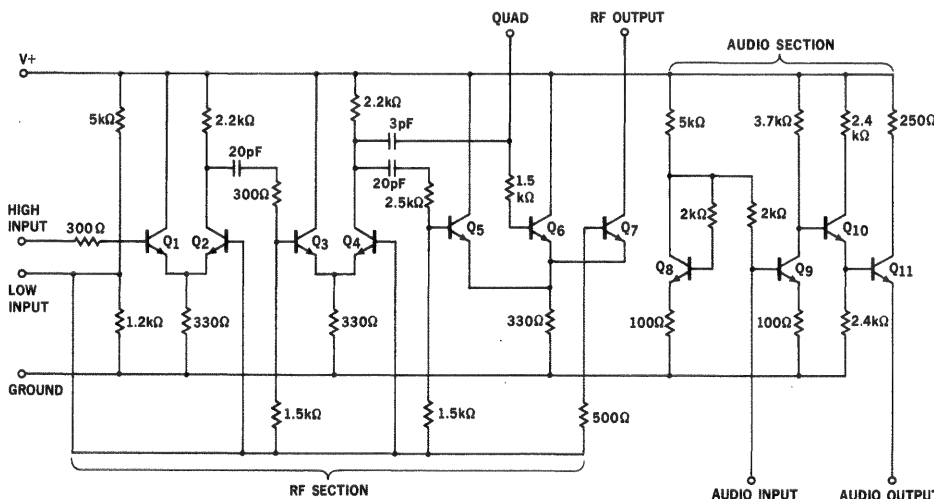
CONNECTION DIAGRAM
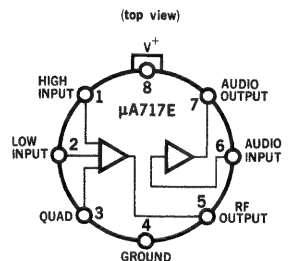
NOTES:
(1) Rating applies for ambient temperatures from 0°C to +70°C.
(2) Derate maximum dissipation by 6.4 mW/°C above 70°C.

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ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12V$, Test Circuit 4 unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total Supply Current			21		mA
Power Consumption	$e_{IN} = 0$		250	350	mW
Audio Output D-C Bias Voltage		2.0	2.6	3.2	V
Voltage Gain of Audio Section			35		
Audio Output Drive Current (clipping)	Audio output load 250Ω applied between pin 7 and ground		20		mA peak
Input Voltage for —3 dB Limiting	f = 4.5 MHz Test Circuit 9		1.5	5.0	mV rms
Noise Figure	R_S = 1kΩ, f = 4.5 MHz Test Circuit 10		7.0		dB
Noise Figure	R_S = 1kΩ, f = 10.7 MHz Test Circuit 10		7.0		dB

PARAMETER	TEST CONDITION		@ f = 4.5 MHz			@ f = 10.7 MHz			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		UNITS
Input Conductance	$e_{in} \leq$ 20 mV rms	Test Circuit 5	0.21			0.35			mmho
Input Capacitance	$e_{in} \leq$ 20 mV rms	Test Circuit 5	12			10			pF
Output Conductance		Test Circuit 6	0.05			0.1			mmho
Output Capacitance		Test Circuit 6	6.0			5.0			pF
Forward Transadmittance		Test Circuit 8	2200			1200			mmho
Gain Maximum Stable (GMS)		Test Circuit 10	80			80			dB
Gain Maximum Available (GMA)		Test Circuit 10	81			71			dB
Quadrature Conductance	$e_{in} \leq$ 20 mV rms	Test Circuit 7	0.22			0.35			mmho
Quadrature Capacitance	$e_{in} \leq$ 20 mV rms	Test Circuit 7	9.5			8.0			pF

TYPICAL PERFORMANCE CURVES

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
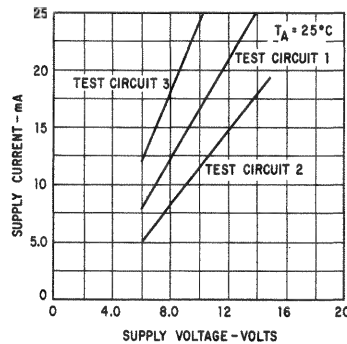
TEST CIRCUIT 1
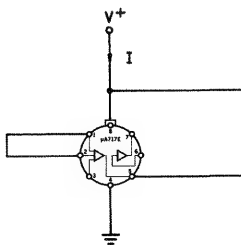
TEST CIRCUIT 2
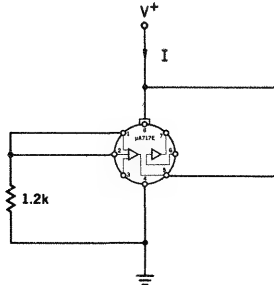
TEST CIRCUIT 3
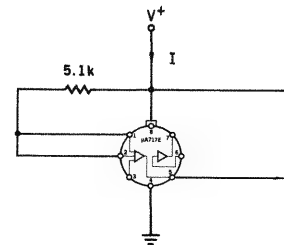
TOTAL SUPPLY CURRENT

TYPICAL PERFORMANCE CURVES

INPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF FREQUENCY
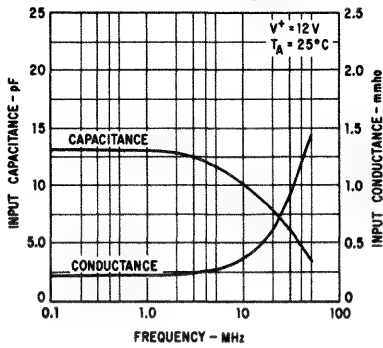
OUTPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF FREQUENCY
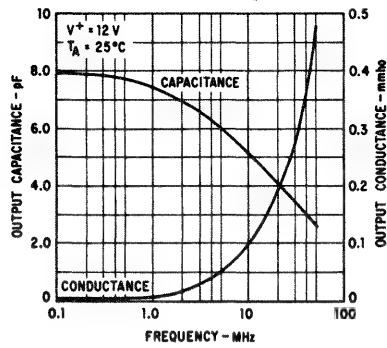
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY
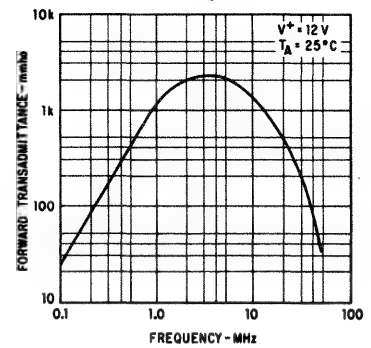
GAIN MAXIMUM AVAILABLE (GMA) AS A FUNCTION OF FREQUENCY
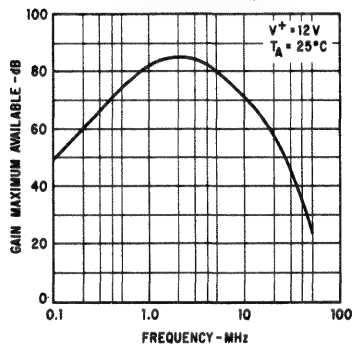
INPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE
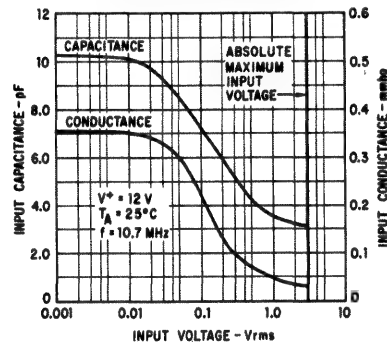
TEST CIRCUIT 4
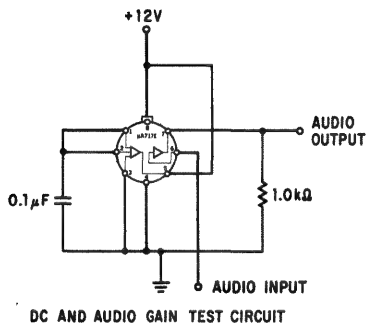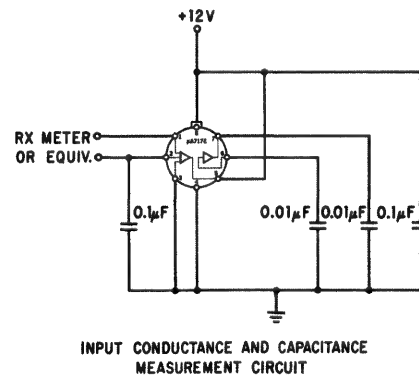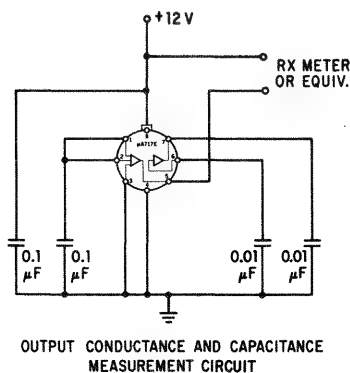
DC AND AUDIO GAIN TEST CIRCUIT

TEST CIRCUIT 5

INPUT CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 6

OUTPUT CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 7

QUADRATURE CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 8

FORWARD TRANSADMITTANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 9

TV SOUND SYSTEM

TEST CIRCUIT 10

MEASUREMENT CIRCUIT

NOISE FIGURE
GAIN MAXIMUM STABLE
GAIN MAXIMUM AVAILABLE
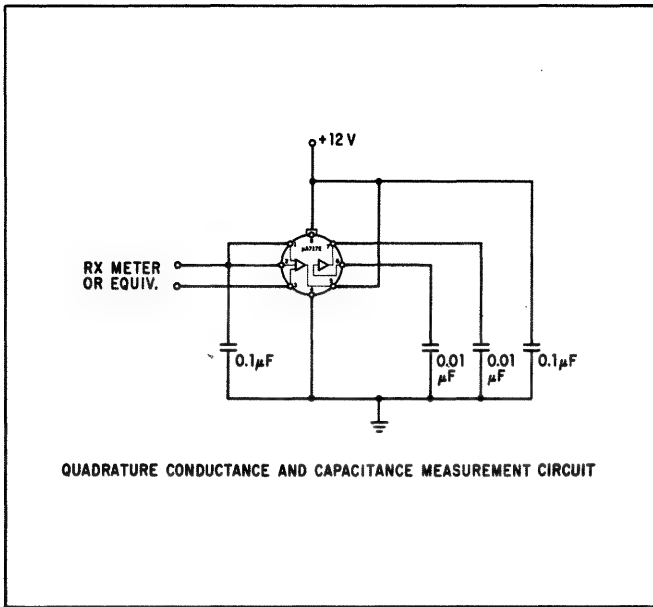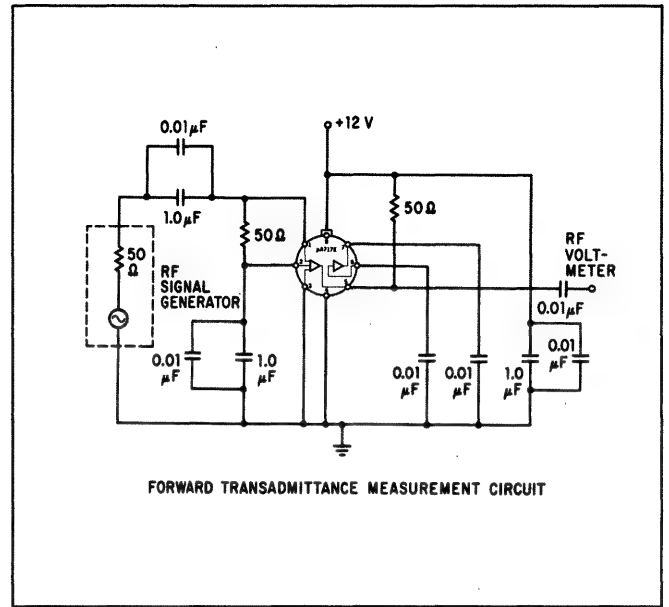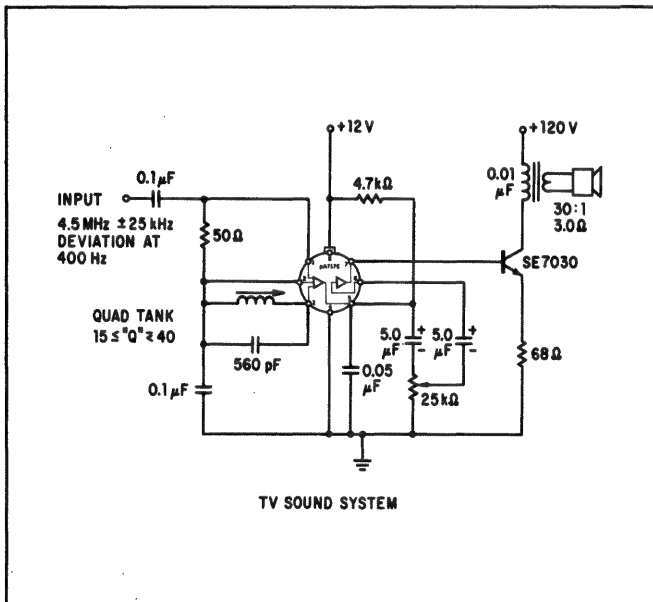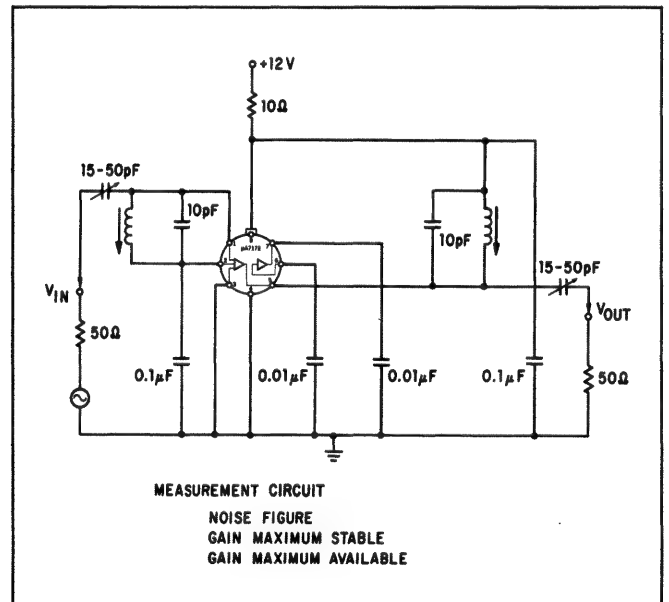
DEFINITION OF TERMS

POWER CONSUMPTION — The total power consumption of Test Circuit 1.

GAIN MAXIMUM STABLE (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum practical power gain realizable based on normal circuit tolerances is either (GMS − 6 dB) or GMA, whichever is smaller.

GAIN MAXIMUM AVAILABLE (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

INPUT LIMITING VOLTAGE — Referring to Test Circuit 9; set 25 kilohm potentiometer to give 1 watt audio output power into speaker with an input signal of 50 mV rms. The −3 dB input limiting voltage is defined as the value of the input voltage when the audio output power has fallen to 0.5 watt. For further information on the μA717E refer to Fairchild Application Bulletin No. 158, — "Two High Performance Monolithic Microcircuits For FM Sound Systems." by David Bingham.

µA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	$-55°C$ to $+125°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temperature (Soldering 60 seconds)	$300°C$
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

TOP VIEW

Note 1: Measured at 1 mA collector current.

* Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_s = \pm15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\,\mu A \leq I_C \leq 100\,\mu A$ $V_{CE} = 5$ V, $R_s \leq 50Ω$		1.0	2.5	mV
Input Offset Current	$I_C = 10\,\mu A$, $V_{CE} = 5$ V		10	50	nA
Input Offset Current	$I_C = 100\,\mu A$, $V_{CE} = 5$ V		50	200	nA
Average Input Bias Current	$I_C = 10\,\mu A$, $V_{CE} = 5$ V		50	150	nA
Average Input Bias Current	$I_C = 100\,\mu A$, $V_{CE} = 5$ V		250	500	nA
Offset Voltage Change	$I_C = 10\,\mu A$, $5\,V \leq V_{CE} \leq 25$ V, $R_s \leq 100$ kΩ		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\,\mu A$, $5\,V \leq V_{CE} \leq 25$ V, $R_s \leq 10$ kΩ		0.3	6.0	mV
Input Offset Voltage Drift	$10\,\mu A \leq I_C \leq 100\,\mu A$, $V_{CE} = 5$ V, $R_s \leq 50Ω$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	$\mu V/°C$
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\,\mu A$, $V_{CE} = 5$ V, $R_s \leq 50Ω$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	$\mu V/°C$
Input Offset Current Drift	$I_C = 10\,\mu A$, $V_{CE} = 5$ V		10		$pA/°C$
Input Offset Current Drift	$I_C = 100\,\mu A$, $V_{CE} = 5$ V		30		$pA/°C$
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\,\mu A$, $R_s \leq 50Ω$,		25		$\mu V/V$
Low-Frequency Noise	$I_C = 10\,\mu A$, $V_{CE} = 5$ V, $R_s \leq 50Ω$ BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\,\mu A$, $V_{CE} = 5$ V, $R_s \leq 50Ω$ BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	$10\,\mu A \leq I_C \leq 100\,\mu A$, $V_{CE} = 5$ V, $R_s \leq 50Ω$, $T_A = 25°C$		5.0		$\mu V/week$
High Frequency Current Gain	$f = 20$ MHz, $I_C = 100\,\mu A$, $V_{CE} = 5$ V	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5$ V		1.0		pF
Emitter Transition Capacitance	$I_E = 100\,\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\,\mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL X1000 CIRCUIT

GENERAL DESCRIPTION—The µA726C is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.   For full temperature range (−55°C to +125°C) see µA726 data sheet.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40V
BV_{CBO}	40V
LV_{CEO} (Note 1)	30V
BV_{EBO}	5V
Collector Current	5 mA

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams
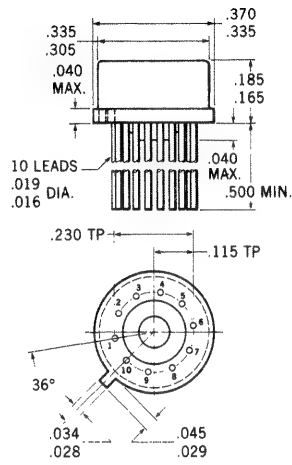
ORDER PART NO. U5J772632X

SCHEMATIC DIAGRAM
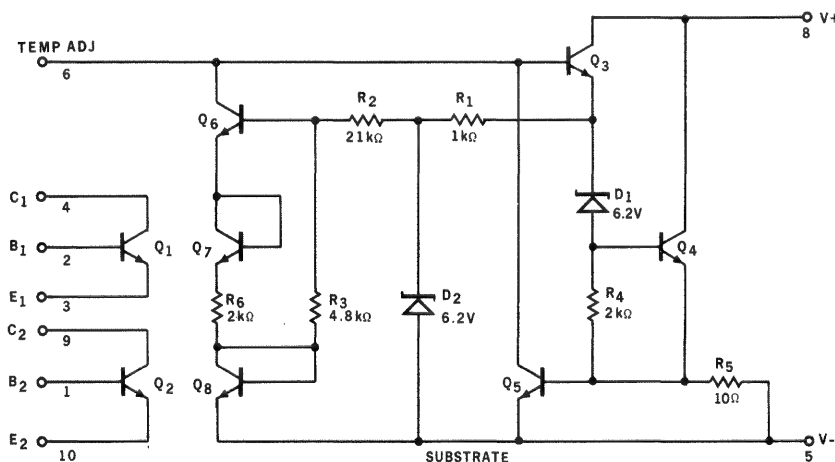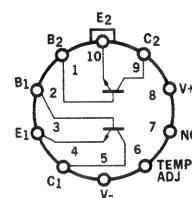
CONNECTION DIAGRAM

TOP VIEW

NOTE: (1) Measured at 1 mA collector current.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
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ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm15V$, $R_{adj} = 75\,k\Omega$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\,\mu A \leq I_C \leq 100\,\mu A$ $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\,\mu A$, $V_{CE} = 5V$		10	100	nA
Input Offset Current	$I_C = 100\,\mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\,\mu A$, $V_{CE} = 5V$		50	300	nA
Average Input Bias Current	$I_C = 100\,\mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\,\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100\,k\Omega$		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\,\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10\,k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	$\mu V/°C$
Input Offset Current Drift	$I_C = 10\,\mu A$, $V_{CE} = 5V$		10		$pA/°C$
Input Offset Current Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$		30		$pA/°C$
Supply Voltage Rejection Ratio	$I_C = 100\,\mu A$, $R_S = 50\Omega$		25		$\mu V/V$
Low-Frequency Noise	$I_C = 10\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz		10		μV pp
Long-Term Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		$\mu V/week$
High-Frequency Current Gain	$f = 20$ MHz, $I_C = 100\,\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\,\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\,\mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL X1000 CIRCUIT

µA730
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA730 is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams
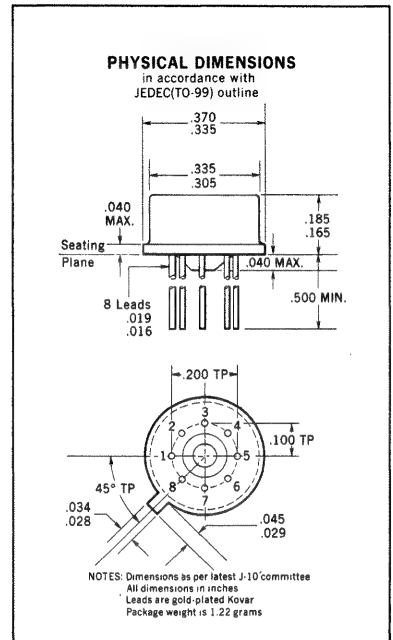
Order Part No. U5B773031X

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM
(Top View)

Note: Pin 4 connected to case

*Planar is a patented Fairchild process.

NOTES:
(1) Rating applies for case temperature to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

FAIRCHILD
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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100 \text{ k}\Omega$	100	145	160	
Differential Distortion	$R_L \geq 100 \text{ k}\Omega$		80	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100 \text{ k}\Omega$	5.0	8.0		Vpp
Supply Current	$R_L \geq 100 \text{ k}\Omega$		9.5	13	mA
Power Consumption	$R_L \geq 100 \text{ k}\Omega$		114	156	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125°C$		0.2	1.5	μA
	$T_A = -55°C$		1.0	3.0	μA
Input Bias Current	$T_A = -55°C$		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$ $f \leq 1.0$ kHz, $+3.5 \text{ V} \leq V_{CM} \leq +5.2 \text{ V}$	70	85		dB
Differential Voltage Gain	$R_L \geq 100 \text{ k}\Omega$	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		Vpp
Supply Current	$T_A = -55°C$		10	15	mA
	$T_A = 125°C$		8.0	11	mA
Power Consumption	$T_A = -55°C$		120	180	mW
	$T_A = 125°C$		96	121	mW

TYPICAL PERFORMANCE CURVES

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL PERFORMANCE CURVES

INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE TRANSFER CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.

BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.

OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.

COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.

OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.

SUPPLY CURRENT—The current required from the power supply to operate the device with no load.

POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

µA730C
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA730C is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

For full temperature range operation (−55°C to +125°C), see µA730 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B773039X

SCHEMATIC DIAGRAM
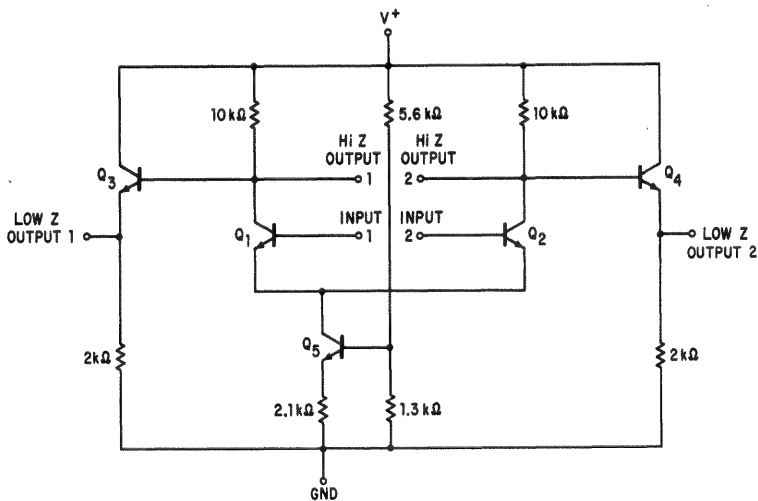
CONNECTION DIAGRAM
(Top View)
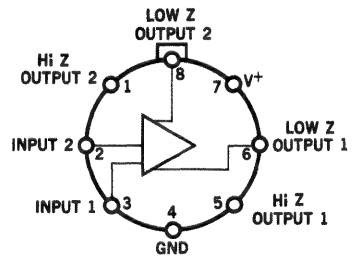
Note: Pin 4 connected to case

NOTES:
(1) Rating applies for ambient temperatures to + 70°C.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V+ = 12.0 V, and $V_{CM} = 3.5$ V unless otherwise specified)

PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$		0.5	3.0	μA
	$T_A = 0°C$		0.8	5.0	μA
Input Bias Current	$T_A = 0°C$		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$	60	80		dB
	$f \leq 1.0$ kHz,				
	$+3.5$ V $\leq V_{CM} \leq +5.2$ V				
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		Vpp
Supply Current	$T_A = 0°C$		10	15	mA
	$T_A = +70°C$		8.8	13	mA
Power Consumption	$T_A = 0°C$		120	180	mW
	$T_A = +70°C$		106	156	mW

TYPICAL PERFORMANCE CURVES

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL PERFORMANCE CURVES

INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

VOLTAGE TRANSFER CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.

BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.

OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.

COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.

OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.

SUPPLY CURRENT—The current required from the power supply to operate the device with no load.

POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

FAIRCHILD
LINEAR
INTEGRATED
CIRCUITS

1970

µA719
HIGH GAIN RF AMPLIFIER/FM DETECTOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The µA719 is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation (Note 1)	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)

NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719312

SCHEMATIC DIAGRAM
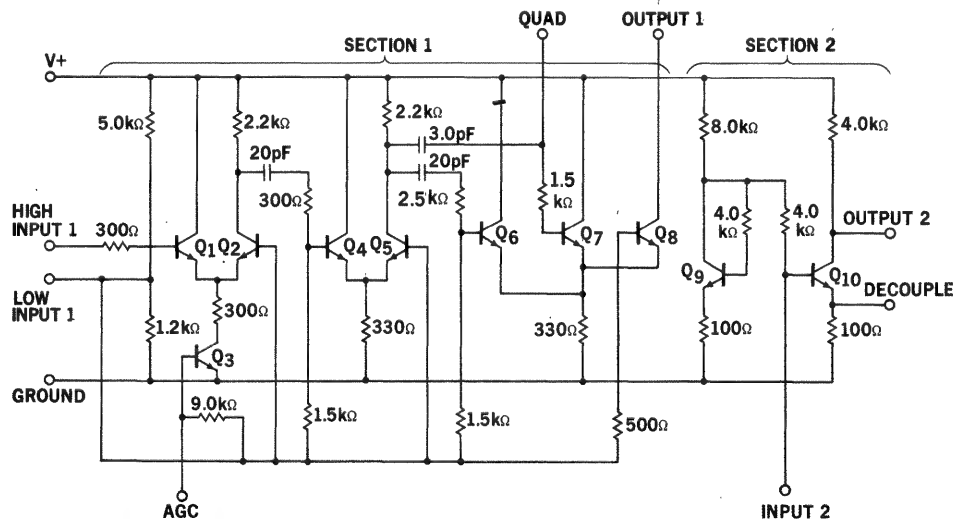
CONNECTION DIAGRAM
(TOP VIEW)
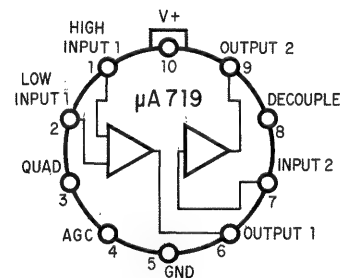
NOTE:
(1) Rating applies for ambient temperatures to +125°C if the package case to ambient thermal resistance is lowered to 40°C/Watt by the addition of a heat dissipator. Derate linearly 5.6 mW/°C for ambient temperatures above 87°C.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)		TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current		$T_A = +25°C$	12	18	25	mA
		$T_C = -55°C$		17.5		mA
		$T_C = +125°C$		17		mA
Supply Current		$V^+ = 9.0$ V,	6.0	12.5	18.5	mA
Power Dissipation		$T_A = +25°C$	144	216	300	mW
		$T_C = -55°C$		210		mW
		$T_C = +125°C$		204		mW
Power Dissipation		$V^+ = 9.0$ V,	54	113	167	mW
Section 1	Quiescent Output Current		1.0	2.5	4.0	mA
Section 1	DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1	AGC Current For 30 dB AGC	$f = 10.7$ MHz, Test Circuit 3		170	250	μA
Section 1	Output Current	$f = 1.0$ MHz, Test Circuit 8		4.4		mA$_{p-p}$
Section 1	Voltage Gain	$f = 10.7$ MHz, Test Circuit 3				
		$T_A = +25°C$	53	60		dB
		$T_C = -55°C$		63		dB
		$T_C = +125°C$		58		dB
Section 1	Voltage Gain	$f = 10.7$ MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1	Input Voltage For -3.0 dB Limiting	$f = 4.5$ MHz, Test Circuit 4		1.5	4.0	mV
Section 1	Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
		$f = 4.5$ MHz		7.0		dB
		$f = 10.7$ MHz		7.0		dB
Section 2	DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2	Voltage Gain	$f = 1.0$ kHz, Test Circuit 2	22	31		dB
Section 2	Voltage at Output 2 Without Clipping	$f = 1.0$ kHz, Test Circuit 2		10		V$_{p-p}$

PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	$e_{IN} \leq 20$ mV Test Circuit 6	170	300	μmho
Input Capacitance	$e_{IN} \leq 20$ mV Test Circuit 6	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8 $V^+ = 9.0$ V	1000	600	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2	Test Circuit 10			
Input Conductance	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

SECTION 1
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE

$V^+ = 12V$
$f = 10.7$ MHz
TEST CIRCUIT

VOLTAGE GAIN – dB

TEMPERATURE – °C

SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

$T_A = 25°C$

$V^+ = 12V$

$V^+ = 9.0V$

FORWARD TRANSADMITTANCE – mmho

FREQUENCY – MHz

SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE

$T_A = 25°C$
$f = 10.7$ MHz

FORWARD TRANSADMITTANCE – mmho

SUPPLY VOLTAGE – V

SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE

CAPACITANCE

$V^+ = 12V$
$T_A = 25°C$
$f = 10.7$ MHz

CONDUCTANCE

INPUT CAPACITANCE – pF

INPUT CONDUCTANCE – μmho

INPUT VOLTAGE – mV (rms)

SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY

$V^+ = 12V$
$T_A = 25°C$

CAPACITANCE

CONDUCTANCE

INPUT CAPACITANCE – pF

INPUT CONDUCTANCE – μmho

FREQUENCY – MHz

SECTION 1
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY

$V^+ = 12V$
$T_A = 25°C$

CAPACITANCE

CONDUCTANCE

OUTPUT CAPACITANCE – pF

OUTPUT CONDUCTANCE – μmho

FREQUENCY – MHz

SECTION 1
AGC AS A FUNCTION OF AGC CURRENT

$V^+ = 12V$
$f = 10.7$ MHz

+25°C
+125°C
-55°C

AGC – GAIN REDUCTION – dB
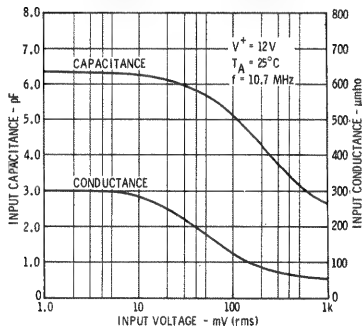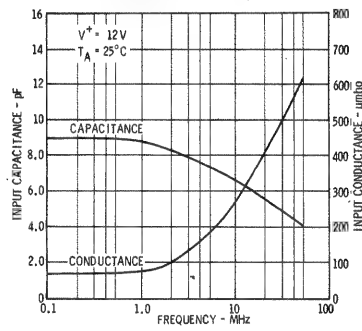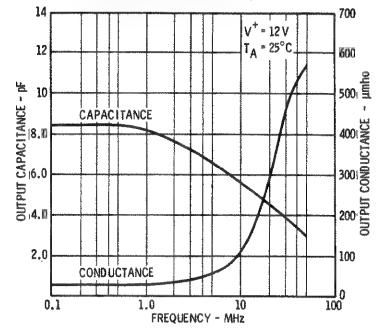
AGC CURRENT – μA
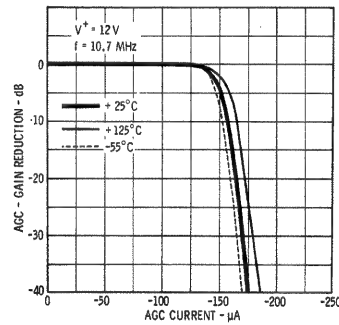
TYPICAL PERFORMANCE CURVES

SECTION 2
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY
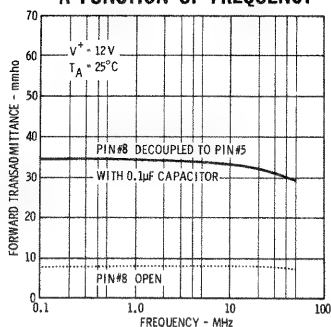
$V^+ = 12 V$
$T_A = 25°C$

PIN#8 DECOUPLED TO PIN#5
WITH 0.1μF CAPACITOR

PIN#8 OPEN

FORWARD TRANSADMITTANCE - mmho
FREQUENCY - MHz

SECTION 2
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY

CAPACITANCE   CONDUCTANCE
$V^+ = 12 V$
$T_A = 25°C$

PIN#8 OPEN
PIN#8 DECOUPLED TO
PIN#5 WITH 0.1μF CAPACITOR.

CAPACITANCE

CONDUCTANCE

INPUT CAPACITANCE - pF
INPUT CONDUCTANCE - μmho
FREQUENCY - MHz

SECTION 2
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY

$V^+ = 12 V$
$T_A = 25°C$

CAPACITANCE
CONDUCTANCE

CAPACITANCE

PIN #8 DECOUPLED TO
PIN #5 WITH 0.1 μF CAPACITOR
PIN #8 OPEN
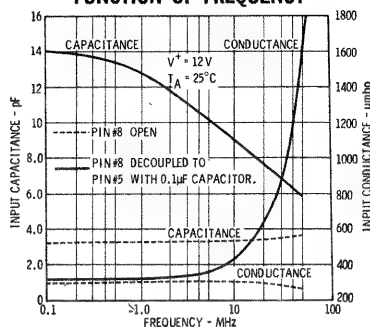
CONDUCTANCE

OUTPUT CAPACITANCE - pF
OUTPUT CONDUCTANCE - μmho
FREQUENCY - MHz

MAXIMUM INTERNAL DISSIPATION AS A FUNCTION OF EITHER AMBIENT OR CASE TEMPERATURE

$V^+ = 12 V$

AMBIENT

MAXIMUM DISSIPATION
(OBTAINED WITH HEAT SINK RATED CASE TO AMBIENT AT 40°C/WATT)

-55   +87

INTERNAL POWER DISSIPATION - mW
TEMPERATURE °C

SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE

$V^+ = 12 V$
$f = 10.7 MHz$

$T_A = +25°C$
$T_A = -55°C$
$T_A = +125°C$

SUPPLY CURRENT - mA
INPUT VOLTAGE - mVrms

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

$V^+ = 12 V$
$T_A = 25°C$
TEST CIRCUIT 1.

SUPPLY CURRENT - mA
SUPPLY VOLTAGE - V

TEST CIRCUITS

TEST CIRCUIT 1

DC MEASUREMENTS

$V+$
I SUPPLY CURRENT
I QUIESCENT (OUTPUT 1)

V OUTPUT 2

μA719

0.1 μF

V_{AGC}

TEST CIRCUIT 2

SECTION 2 GAIN AND OUTPUT VOLTAGE SWING

$+12 V$

VTUM

μA719

0.1μF

10μF
6.0V

$R_S \leq 600 Ω$
$R_L \geq 100 kΩ$

e_{in}

TEST CIRCUITS

TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC

TEST CIRCUIT 4

-3.0 dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*

INPUT SIGNAL 4.5 MHz 25 kHz DEVIATION AT 400 Hz. UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 65.
* SEE DEFINITIONS

TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.

TEST CIRCUIT 6

SECTION 1 INPUT PARAMETERS

TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS

TEST CIRCUIT 8

SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT

$$\text{FORWARD TRANSADMITTANCE} = \frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3 \text{ mmho}$$

TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS

TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS

TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS

TEST CIRCUIT 12

SECTION 2 FORWARD TRANSADMITTANCE

$$\text{FORWARD TRANSADMITTANCE} = \frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3 \, \text{mmho}$$

DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$\text{GMA} = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$\text{GMS} = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719 being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719 and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

µA719C
HIGH GAIN RF AMPLIFIER/FM DETECTOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The µA719C is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO—100)
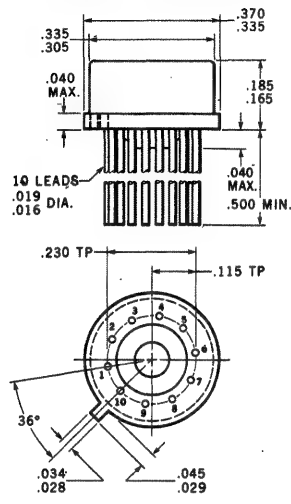
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719393

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM
(TOP VIEW)

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12\,V$, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_A = 0°C$	10	17.5	27	mA
	$T_A = +70°C$	10	17	25	mA
Supply Current	$V^+ = 9.0\,V$	6.0	12.5	18.5	mA
Supply Current	$V^+ = 6.0\,V$, $70°C \leq T_A \leq 0°C$	3.0	6.0	10	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_A = 0°C$	120	210	324	mW
	$T_A = +70°C$	120	204	300	mW
Power Dissipation	$V^+ = 9.0\,V$	54	113	167	mW
Power Dissipation	$V^+ = 6.0\,V$, $70°C \leq T_A \leq 0°C$	18	36	60	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	$f = 10.7\,MHz$, Test Circuit 3		170	250	μA
Section 1 Output Current	$f = 1.0\,MHz$, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	$f = 10.7\,MHz$, Test Circuit 3				
	$T_A = +25°C$	50	60	70	dB
	$T_A = 0°C$	50	61	70	dB
	$T_A = +70°C$	48	59	70	dB
Section 1 Voltage Gain	$f = 10.7\,MHz$, Test Circuit 3, $V^+ = 9.0\,V$		53		dB
Section 1 Voltage Gain	$f = 10.7\,MHz$, Test Circuit 3, $V^+ = 6.0\,V$		38		dB
Section 1 Input Voltage For −3.0 dB Limiting	$f = 4.5\,MHz$, Test Circuit 4		1.5	6.5	mV
Section 1 Noise Figure	$R_S = 1.0\,k\Omega$, Test Circuit 5				
	$f = 4.5\,MHz$		7.0		dB
	$f = 10.7\,MHz$		7.0		dB
Sections 1 and 2 Cascaded Voltage Gain	$f = 10.7\,MHz$, Test Circuit 13 $V^+ = 6.0\,V$, $R = 3.0\,k\Omega$				
	Pin #8 Unbypassed		51		dB
	Pin #8 Bypassed		56		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	$f = 1.0\,kHz$, Test Circuit 2	22	31	40	dB
Section 2 Voltage at Output 2 Without Clipping	$f = 1.0\,kHz$, Test Circuit 2	7.0	10	11.5	V_{p-p}

PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	Test Circuit 6, $e_{IN} \leq 20\,mV$	170	300	μmho
Input Capacitance	Test Circuit 6, $e_{IN} \leq 20\,mV$	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 9.0\,V$	1000	600	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 6.0\,V$	180	100	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2	Test Circuit 10			
Input Conductance	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE
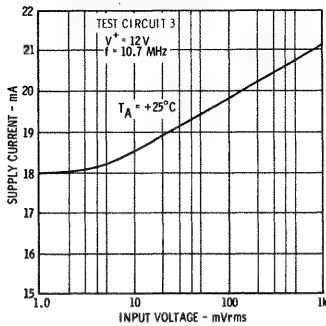
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
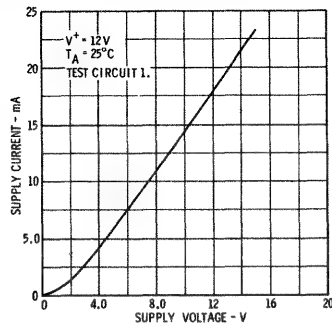
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY
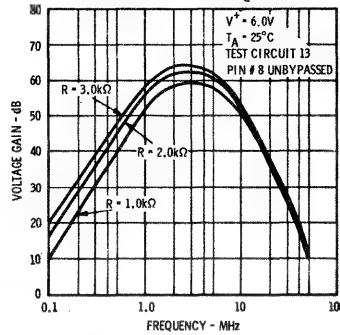
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY
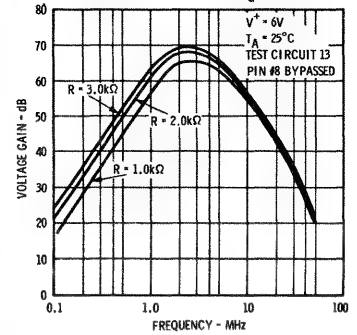
SECTION 1 AGC AS A FUNCTION OF AGC CURRENT
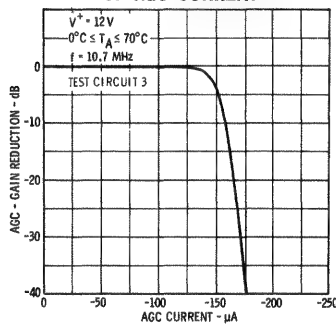
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY
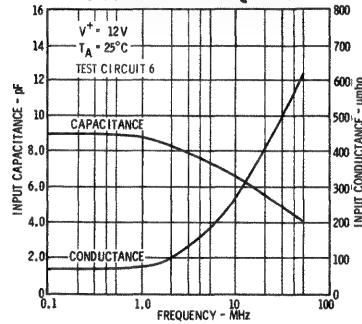
SECTION 1 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY
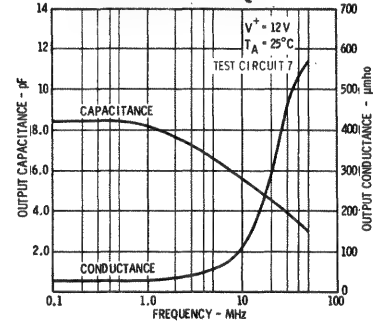
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY
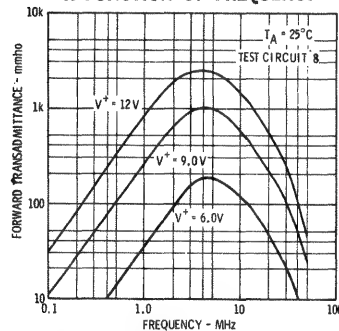
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE
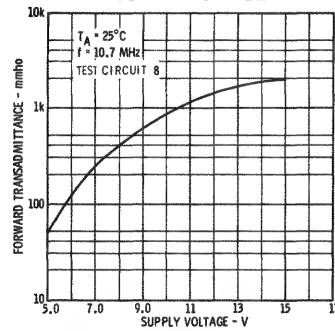
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE
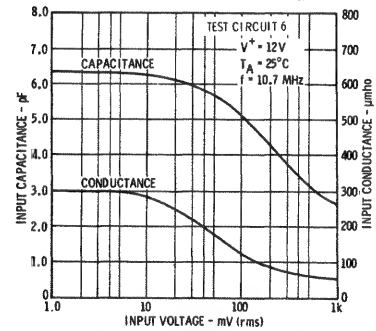
SECTION 2 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY
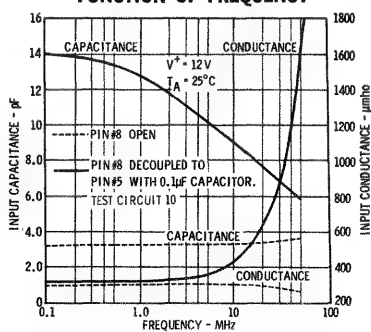
SECTION 2 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY
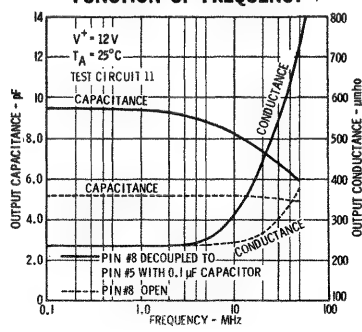
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

TEST CIRCUITS

TEST CIRCUIT 1

DC MEASUREMENTS
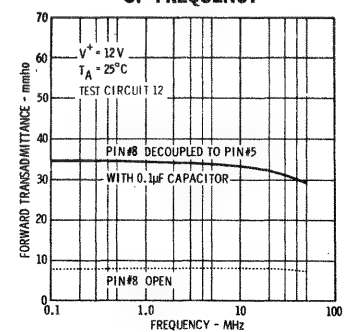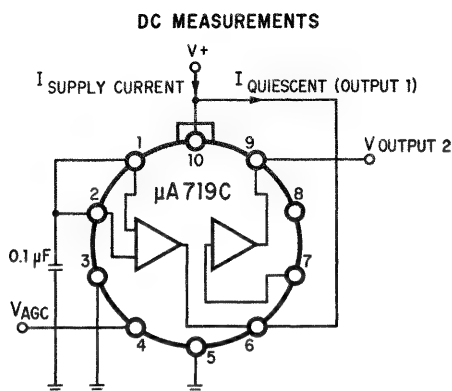
TEST CIRCUIT 2

SECTION 2 GAIN AND OUTPUT VOLTAGE SWING

TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC
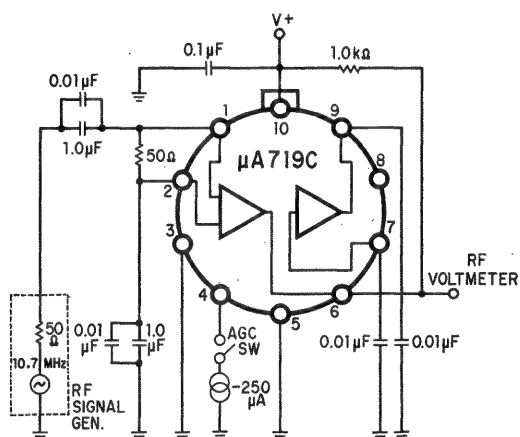
TEST CIRCUIT 4

−3.0 dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR *

INPUT SIGNAL 4.5 MHz 25 kHz DEVIATION AT 400 Hz. UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 22.
* SEE DEFINITIONS
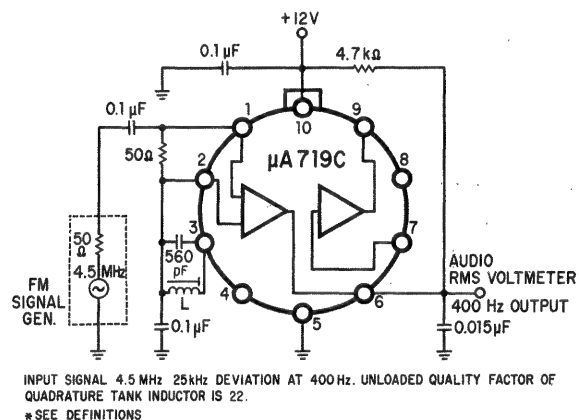
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.
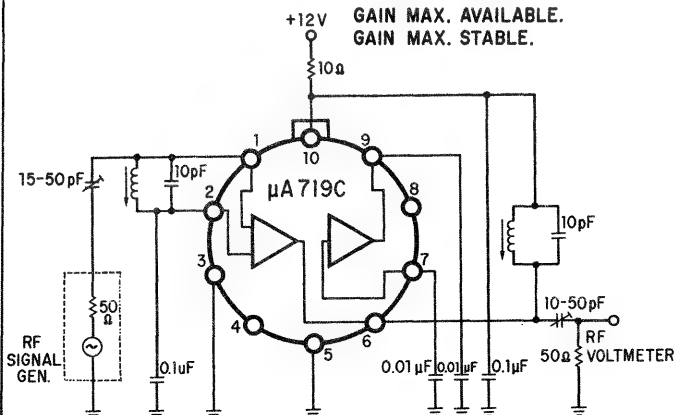
TEST CIRCUIT 6

SECTION 1 INPUT PARAMETERS

TEST CIRCUITS

TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS
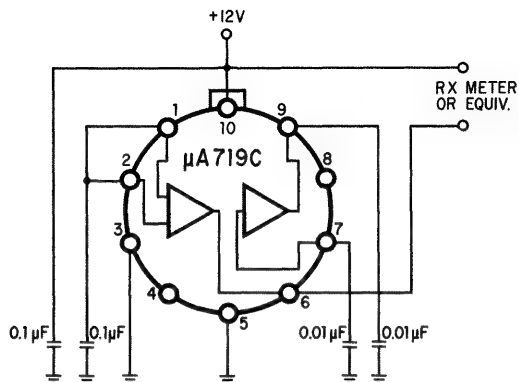
TEST CIRCUIT 8

SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT

$$\text{FORWARD TRANSADMITTANCE} = \frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3 \text{ mmho}$$

TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS

TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS

TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS

TEST CIRCUIT 12

SECTION 2 FORWARD TRANSADMITTANCE

$$\text{FORWARD TRANSADMITTANCE} = \frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3 \text{ mmho}$$
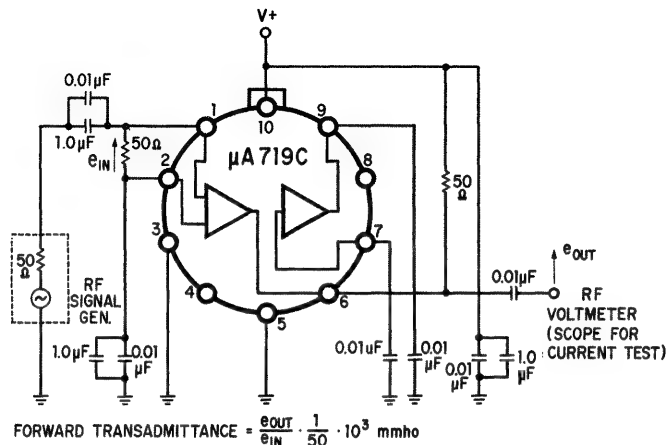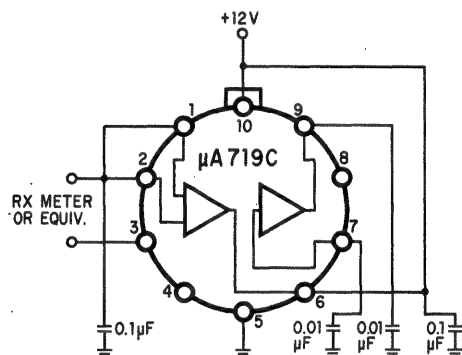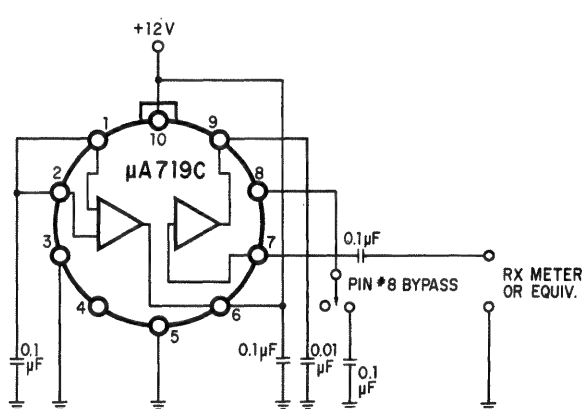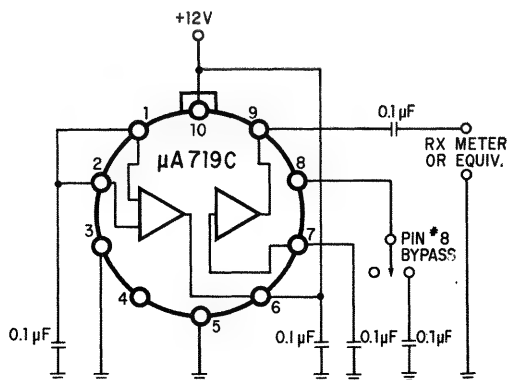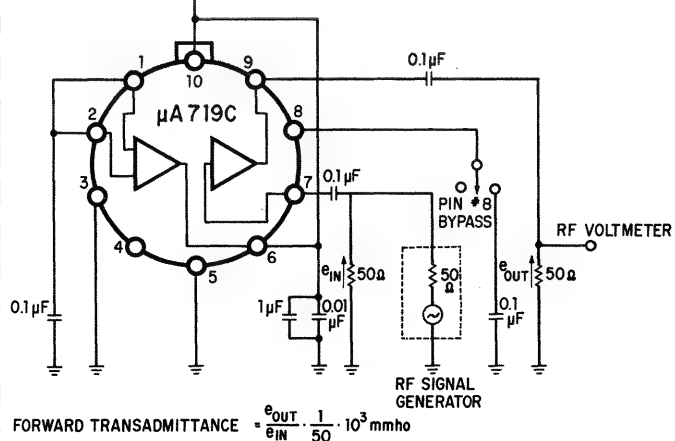
TEST CIRCUIT 13

SECTION 1 AND 2 CASCADED VOLTAGE GAIN

V⁺ = 6.0V

0.1µF
50Ω
RF
SIGNAL
GEN.
50Ω
0.1µF

μA719C

RF VOLTMETER

1000pF
R

PIN 8 BYPASS

0.1µF   0.1µF

DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{ forward transadmittance }|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$GMS = \frac{|\text{ forward transadmittance }|}{|\text{ reverse transadmittance }|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719C being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719C and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

µA723
PRECISION VOLTAGE REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

* POSITIVE OR NEGATIVE SUPPLY OPERATION
* SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
* .01% LINE AND LOAD REGULATION
* OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
* OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR

GENERAL DESCRIPTION — The µA723 is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The µA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.
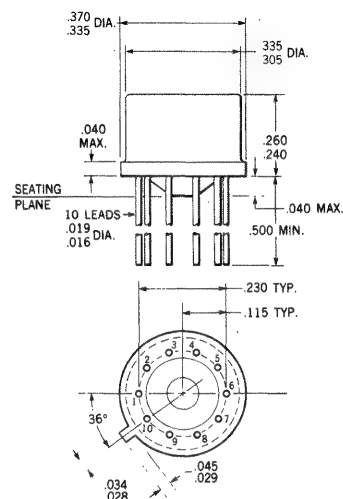
ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V$^+$ to V$^-$ (50 msec)	50 V
Continuous Voltage from V$^+$ to V$^-$	40 V
Input-Output Voltage Differential	40 V
Current from V$_Z$	25 mA
Current from V$_{REF}$	15 mA
Internal Power Dissipation Metal Can (Note 1)	800 mW
DIP (Note 1)	900 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5R7723312

EQUIVALENT CIRCUIT

CONNECTION DIAGRAMS
TOP VIEWS

Note: On metal can, pin 5 is connected to case

TYPICAL DUAL IN-LINE PACKAGE

NOTES: All dimensions in inches
Leads are intended for insertion
in hole rows, .300 centers

ORDER PART NO. U6A7723393

Notes on Page 2.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (Note 2)

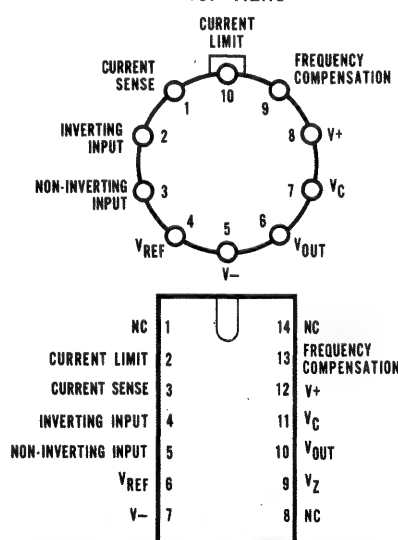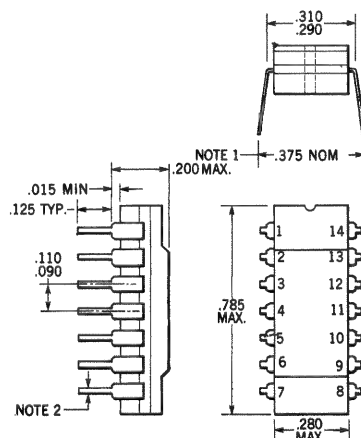| PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12\,V$ to $V_{IN} = 15\,V$		.01	0.1	% V_{OUT}
	$V_{IN} = 12\,V$ to $V_{IN} = 40\,V$		.02	0.2	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $V_{IN} = 12\,V$ to $V_{IN} = 15\,V$			0.3	% V_{OUT}
Load Regulation	$I_L = 1\,mA$ to $I_L = 50\,mA$		.03	0.15	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $I_L = 1\,mA$ to $I_L = 50\,mA$			0.6	% V_{OUT}
Ripple Rejection	$f = 50\,Hz$ to $10\,kHz$, $C_{REF} = 0$		74		dB
	$f = 50\,Hz$ to $10\,kHz$, $C_{REF} = 5\,\mu F$		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		.002	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\,\Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	$BW = 100\,Hz$ to $10\,kHz$, $C_{REF} = 0$		20		μV_{rms}
	$BW = 100\,Hz$ to $10\,kHz$, $C_{REF} = 5\,\mu F$		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30\,V$		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION — The percentage change in output voltage for a specified change in load current.

RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.

SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.

REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.

OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.

STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.

INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.

OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.

TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

NOTES:
(1) Derate metal can package at 6.8 mW/°C and dual-in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12\,V$, $V^- = 0$, $V_{out} = 5\,V$, $I_L = 1\,mA$, $R_{SC} = 0$, $C_I = 100\,pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10\,K\Omega$ connected as shown in Fig. 1.
(3) L_I is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
(4) Figures in parentheses may be used if R_I/R_2 divider is placed on opposite of error amp.
(5) Replace R_I/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a $+3\,V$ or greater supply.

TYPICAL PERFORMANCE CURVES

MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL
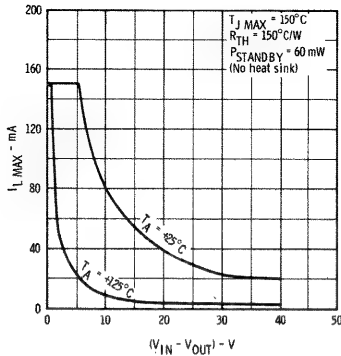
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING
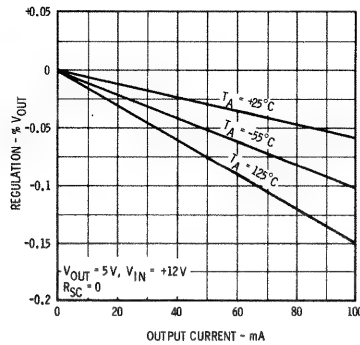
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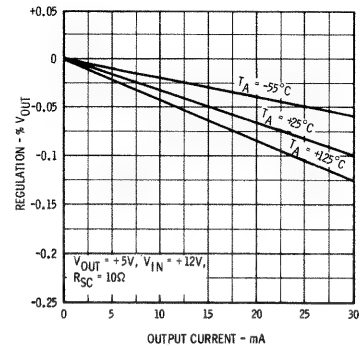
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING
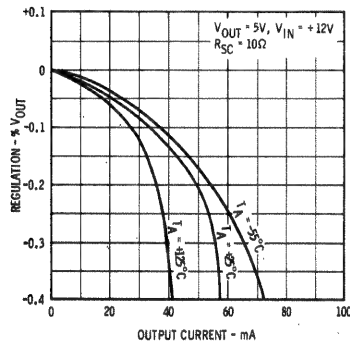
CURRENT LIMITING CHARACTERISTICS
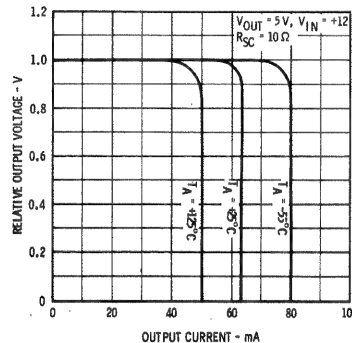
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE
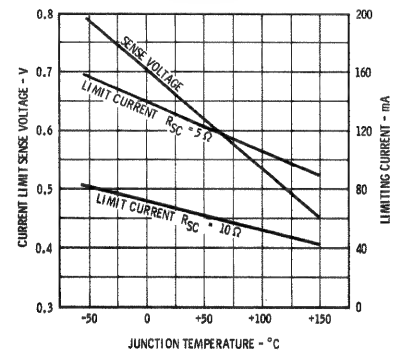
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL
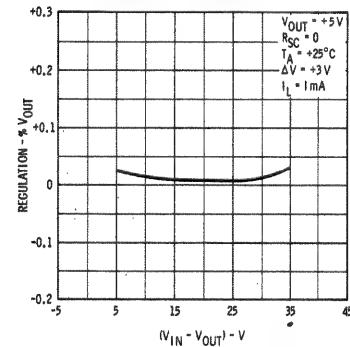
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

LINE TRANSIENT RESPONSE

LOAD TRANSIENT RESPONSE

OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

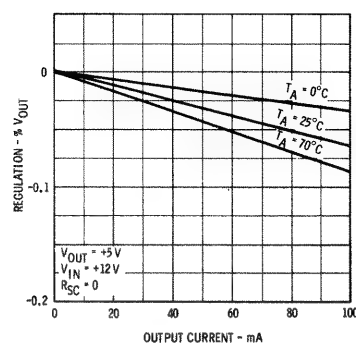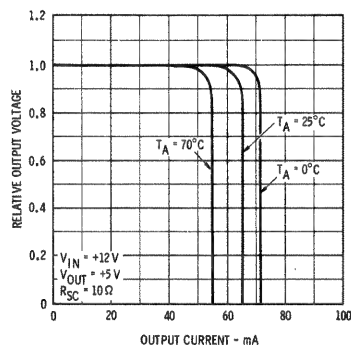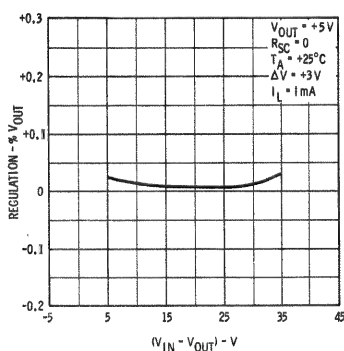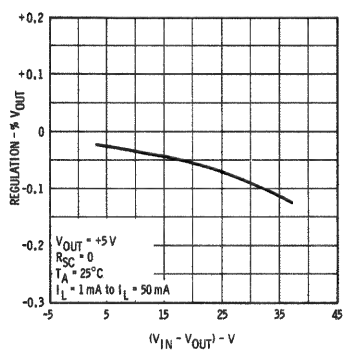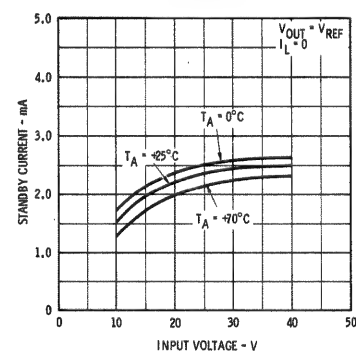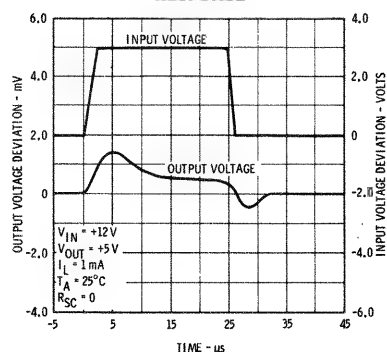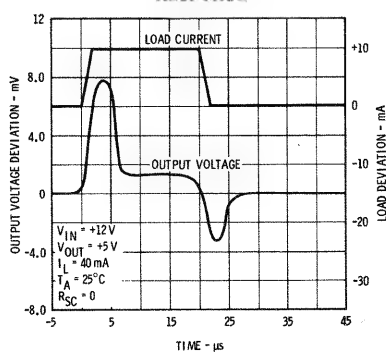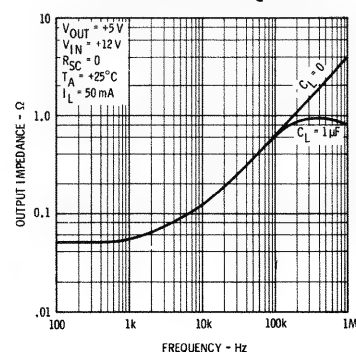| POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES (Note 4)	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)]	Outputs from +4 to +250 volts [Figure 7]	Current Limiting
$V_{OUT} = [V_{REF} \times \dfrac{R_2}{R_1 + R_2}]$	$V_{OUT} = [\dfrac{V_{REF}}{2} \times \dfrac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	$I_{LIMIT} = \dfrac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)]	Outputs from −6 to −250 volts [Figures 3, 8, 10]	Foldback Current Limiting
$V_{OUT} = [V_{REF} \times \dfrac{R_1 + R_2}{R_2}]$	$V_{OUT} = [\dfrac{V_{REF}}{2} \times \dfrac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	$I_{KNEE} = [\dfrac{V_{OUT} R_3}{R_{sc} R_4} + \dfrac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\dfrac{V_{SENSE}}{R_{sc}} \times \dfrac{R_3 + R_4}{R_4}]$

Figure 1
BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

TYPICAL PERFORMANCE
Regulated Output Voltage — 5 V
Line Regulation (ΔV_{IN} = 3 V) 0.5 mV
Load Regulation (ΔI_L = 50 mA) 1.5 mV

Note: $R_3 = \dfrac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2
BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)

TYPICAL PERFORMANCE
Regulated Output Voltage — 15 V
Line Regulation (ΔV_{IN} = 3 V) 1.5 mV
Load Regulation (ΔI_L = 50 mA) 4.5 mV

Note: $R_3 = \dfrac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3
NEGATIVE VOLTAGE REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 3 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Figure 4
POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

Figure 5
POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

Figure 6
FOLDBACK CURRENT LIMITING

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Current Limit Knee	20 mA

Figure 7
POSITIVE FLOATING REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

Figure 8
NEGATIVE FLOATING REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔV_{IN} = 20 V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

Figure 9

POSITIVE SWITCHING REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30 V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

Note 3

Figure 10

NEGATIVE SWITCHING REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

Note: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Figure 12

SHUNT REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L=100 mA)	1.5 mV

Figure 13

OUTPUT VOLTAGE ADJUST

SCHEMATIC DIAGRAM

µA723C
PRECISION VOLTAGE REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- .01% LINE AND LOAD REGULATION
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
- OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR

GENERAL DESCRIPTION — The µA723C is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The µA723C is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits. For full temperature range operation (−55°C to +125°C), see µA723 data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage from V⁺ to V⁻	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation—Metal Can (Note 1)	800 mW
Internal Power Dissipation—DIP (Note 1)	900 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS

NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5R7723393

EQUIVALENT CIRCUIT

CONNECTION DIAGRAMS
TOP VIEWS

Note: On metal can, pin 5 is connected to case

TYPICAL DUAL IN-LINE PACKAGE

NOTES: All dimensions in inches
Leads are intended for insertion
in hole rows, .300 centers

ORDER PART NO. U6A7723393

Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		.01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		0.1	0.5	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.2	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		.003	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10$ Ω, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

NOTES:
(1) Derate metal can package at 6.8 mW/°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12$ V, $V^- = 0$, $V_{out} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, $C_I = 100$ pF, $C_{REF} = 0$, divider impedance as seen by error amplifier ≤ 10 kΩ, and connected as shown in Figure 1.
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{out}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.
(7) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

TYPICAL PERFORMANCE CURVES

MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

$T_{J\,MAX} = 150°C$
$R_{TH} = 150°C/W$
$P_{STANDBY} = 60\,mW$
METAL CAN PACKAGE
(NO HEAT SINK)

$T_A = 25°C$
$T_A = 70°C$

$I_L\,MAX - mA$ vs $(V_{IN} - V_{OUT}) - V$

MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

$T_{J\,MAX} = 125°C$
$R_{TH} = 111°C/W$
$P_{STANDBY} = 60\,mW$
DIP PACKAGE
(NO HEAT SINK)

$T_A = 25°C$
$T_A = 70°C$

$I_L\,MAX - mA$ vs $(V_{IN} - V_{OUT}) - V$

LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

$T_A = 0°C$
$T_A = 25°C$
$T_A = 70°C$

$V_{OUT} = +5\,V$
$V_{IN} = +12\,V$
$R_{SC} = 0$

REGULATION - % V_{OUT} vs OUTPUT CURRENT - mA

LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

$V_{OUT} = +5\,V$
$V_{IN} = +12\,V$
$R_{SC} = 10\,\Omega$

$T_A = 25°C$
$T_A = 0°C$
$T_A = 70°C$

REGULATION - % V_{OUT} vs OUTPUT CURRENT - mA

CURRENT LIMITING CHARACTERISTICS

$T_A = 70°C$
$T_A = 25°C$
$T_A = 0°C$

$V_{IN} = +12\,V$
$V_{OUT} = +5\,V$
$R_{SC} = 10\,\Omega$

RELATIVE OUTPUT VOLTAGE vs OUTPUT CURRENT - mA

CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE

SENSE VOLTAGE
LIMIT CURRENT $R_{SC} = 5\,\Omega$
LIMIT CURRENT $R_{SC} = 10\,\Omega$

CURRENT LIMIT SENSE VOLTAGE - V / LIMITING CURRENT - mA vs JUNCTION TEMPERATURE - °C

LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

$V_{OUT} = +5\,V$
$R_{SC} = 0$
$T_A = +25°C$
$\Delta V = +3\,V$
$I_L = 1\,mA$

REGULATION - % V_{OUT} vs $(V_{IN} - V_{OUT}) - V$

LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

$V_{OUT} = +5\,V$
$R_{SC} = 0$
$T_A = 25°C$
$I_L = 1\,mA$ to $I_L = 50\,mA$

REGULATION - % V_{OUT} vs $(V_{IN} - V_{OUT}) - V$

STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

$V_{OUT} = V_{REF}$
$I_L = 0$

$T_A = 0°C$
$T_A = +25°C$
$T_A = +70°C$

STANDBY CURRENT - mA vs INPUT VOLTAGE - V

LINE TRANSIENT RESPONSE

INPUT VOLTAGE
OUTPUT VOLTAGE

$V_{IN} = +12\,V$
$V_{OUT} = +5\,V$
$I_L = 1\,mA$
$T_A = 25°C$
$R_{SC} = 0$

OUTPUT VOLTAGE DEVIATION - mV / INPUT VOLTAGE DEVIATION - VOLTS vs TIME - μs

LOAD TRANSIENT RESPONSE

LOAD CURRENT
OUTPUT VOLTAGE

$V_{IN} = +12\,V$
$V_{OUT} = +5\,V$
$I_L = 40\,mA$
$T_A = 25°C$
$R_{SC} = 0$

OUTPUT VOLTAGE DEVIATION - mV / LOAD DEVIATION - mA vs TIME - μs

OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

$V_{OUT} = +5\,V$
$V_{IN} = +12\,V$
$R_{SC} = 0$
$T_A = +25°C$
$I_L = 50\,mA$

$C_L = 0$
$C_L = 1\,\mu F$

OUTPUT IMPEDANCE - Ω vs FREQUENCY - Hz

TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}] ; R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}] ; R_3 = R_4$$

Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE} (R_3 + R_4)}{R_{sc} R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1
BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

TYPICAL PERFORMANCE

Regulated Output Voltage 5 V
Line Regulation (ΔV_{IN} = 3 V) 0.5 mV
Load Regulation (ΔI_L = 50 mA) 1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 2
BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)
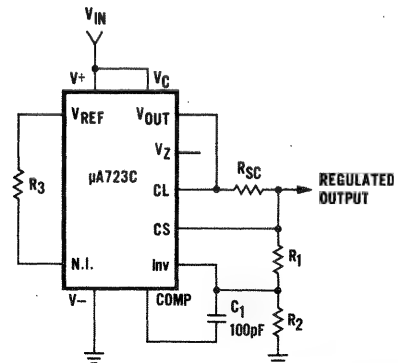
TYPICAL PERFORMANCE

Regulated Output Voltage 15 V
Line Regulation (ΔV_{IN} = 3 V) 1.5 mV
Load Regulation (ΔI_L = 50 mA) 4.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3
NEGATIVE VOLTAGE REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_IN = 3 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Note 3

Figure 4
POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔV_IN = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

Figure 5
POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_IN = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

Figure 6
FOLDBACK CURRENT LIMITING

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_IN = 3 V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Current Limit Knee	20 mA

Figure 7
POSITIVE FLOATING REGULATOR

TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_IN = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

Note 3

Figure 8
NEGATIVE FLOATING REGULATOR
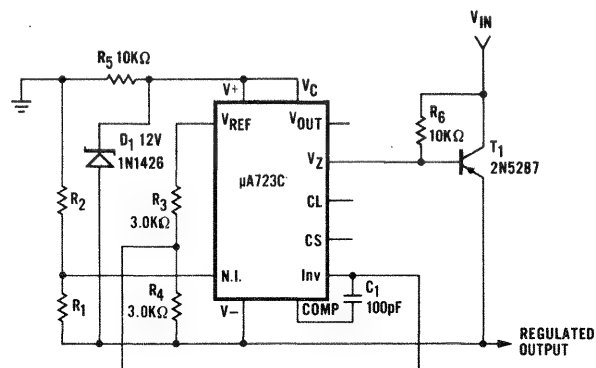
TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔV_IN = 20 V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

Note 3

Figure 9
POSITIVE SWITCHING REGULATOR
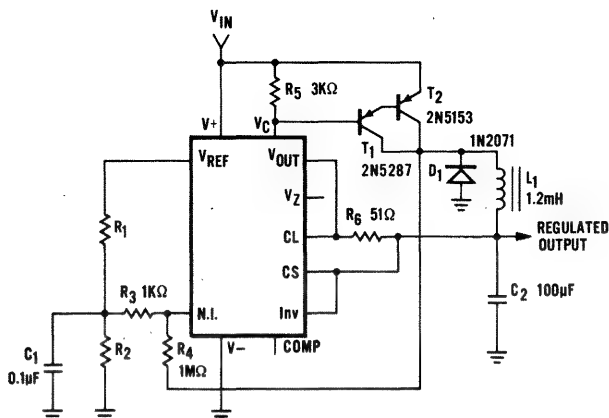
TYPICAL PERFORMANCE

Regulated Output Voltage	$+5$ V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 7

Figure 10
NEGATIVE SWITCHING REGULATOR
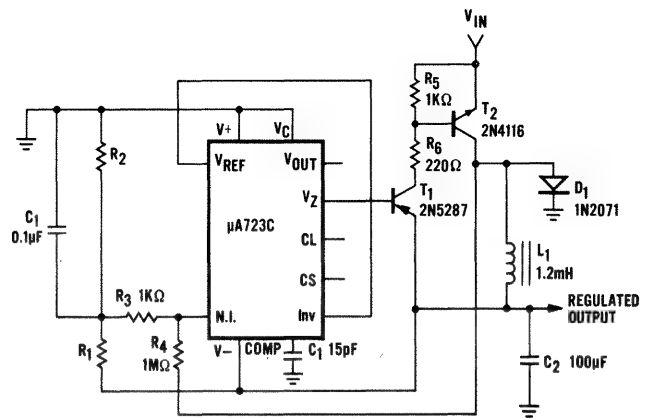
TYPICAL PERFORMANCE

Regulated Output Voltage	-15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Note 3
Note 7

Figure 11
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

Note: Current limit transistor may be used for shutdown if current limiting is not required.
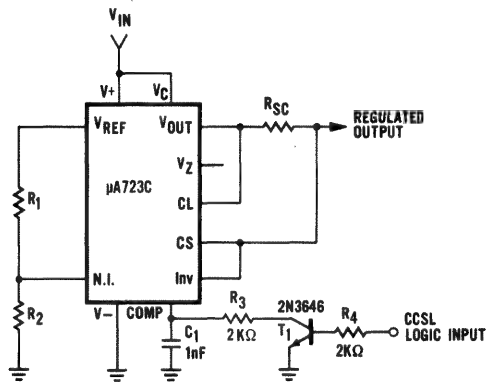
TYPICAL PERFORMANCE

Regulated Output Voltage	$+5$ V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 50$ mA)	1.5 mV

Figure 12
SHUNT REGULATOR
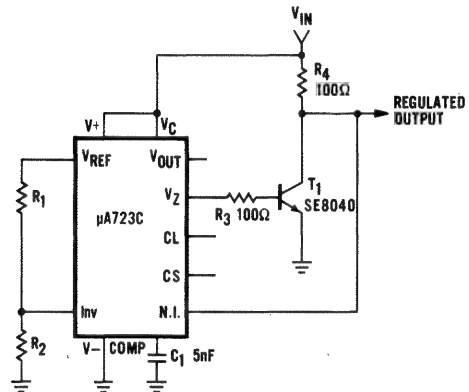
TYPICAL PERFORMANCE

Regulated Output Voltage	$+5$ V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation ($\Delta I_L = 100$ mA)	1.5 mV

Note 3

Figure 13
OUTPUT VOLTAGE ADJUST
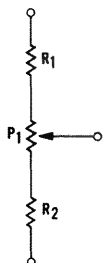
SCHEMATIC DIAGRAM
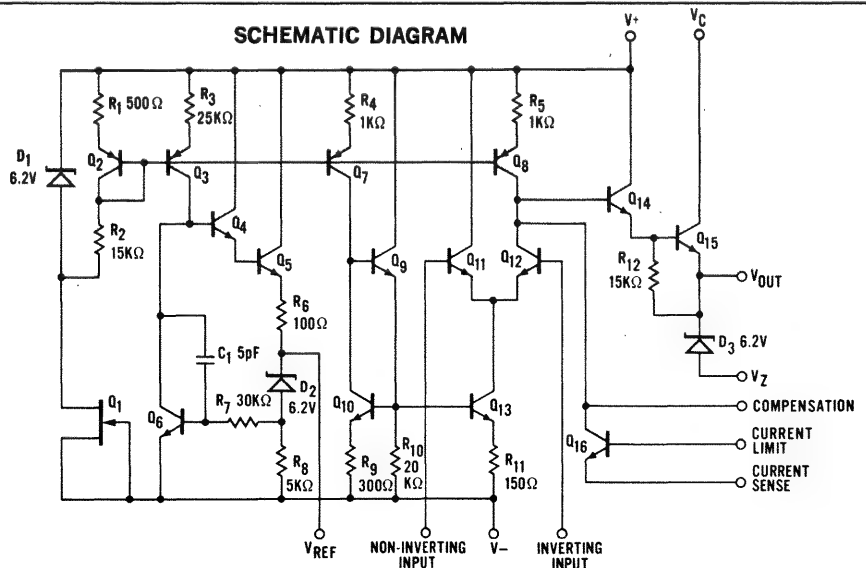
µA727
TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES
- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

GENERAL DESCRIPTION — The µA727 is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters.

ABSOLUTE MAXIMUM RATINGS

|	
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)
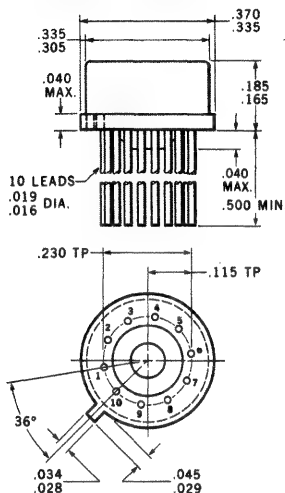
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5J7727312

SCHEMATIC DIAGRAM
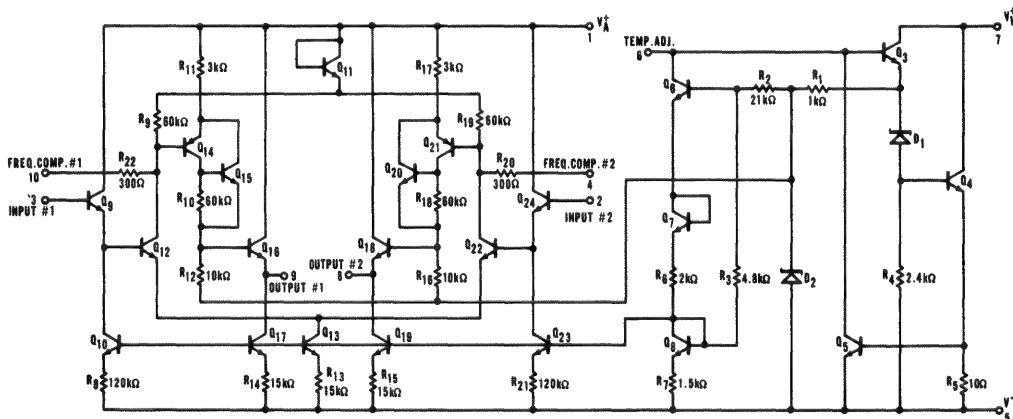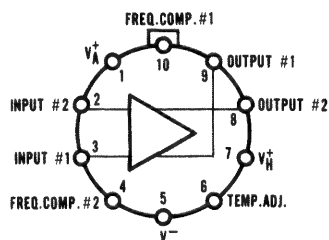
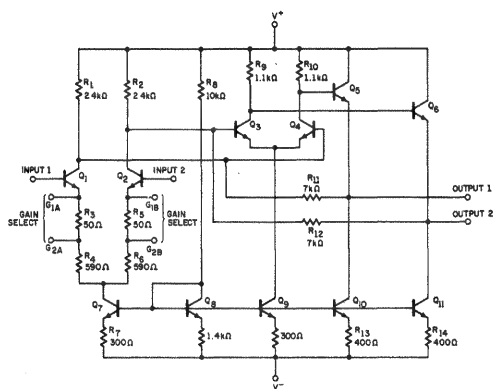**CONNECTION DIAGRAM**
(Top View)

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_H{}^+ = V_A{}^+ = +15\,V$, $V^- = -15\,V$, $R_{ADJ} = 330\,k\Omega$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\,\Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\,\Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\,\Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\,k\Omega$		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\,k\Omega$	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\,\Omega$		3.0		μVrms
Long Term Drift	$R_S \leq 50\,\Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT

TYPICAL PERFORMANCE CURVES

NOISE VOLTAGE AS A FUNCTION OF FREQUENCY
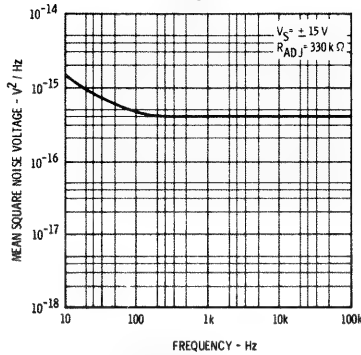
NOISE CURRENT AS A FUNCTION OF FREQUENCY
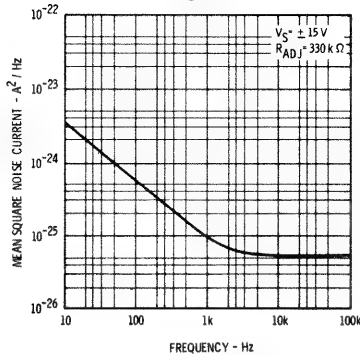
SPOT NOISE FIGURE CONTOURS
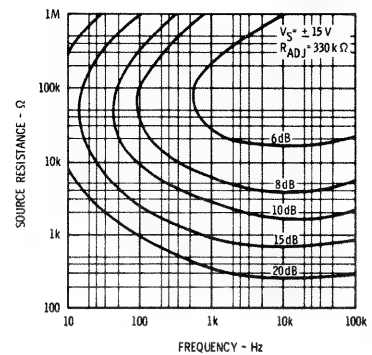
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE
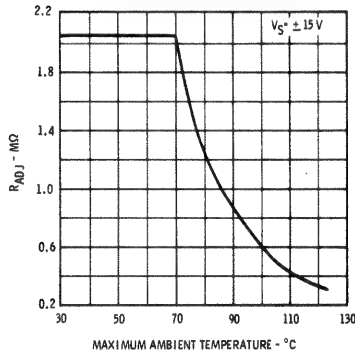
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE
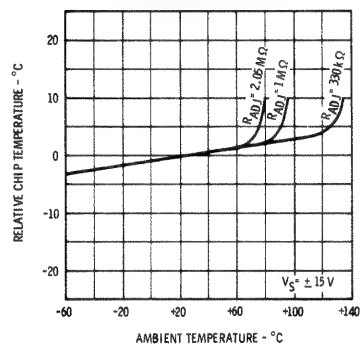
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE
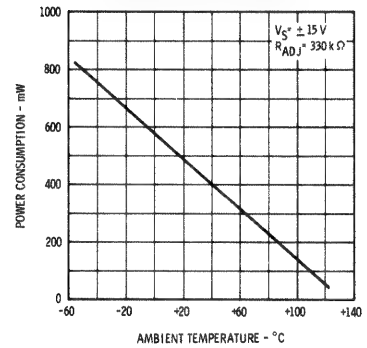
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE
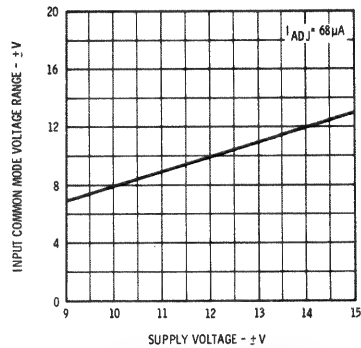
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE
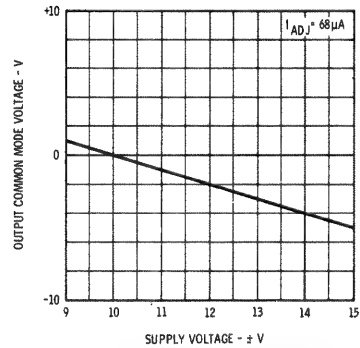
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
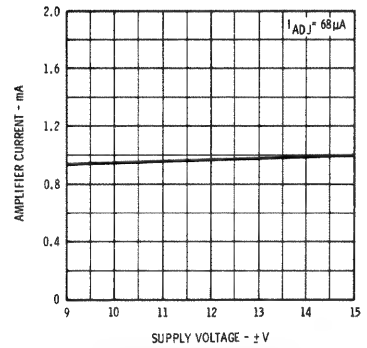
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE
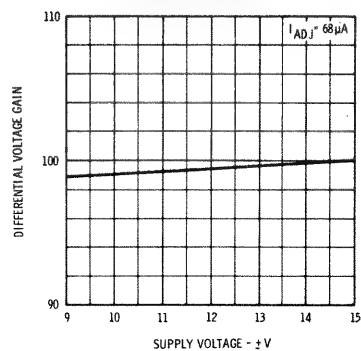
REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE
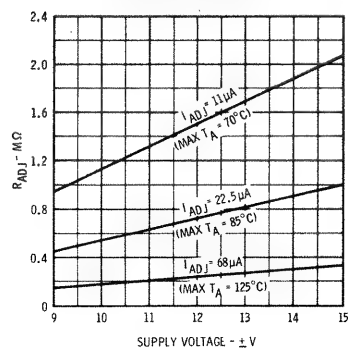
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION
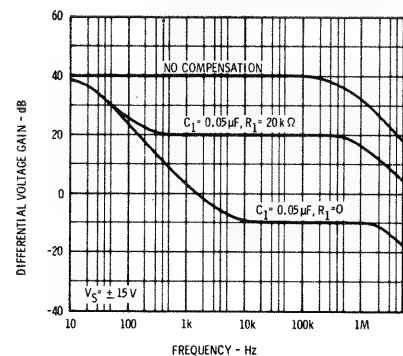
DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero differential output voltage.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the differential output at zero.

DIFFERENTIAL INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

COMMON MODE INPUT RESISTANCE — The resistance looking into both inputs tied together.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in differential output voltage to the change in differential input voltage producing it.

DIFFERENTIAL OUTPUT VOLTAGE SWING — The peak differential output swing that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal with the differential output at zero.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT COMMON MODE VOLTAGE — The average voltage at the two output terminals referred to ground.

OUTPUT SINK CURRENT — The maximum negative current that can be supplied by each output.

DIFFERENTIAL LOAD REJECTION — The ratio of the change in input offset voltage to the change in differential load current producing it.

I_{ADJ} — The current into terminal 6.

FREQUENCY COMPENSATION CIRCUIT
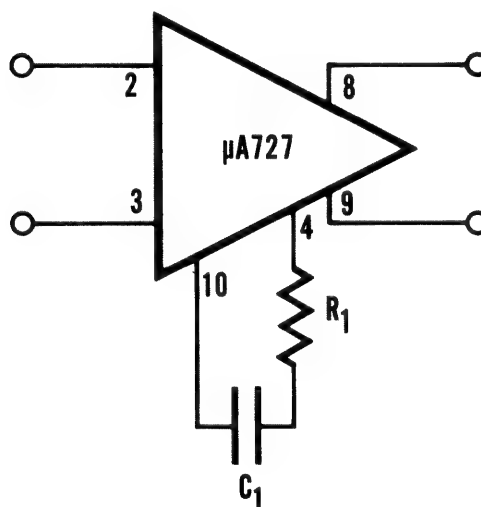
µA727B
TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES
- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

GENERAL DESCRIPTION — The µA727B is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters. For full temperature range operation (−55°C to +125°C) see µA727 data sheet.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-100)

.370 / .335
.335 / .305
.040 MAX.
.185 / .165
10 LEADS .019 / .016 DIA.
.040 MAX.
.500 MIN.
.230 TP
.115 TP
36°
.034 / .028
.045 / .029
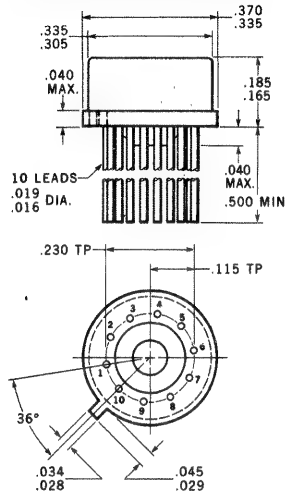
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. U5J7727333

SCHEMATIC DIAGRAM
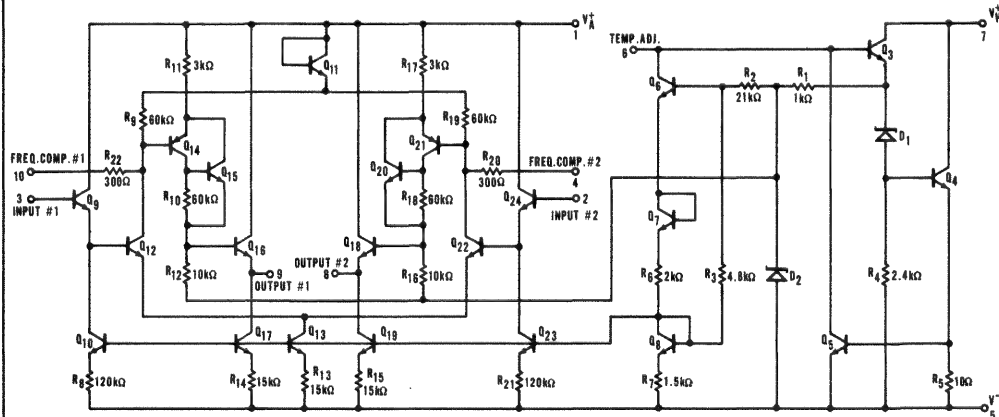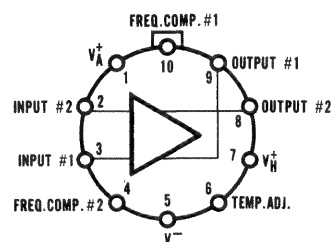
CONNECTION DIAGRAM
(top view)

FREQ.COMP.#1
V$_A^+$ 1 — 10 — 9 — OUTPUT #1
INPUT #2 2 — OUTPUT #2 8
INPUT #1 3 — V$_H^+$ 7
FREQ.COMP.#2 4 — 5 — 6 — TEMP.ADJ.
V−

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_H{}^+ = V_A{}^+ = +15\,V$, $V^- = -15\,V$, $R_{ADJ} = 680\,K\Omega$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\,\Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\,\Omega$		0.6	3.0	$\mu V/°C$
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		$M\Omega$
Common Mode Input Resistance			1000		$M\Omega$
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\,k\Omega$		80		$\mu V/V$
Common Mode Rejection Ratio	$R_S \leq 100\,k\Omega$	70	100		dB
Output Resistance			1.0	4.0	$k\Omega$
Output Common Mode Voltage		-7.0	-5.0	-4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10.0	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15.0	$\mu V/\mu A$
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\,\Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\,\Omega$		5.0		$\mu V/week$
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT
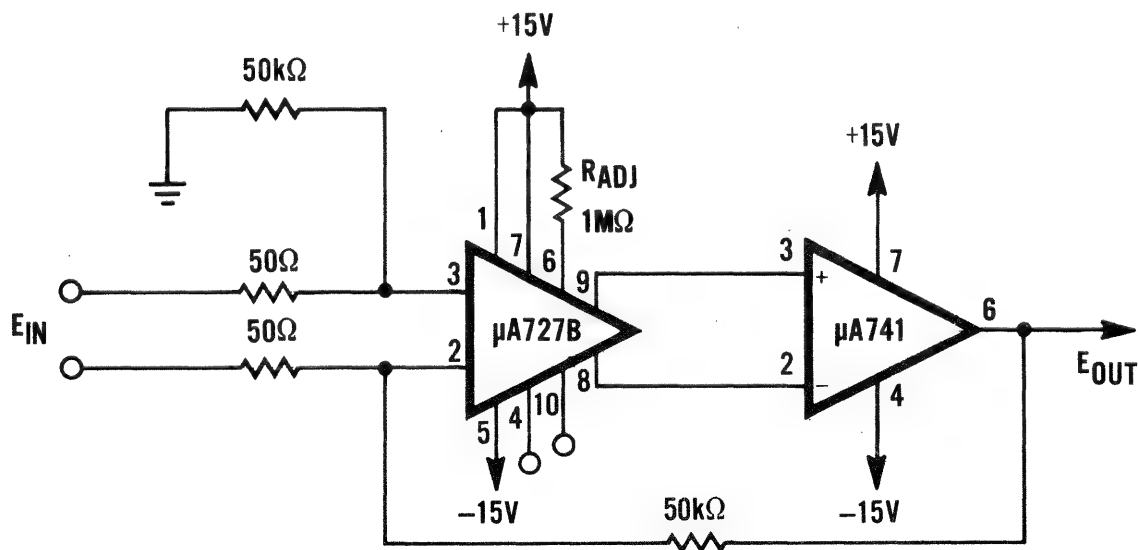
μA733
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES
- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
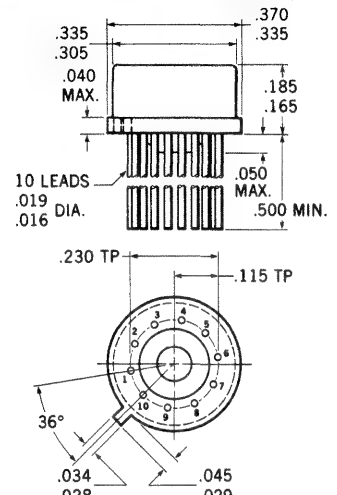- **NO FREQUENCY COMPENSATION REQUIRED**

GENERAL DESCRIPTION — The μA733 is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

ABSOLUTE MAXIMUM RATINGS

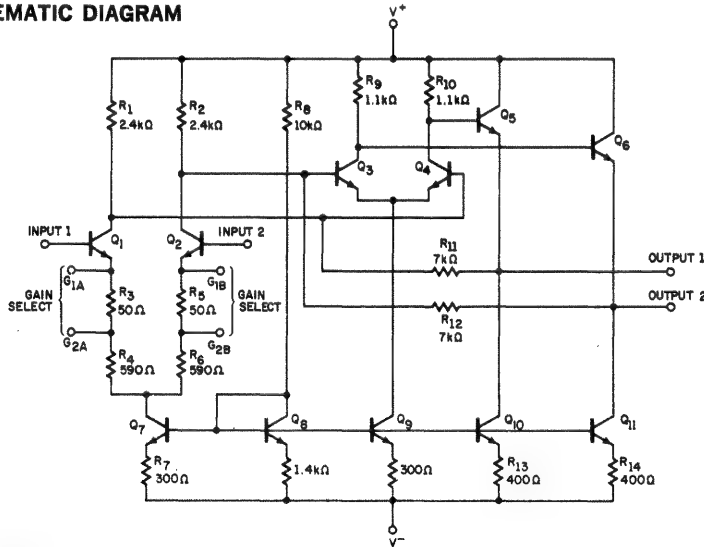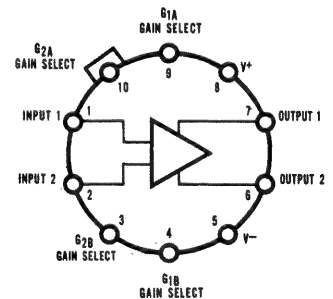|	
Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation TO-100 (Note 1)	500 mW
Operating Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)
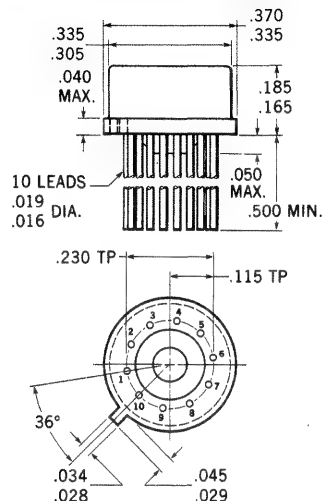
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5F7733312

CONNECTION DIAGRAMS
(TOP VIEW)
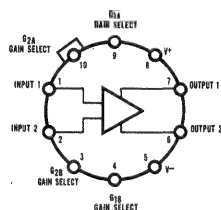
TO-100
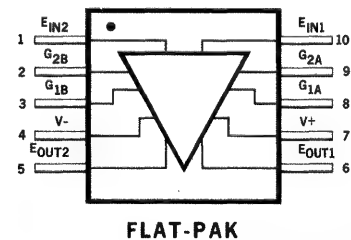
FLAT-PAK

SCHEMATIC DIAGRAM

FLAT PACKAGE
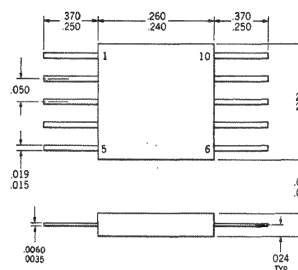
NOTES: All dimensions in inches

ORDER PART NO. U3F7733312

Notes on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

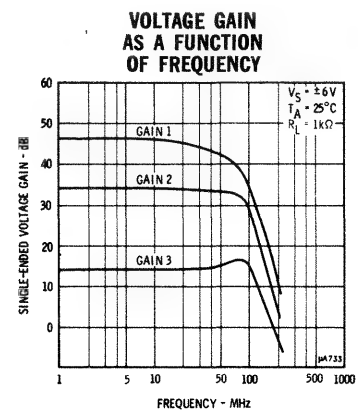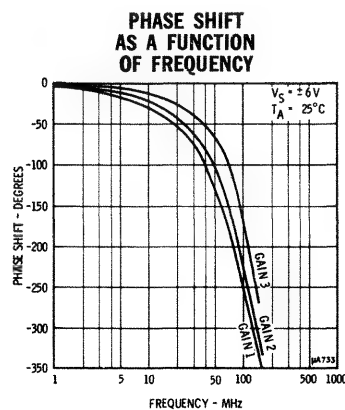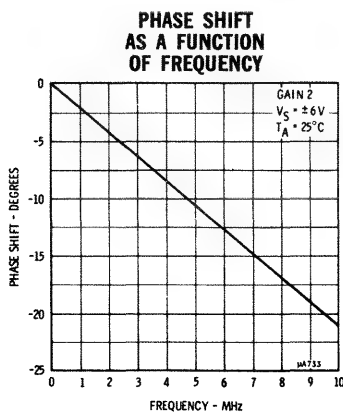313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	$R_S = 50\,\Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\,\Omega$, $V_{out} = 1\,Vpp$				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\,\Omega$, $V_{out} = 1\,Vpp$				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	$R_S = 50\,\Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, $f \leq 100$ kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, $f = 5$ MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

NOTES:
(1) For TO-100 rating applies for case temperature to 125°C; derate linearly at 6.5 mW/°C for ambient temperature above 75°C.
(2) Gain Select pins G_{1A} and G_{1B} connected together.
(3) Gain Select pins G_{2A} and G_{2B} connected together.
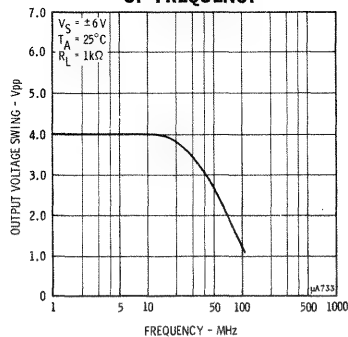(4) All Gain Select pins open.

TYPICAL PERFORMANCE CURVES

PHASE SHIFT AS A FUNCTION OF FREQUENCY

PHASE SHIFT AS A FUNCTION OF FREQUENCY

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY
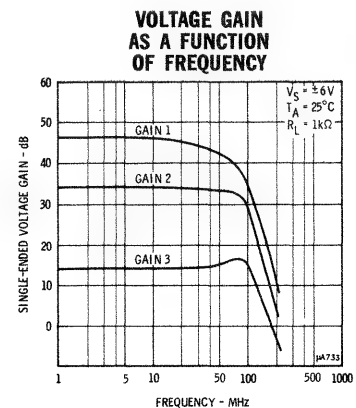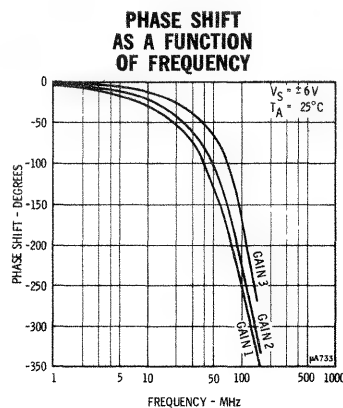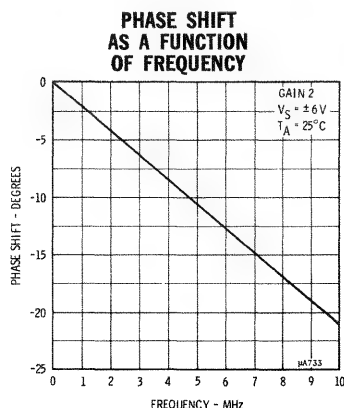
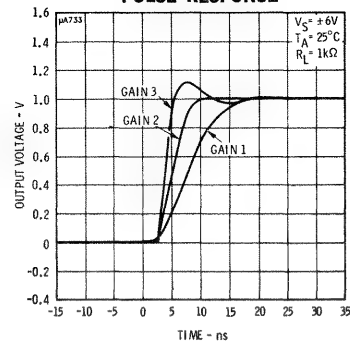## TYPICAL PERFORMANCE CURVES

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY
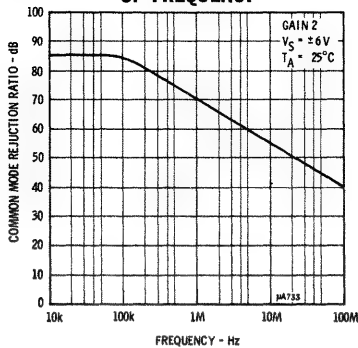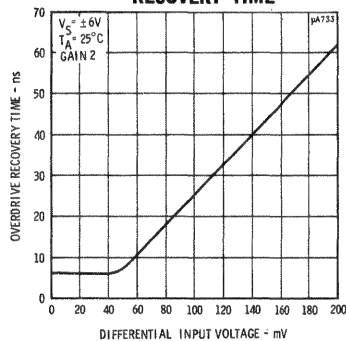

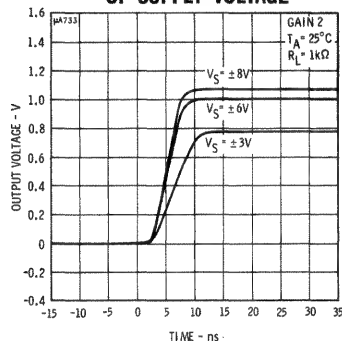### OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY
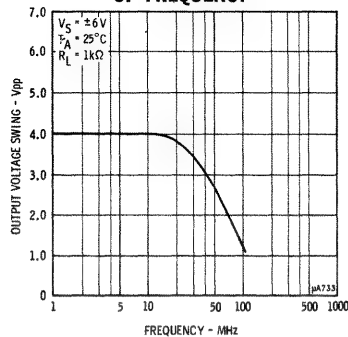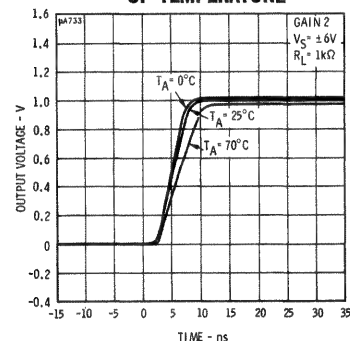

PULSE RESPONSE
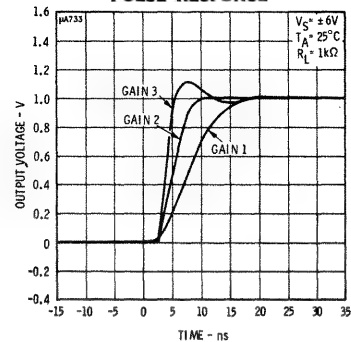
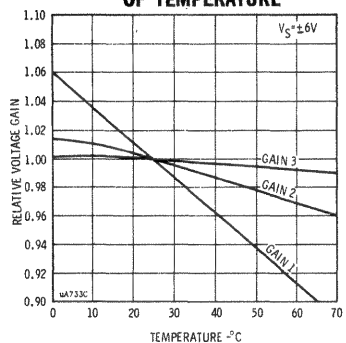### DIFFERENTIAL OVERDRIVE RECOVERY TIME
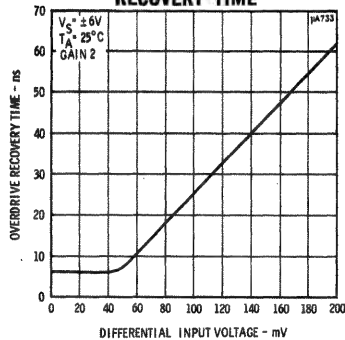
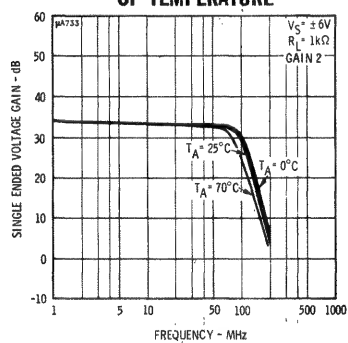### PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE
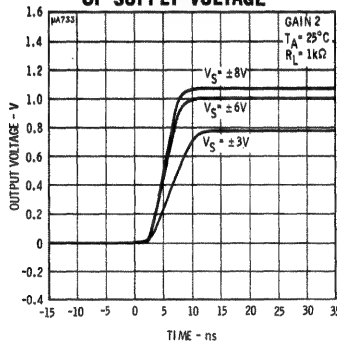
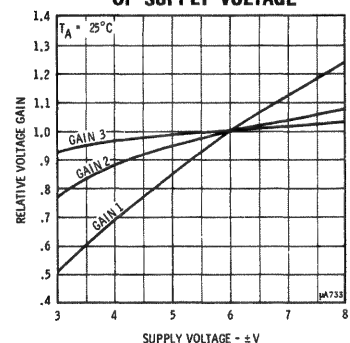### PULSE RESPONSE AS A FUNCTION OF TEMPERATURE
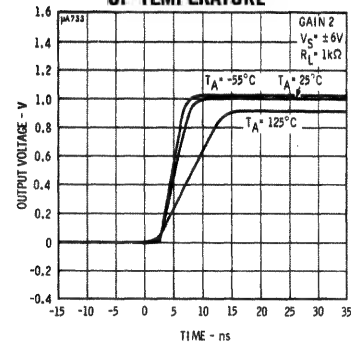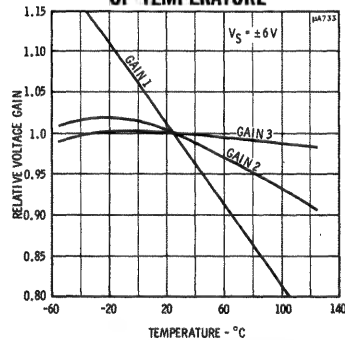
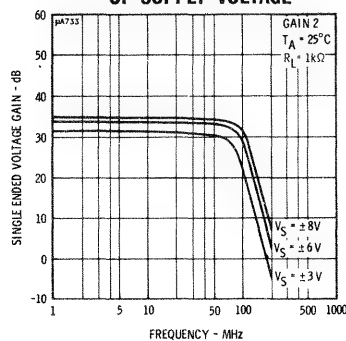### VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE

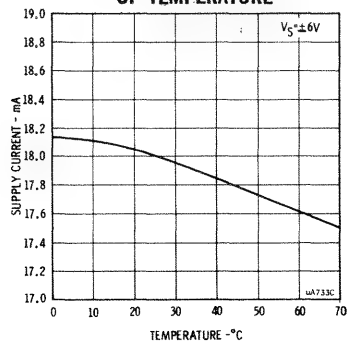### GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE
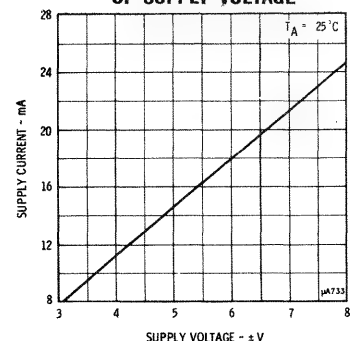

GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

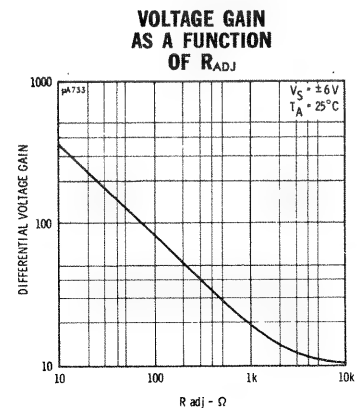OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

OUTPUT SINK CURRENT — The peak negative current available at either output of the amplifier.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with no load.

TYPICAL PERFORMANCE CURVES

OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

VOLTAGE GAIN ADJUST CIRCUIT

VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}

µA733C
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES
- 120 MHz BANDWIDTH
- 250 kΩ INPUT RESISTANCE
- SELECTABLE GAINS OF 10, 100, AND 400
- NO FREQUENCY COMPENSATION REQUIRED

GENERAL DESCRIPTION — The µA733C is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

For full temperature range performance (—55°C to 125°C), see µA733 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	—65°C to 150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)

NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5F7733393

SCHEMATIC DIAGRAM

Notes on Page 2

CONNECTION DIAGRAM
(TOP VIEW)

Note: Pin 5 connected to case.

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	$R_S = 50\ \Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, $f \leq 100$ kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, $f = 5$ MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA

NOTES:
(1) Rating applies for ambient temperatures to 70°C.
(2) Gain Select pins G_{1A} and G_{1B} connected together.
(3) Gain Select pins G_{2A} and G_{2B} connected together.
(4) All Gain Select pins open.

TYPICAL PERFORMANCE CURVES

PHASE SHIFT AS A FUNCTION OF FREQUENCY

PHASE SHIFT AS A FUNCTION OF FREQUENCY

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

TYPICAL PERFORMANCE CURVES

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT — The difference between the currents into the two input terminals.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

OUTPUT SINK CURRENT — The peak negative current available at either output of the amplifier.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with no load.

TYPICAL PERFORMANCE CURVES

OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

VOLTAGE GAIN ADJUST CIRCUIT

VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}

µA737E
COLOR TV CHROMA DEMODULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA737E is a monolithic silicon integrated circuit which demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs.

FEATURES
- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B - E_Y OUTPUT**
- **PLUGS INTO A STANDARD 9-PIN MINIATURE TUBE SOCKET OR SOLDERS INTO A PRINTED BOARD**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+28 V
Minimum Load Resistance	3 kΩ
Peak-to-Peak Reference Input Voltage	5 V
Peak-to-Peak Chroma Input Voltage	5 V
Internal Power Dissipation	450 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	+260°C

PHYSICAL DIMENSIONS
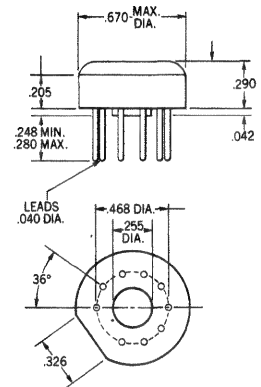
ORDER PART NO. U8F7737394

SCHEMATIC DIAGRAM
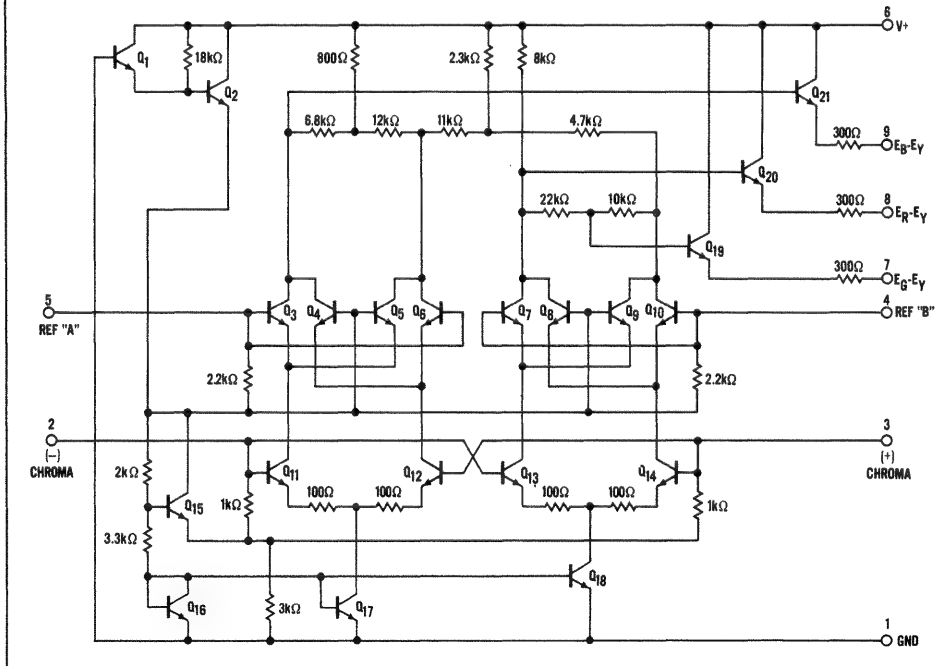
CONNECTION DIAGRAM
(TOP VIEW)

FAIRCHILD

SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
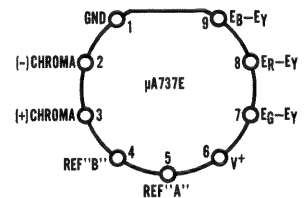
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 24$ V, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_C = 0$, $R_L = 1$ MΩ	4.5	8.0	11.5	mA
	$e_C = 0$, $R_L = 1$ MΩ, $T_A = 70°C$		8.0	12.0	mA
	$e_C = 0$	16.5	21	25.5	mA
	$e_C = 0$, $T_A = 70°C$		21		mA
Internal Power Dissipation	$e_C = 0$		320	410	mW
	$e_C = 0$, $T_A = 70°C$		320	420	mW
DC Voltage at any Output Terminal	$e_C = 0$	12.5	14.7	16.5	V
	$e_C = 0$, $T_A = 70°C$	12.0	14.3		V
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.2	1.0	V
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		V
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		V
Reference Input Resistance	$e_C = 0$		1.7		kΩ
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5Vp\text{-}p$		0.4	0.7	V
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5Vp\text{-}p$	3.5	3.8	4.2	V
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5Vp\text{-}p$	0.75	1.0	1.25	V
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5Vp\text{-}p$	8.0	10		V
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5Vp\text{-}p$	96	104	112	Degrees
Highest Peak-to-Peak Demodulator AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	V

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(—) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (—) Chroma input.

TYPICAL ELECTRICAL CHARACTERISTICS
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

SUPPLY CURRENT VERSUS SUPPLY VOLTAGE
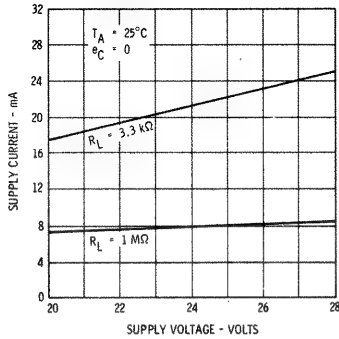
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE
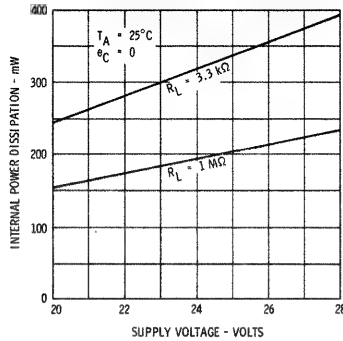
DIFFERENCE BETWEEN THE SUPPLY VOLTAGE AND THE DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE
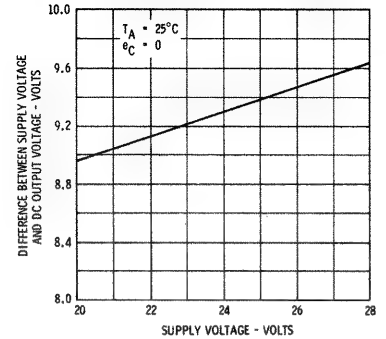
SUPPLY CURRENT VERSUS LOAD RESISTANCE
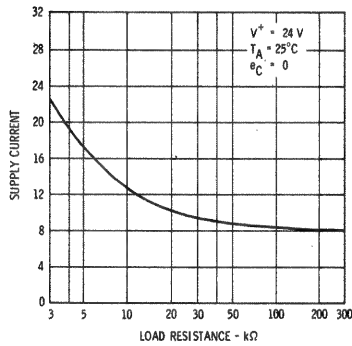
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE
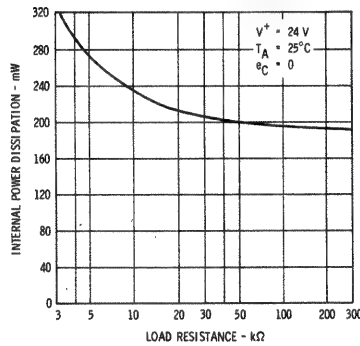
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE
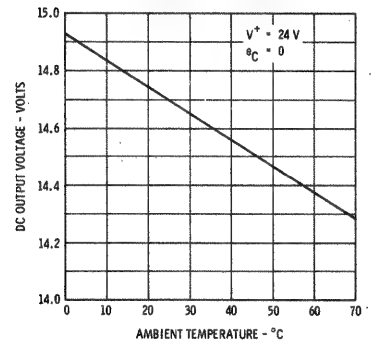
DEMODULATION LINEARITY
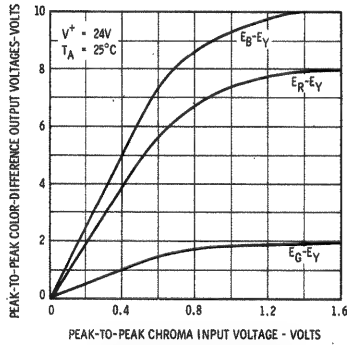
DEMODULATION ANGLES AND RELATIVE GAINS
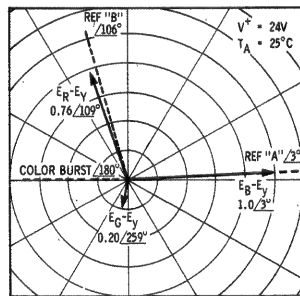
DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS
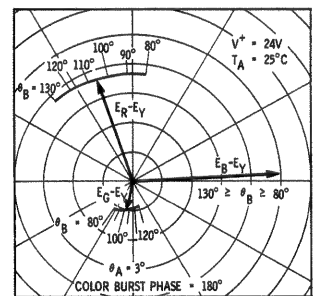
DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS
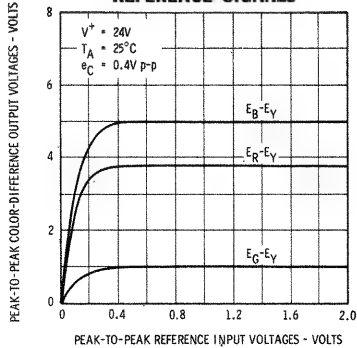
TEST CIRCUIT 1
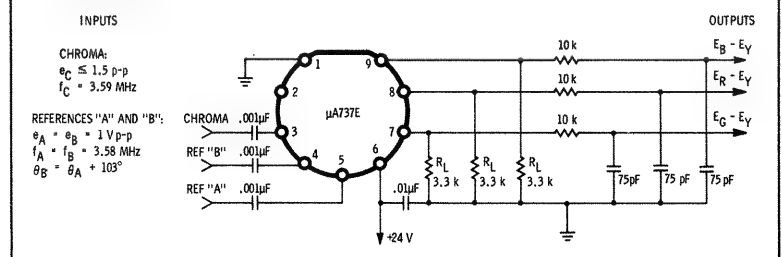
µA739C
DUAL LOW-NOISE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The µA739C consists of two identical operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These low-noise, high-gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltage and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

FEATURES
- SINGLE OR DUAL SUPPLY OPERATION
- LOW NOISE FIGURE, 2.0 dB
- HIGH GAIN, 20,000 V/V
- LARGE COMMON MODE RANGE, ±11 V
- EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE
- NO LATCH-UP
- OUTPUT SHORT CIRCUIT PROTECTED

TYPICAL APPLICATIONS
- DUAL OPERATIONAL AMPLIFIER
- PHONO AND TAPE STEREO PREAMPLIFIER
- TV REMOTE CONTROL RECEIVER
- DUAL COMPARATOR
- SENSE AMPLIFIER
- OSCILLATOR
- ACTIVE FILTER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	260°C
Output Short-Circuit Duration, $T_A = 25°C$ (Note 3)	30 seconds

TYPICAL DUAL IN-LINE PACKAGE
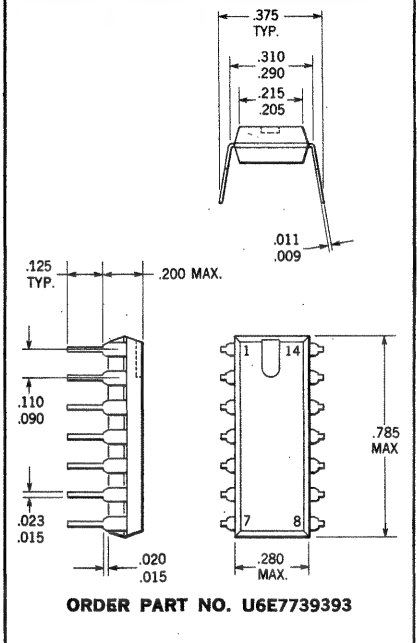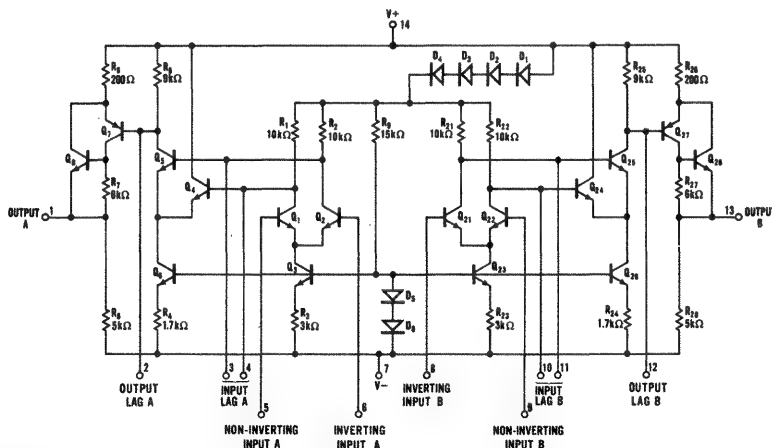
ORDER PART NO. U6E7739393

SCHEMATIC DIAGRAM

Notes on page 2

CONNECTION DIAGRAM
(TOP VIEW)

*Planar is a patented Fairchild process.
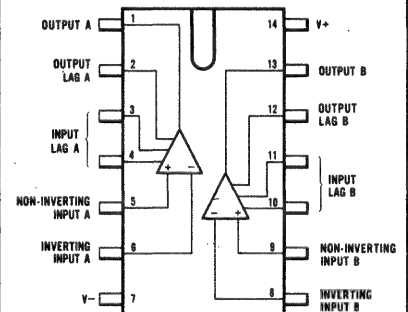
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($V_S = \pm15$ V, $R_L = 50$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm5.0$ V	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	$f = 1.0$ kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50		μV/V
Power Consumption	$V_{OUT} = 0$		270	420	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 10$ kΩ, BW = 10 Hz to 10 kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm20$ mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm20$ mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	$C_I = 0.1\ \mu F$, $R_I = 4.7\ \Omega$		1.0		V/μs
Channel Separation (See Figure 3)	$R_S \leq 10$ kΩ, $f = 10$ kHz		140		dB

The following specifications apply for $V_S = \pm4.0$ V, $T_A = 25°C$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Power Consumption	$V_{OUT} = 0$		20		mW
Large-Signal Voltage Gain	$V_{OUT} = \pm1.0$ V	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

PULSE RESPONSE
WAVEFORMS
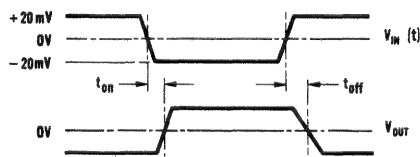
Figure 1

FREQUENCY RESPONSE
TEST CIRCUIT
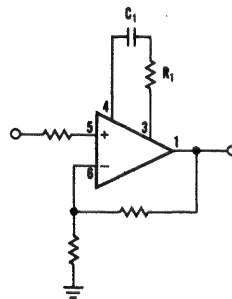
Figure 2

CHANNEL SEPARATION
TEST CIRCUIT

$$\text{SEPARATION} = \frac{V_{OA}}{V_{OB}} \cdot \frac{1}{100}$$
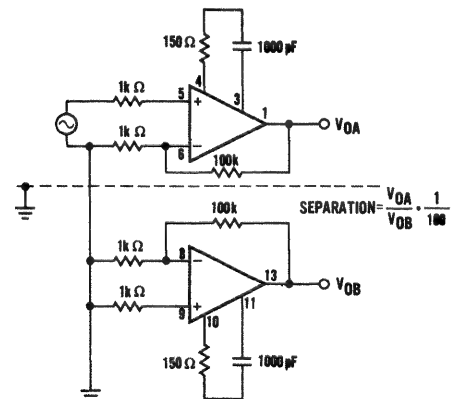
Figure 3

NOTES:
(1) Rating applies at ambient temperature below 60°C. Derate at 7.7 mw/°C above 60°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply.

TYPICAL PERFORMANCE CURVES

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY
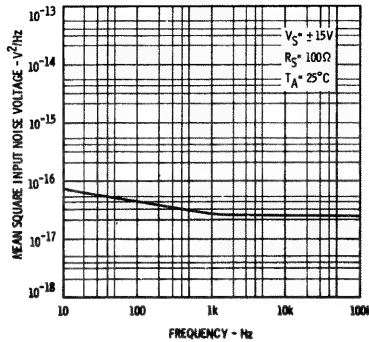
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY
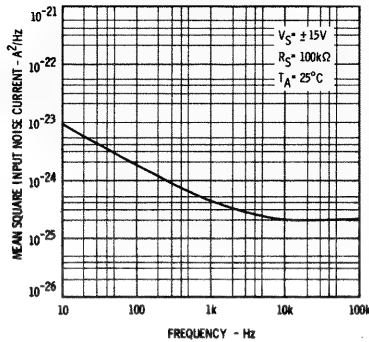
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE
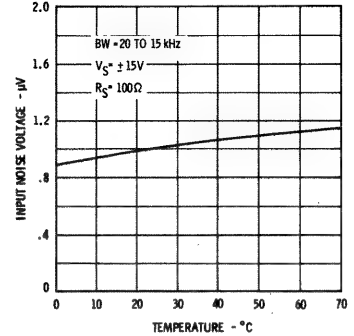
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE
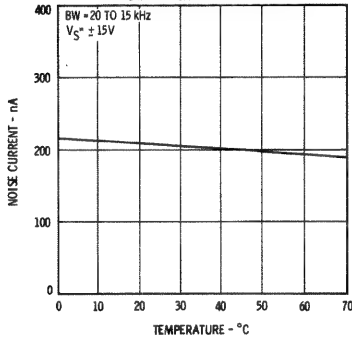
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE
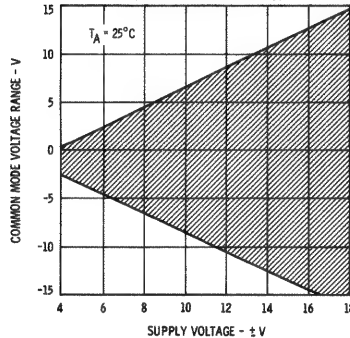
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE
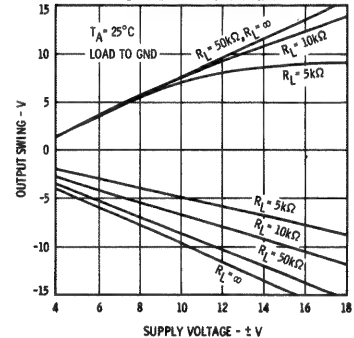
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE
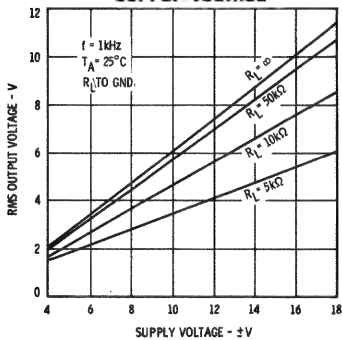
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
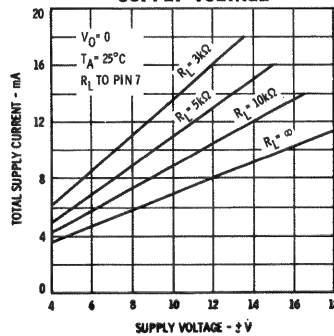
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD
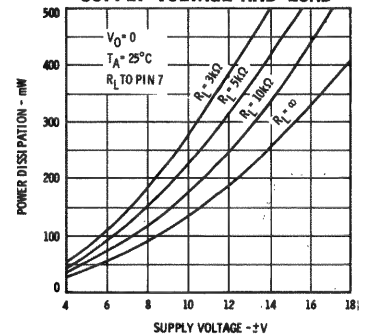
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE
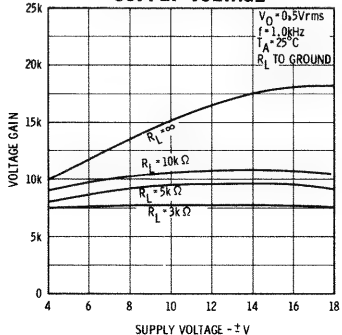
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE
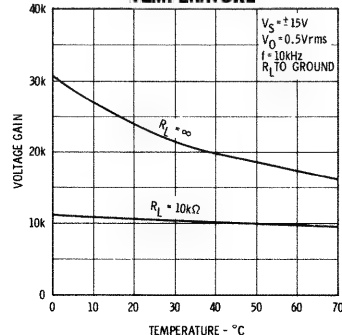
INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

TYPICAL PERFORMANCE CURVES

CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY

OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS
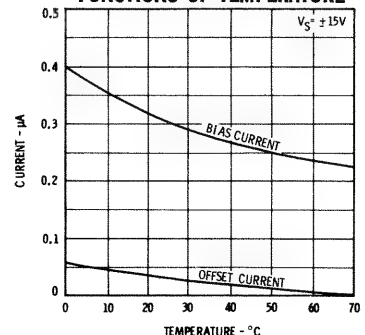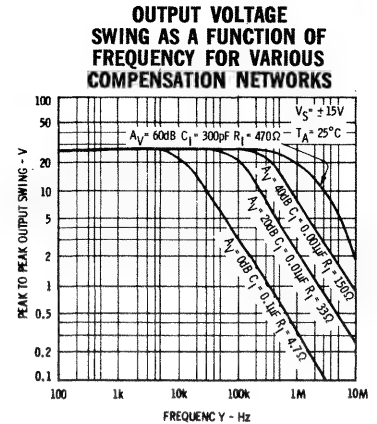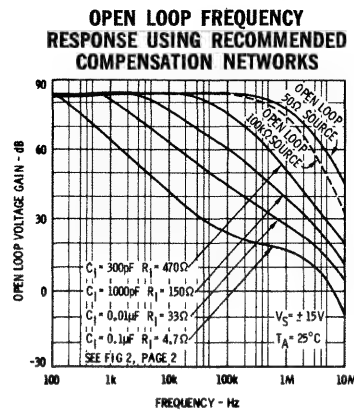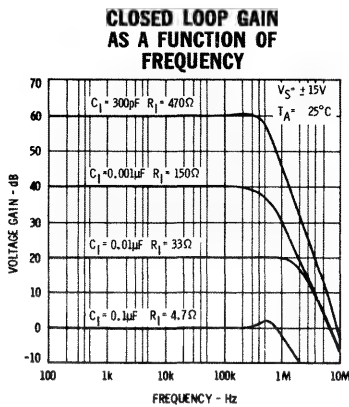
FREQUENCY COMPENSATION NETWORK
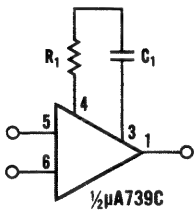
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION
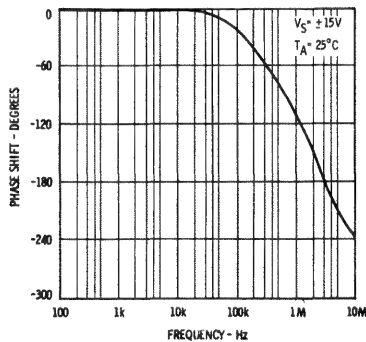
CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY
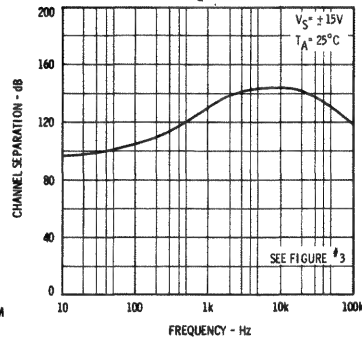
CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE
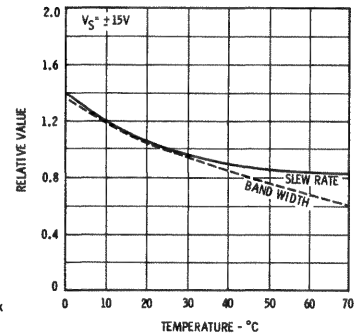
TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER—RIAA EQUALIZED
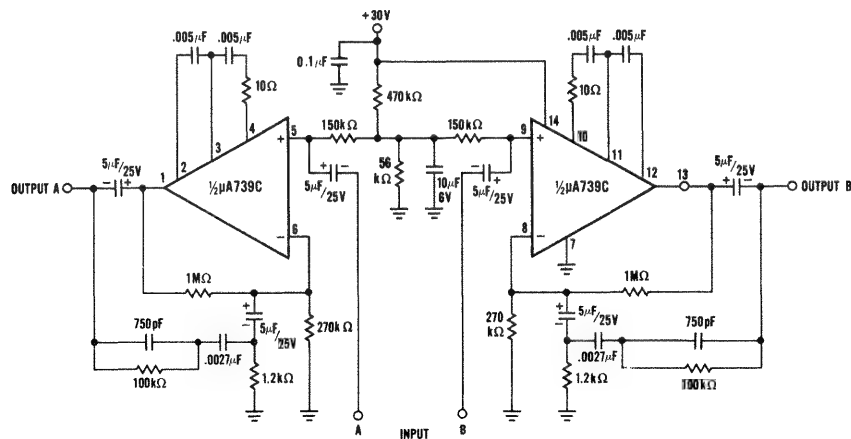
TYPICAL PERFORMANCE

Gain 40 dB at 1 kHz, RIAA equalized
Input overload point, 80 mV rms
Noise level, 2μV referred to input
Signal to noise ratio, 74 dB below 10 mV
Channel separation @ 1 kHz, 80 dB

µA741
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

GENERAL DESCRIPTION — The µA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the µA741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The µA741 is short-circuit protected, has the same pin configuration as the popular µA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline
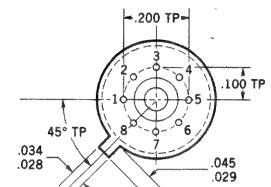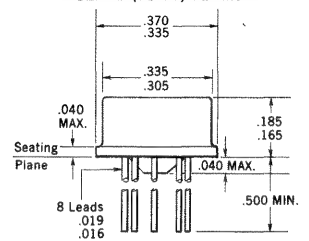
NOTES. Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7741312

SCHEMATIC DIAGRAM
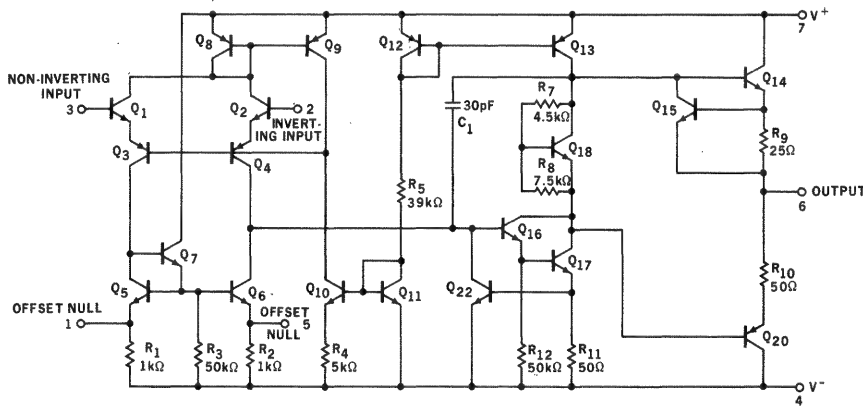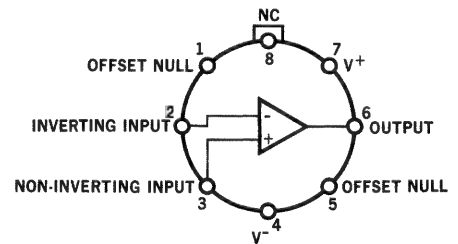
CONNECTION DIAGRAM
(TOP VIEW)

NOTE: PIN 4 CONNECTED TO CASE

NOTES:
(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435
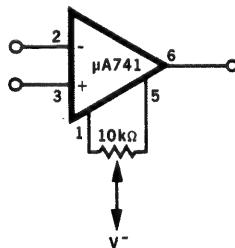
FAIRCHILD LINEAR INTEGRATED CIRCUITS μA741

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25$°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for -55°C $\leq T_A \leq +125$°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

OPEN LOOP VOLTAGE GAIN
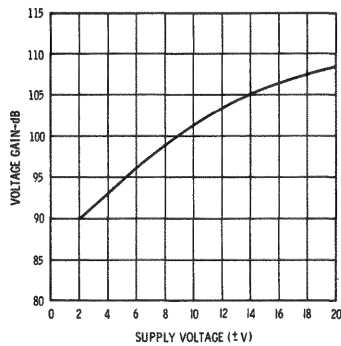
VOLTAGE OFFSET NULL CIRCUIT

ABSOLUTE MAXIMUM POWER DISSIPATION
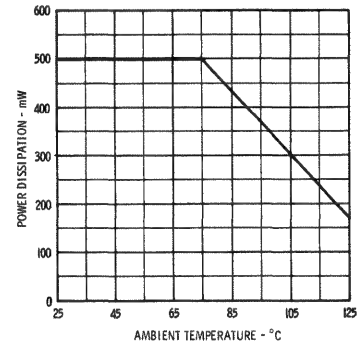
OPEN LOOP FREQUENCY RESPONSE
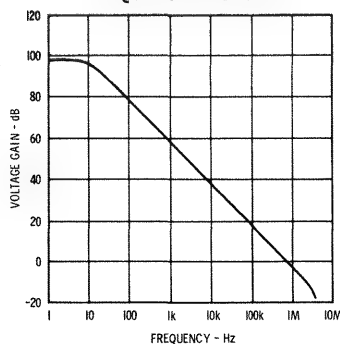
TRANSIENT RESPONSE TEST CIRCUIT
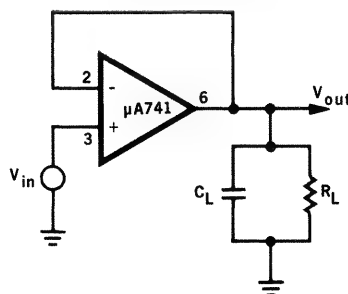
TRANSIENT RESPONSE
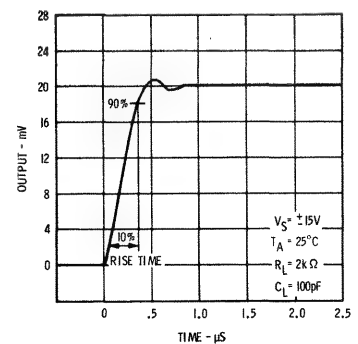
µA741C
HIGH PERFORMANCE OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The µA741C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the µA741C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The µA741C is short-circuit protected, has the same pin configuration as the popular µA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (—55°C to +125°C) see µA741 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Storage Temperature Range TO-99	—65°C to +150°C
Dual-In-Line	—55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec) TO-99	300°C
(Soldering, 10 sec) Dual-In-Line	260°C
Output Short-Circuit Duration (Note 2)	Indefinite

PHYSICAL DIMENSIONS
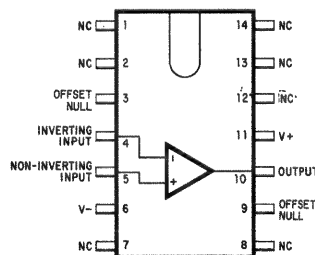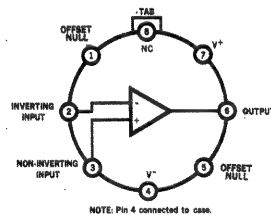in accordance with
JEDEC (TO-99) outline
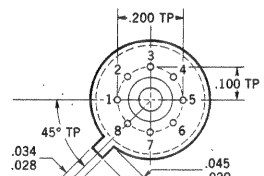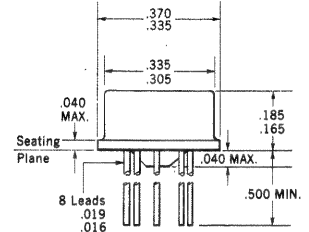
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
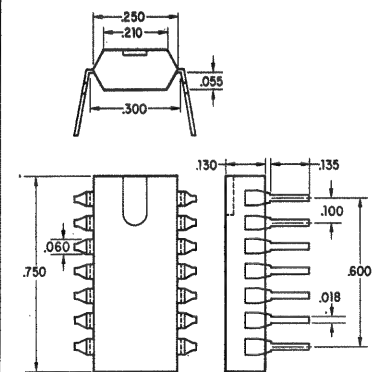Package weight is 1.22 grams

ORDER PART NO. U5B7741393

SCHEMATIC DIAGRAM
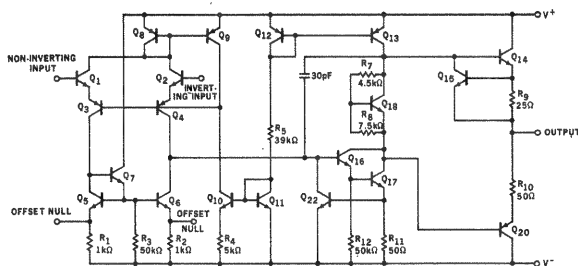
CONNECTION DIAGRAMS

NOTE: Pin 4 connected to case.

TYPICAL DUAL IN-LINE PACKAGE

NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO. U6E7741393

*Planar is a patented Fairchild process.

NOTES:
(1) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(2) Short circuit may be to ground or either supply.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435
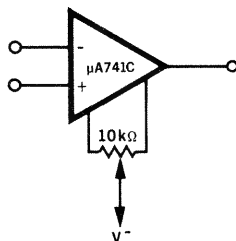
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ				
	$C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN

OPEN LOOP FREQUENCY RESPONSE

TRANSIENT RESPONSE
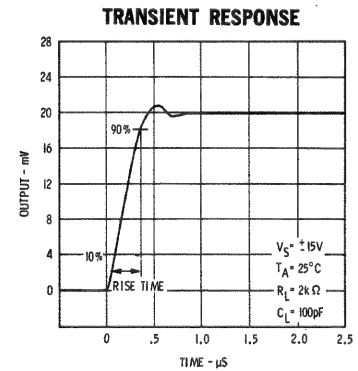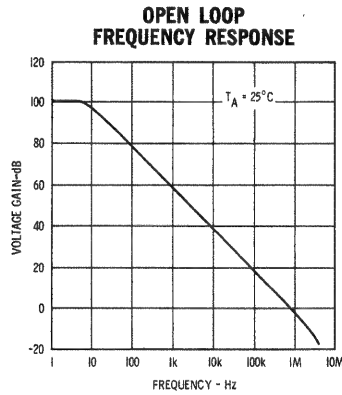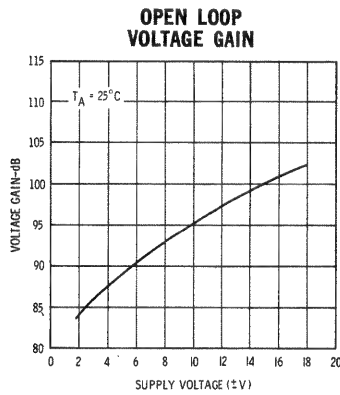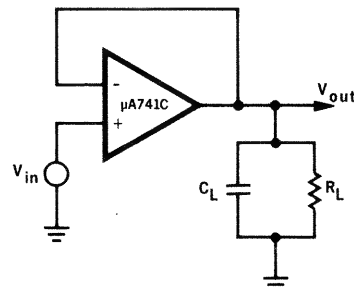

VOLTAGE OFFSET NULL CIRCUIT

TRANSIENT RESPONSE TEST CIRCUIT

µA751C
DIFFERENTIAL VIDEO AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES
- VOLTAGE GAIN 600
- 200Ω INPUT LINE TERMINATION
- 10 ns TYPICAL PROPAGATION DELAY
- NO FREQUENCY COMPENSATION REQUIRED

GENERAL DESCRIPTION — The µA751C is a monolithic two-stage differential input differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series feedback is used for high gain and excellent gain stability. Internal sense line termination minimizes line reflections and eliminates the need for external termination components. External frequency compensation is not required. The device is particularly useful as a read amplifier in high-speed thin film memories. Other applications include general purpose video and pulse amplifiers where high gain and excellent gain stability are required. For applications where lower gain is required and where input termination is not desirable, see the µA733 data sheet.

ABSOLUTE MAXIMUM RATINGS
|	
Supply Voltage	±8 V
Differential Input Voltage	±2 V
Common Mode Input Voltage (Note 1)	±1 V
Output Current	7.5 mA
Internal Power Dissipation (Note 2)	250 mW
Operating Temperature Range	−0° to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 second time limit)	300°C

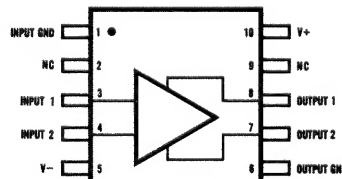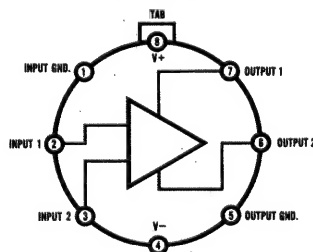### PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline
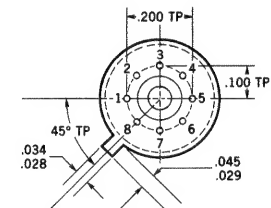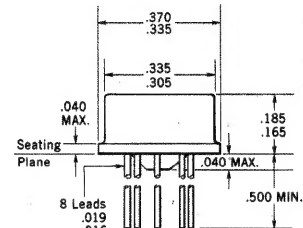
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams
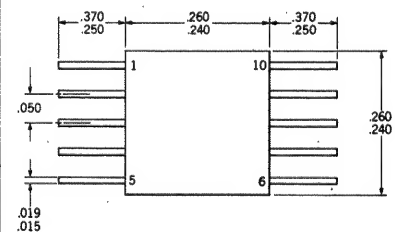
ORDER PART NO. U5B7751393

SCHEMATIC DIAGRAM
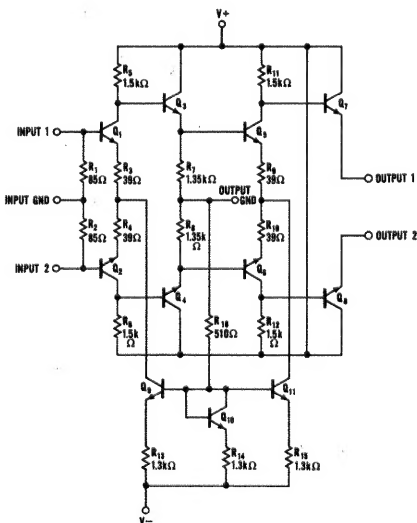
CONNECTION DIAGRAMS
(TOP VIEW)

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

ORDER PART NO. U3H7751393

*Planar is a patented Fairchild process.

NOTES:
(1) Input voltage limited due to internal resistor between inputs and ground.
(2) Rating applies for ambient temperatures to 70°C.

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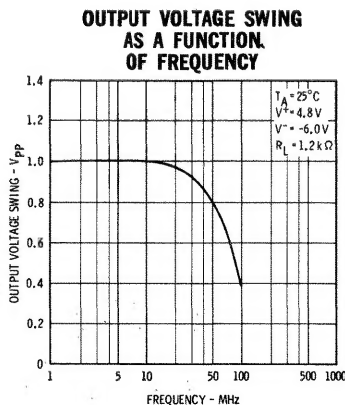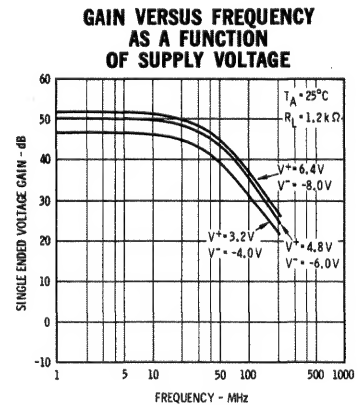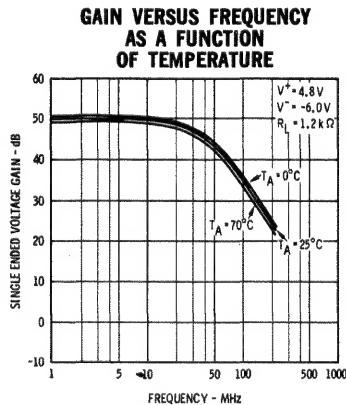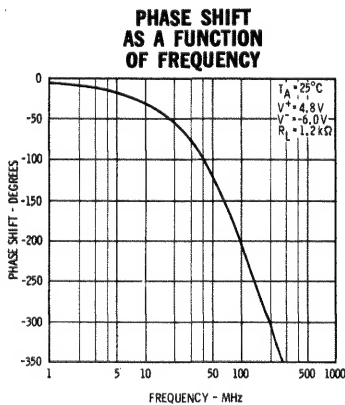313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435
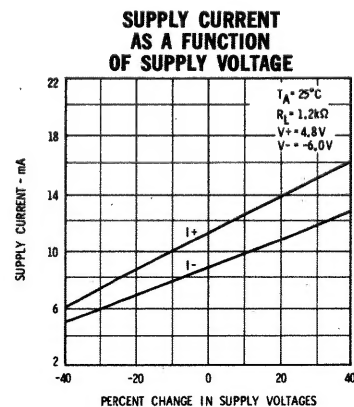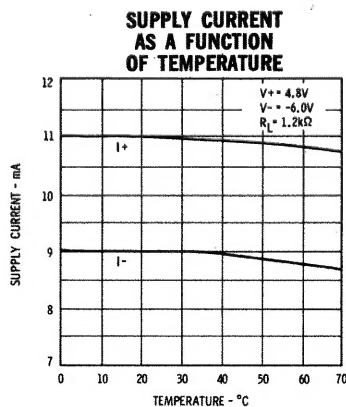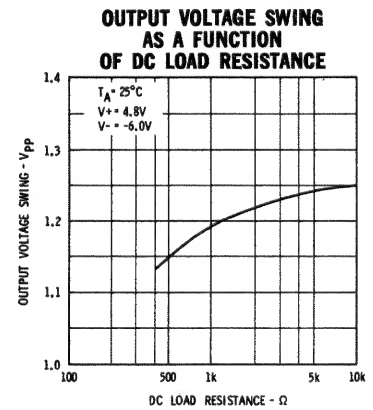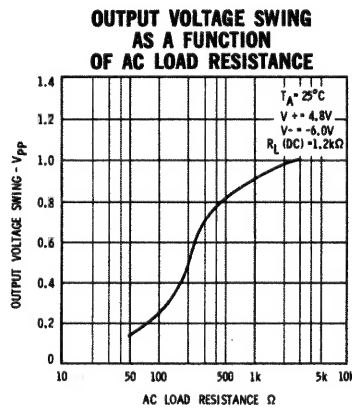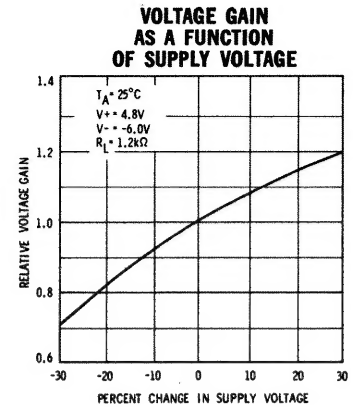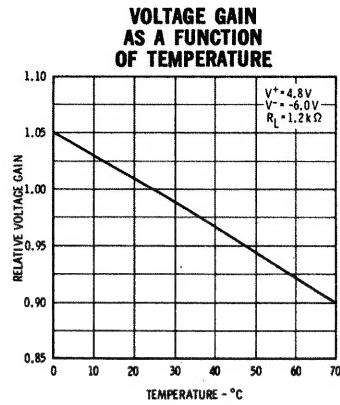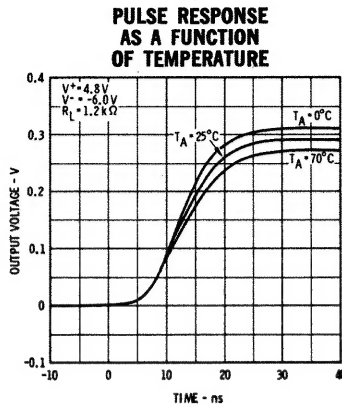
FAIRCHILD LINEAR INTEGRATED CIRCUITS μA751C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +4.8$ V, $V^- = -6.0$ V unless otherwise specified)

PARAMETER (see definitions, page 4)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain		375	600	825	
Bandwidth			30		MHz
Risetime	$V_{IN} = 1.0$ mV		12	25	ns
Propagation Delay	$V_{IN} = 1.0$ mV		10	20	ns
Differential Input Resistance		140	180	220	Ω
Input Capacitance			2.0		pF
Output Noise Voltage	BW = 20 Hz to 30 MHz		7.5		mVrms
Common Mode Rejection Ratio	$V_{CM} = 20$ mV		46		dB
Supply Voltage Rejection Ratio			60		dB
Output Offset Voltage			0.5	1.5	V
Output Common Mode Voltage		0.9	1.8	3.5	V
Output Voltage Swing			1.2		Vpp
Output Resistance			50		Ω
Positive Power Supply Current			11	14	mA
Negative Power Supply Current			9.0	12	mA

TYPICAL PERFORMANCE CURVES

PHASE SHIFT AS A FUNCTION OF FREQUENCY

GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE

GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

DIFFERENTIAL OVERDRIVE RECOVERY TIME

TYPICAL PERFORMANCE CURVES

PULSE RESPONSE AS A FUNCTION OF TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE

VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF AC LOAD RESISTANCE

OUTPUT VOLTAGE SWING AS A FUNCTION OF DC LOAD RESISTANCE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

TEST CIRCUIT

V+=4.8V

INPUT

1kΩ

2
INPUT 1
5Ω

3
INPUT2

1

μA751C

8

7

6

4   5

50Ω

1kΩ

V−=−6.0V

OUTPUT 1

OUTPUT 2

56pF

56pF

1.2kΩ   510Ω   1.2kΩ   510Ω

NOTE: Circuit measures device performance with common mode and differential pulses simultaneously applied and typical output loading. Pin numbers are for TO-99 package.

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH — The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME — The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY — The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE — The resistance seen between the two input terminals.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT OFFSET VOLTAGE — The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT COMMON MODE VOLTAGE — The average of the voltages at the two output terminals.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without distortion. This includes the unbalance caused by output offset voltage.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal.

POWER SUPPLY CURRENT — The current required from the power supplies to operate the device with each output externally loaded with 1.2 kΩ.